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Fabrication of single-electron devices using dispersed nanoparticles and fitting the measurement results to curves calculated based on percolation model

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Abstract We calculated the connection probability , P_C, between electrodes on the basis of the triangular lattice percolation model for investigating the effect of distance variation between electrodes and the electrode width on fabricated capacitively coupled single-electron transistors. single-electron devices were fabricated via the dispersion of gold nanoparticles (NPs). The NPs were dispersed via the repeated dropping of an NP solution onto a chip. The experimental results were fitted to the calculated results, and the fitting parameters were compared with the occupation probability , P_O, which was estimated for one drop of the NP solution. On the basis of curves of the drain current vs. the drain-source voltage ($I_{\mathrm{D}} - V_{\mathrm{DS}}$) measured at 77 K, the current was suppressed at approximately 0 V.

Keywords Gold nanoparticle solution · Drop · Percolation

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1 Introduction

Single-electron devices has been investigated by many researchers [1] [2]. Single-electron devices have numerous applications including single-electron turnstiles [3], single-electron pumps and high accurate current sources [4] [5] [6] [7] , current mirror [8], single-electron memory [9], a Coulomb blockade thermometer [10], and highly sensitive sensors [11] [12] , among others.

The single-electron transistor (SET) is a key single-electron device [1] [13] . SETs have been fabricated using a combination of electron beam lithography and shadow evaporation [8]. An SET comprises two small tunnel junctions on both sides of an island electrode and a gate electrode. Nanoparticles (NPs) are also used as the island electrode in SETs [14]; however, a special technique is required to fabricate the small nanometer-scale gap. Meanwhile, the Coulomb blockade effect has been observed for single-electron devices fabricated via the repeated dispersion of gold NPs and the forming of drain (D) and source (S) electrodes [15].

In this work, we fabricated drain, source, and gate (G) electrodes and fabricated devices by repeatedly dispersing of gold NPs. To disperse the NPs, we dropped a gold NP solution onto a chip on which electrodes had been fabricated.; the we dried the chip. This process of dropping the NP solution and drying was repeated. This method is a simple way to fabricate an NP SET (NP-SET).

2 Calculation of connection probability on the basis of percolation theory

When NPs are dispersed, the connection probability (P_C) between the electrodes can be calculated on the

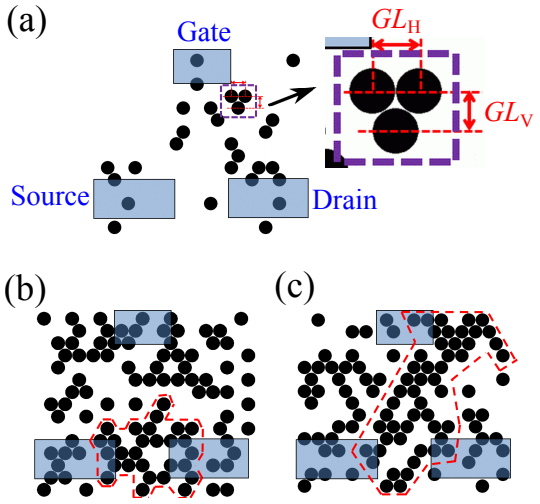

Fig. 1 Schematic of dispersed particles and electrodes on a triangular lattice percolation model. (a) All electrodes are isolated. (b) The source (S) and drain (D) electrodes are connected and the gate (G) electrode is isolated ("S-D_(G)") . (c) The S, D, and G electrodes are connected ("S-D-G").

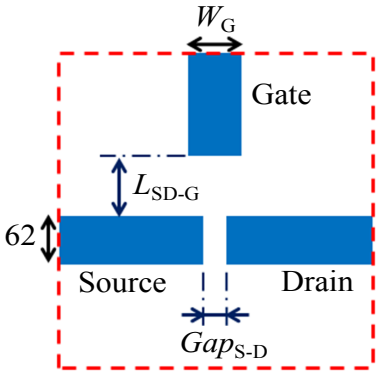

Fig. 2 Defining the width of each electrode and the length between the electrodes. The area enclosed by a dashed line is that used in calculation based on the triangular lattice percolation model.

basis of percolation theory. Fig. 1 shows a schematic of dispersed particles and electrodes. A triangular lattice was used for calculations. When the occupation probability, P_O, is low , all electrodes are isolated (Fig. 1 (a), $P_O = 0.15$). The area indicated by the arrow is an enlarged view of the region outlined with a dashed line. GL_H and GL_V are the horizontal and vertical grid lengths, respectively. When P_O increases, the S and D electrodes are connected and the G electrode is isolated (Fig. 1 (b), $P_O = 0.4$); we refer to this state as "S-D_(G)". When P_O further increased, not only the S and D electrodes but also the G electrode are connected (Fig. 1 (c), $P_O = 0.45$); we refer to this state as "S-D-G". In Fig. 1 (b) and (c), a group of particles that connects the electrodes is denoted by a dashed line. The "S-D_(G)" configuration means that the G electrode couples to the S and D electrodes capacitively. Because the "S-D_(G)" configuration is needed for fabricating a capacitively coupled SET (C-SET), the "S-D_(G)" configuration is very important for the dispersion of the NPs to enable the fabrication of an NP-SET.

The width of each electrode and the length between the electrodes are defined in Fig. 2. The area enclosed by a dashed line is the area used in the calculation based on the triangular lattice percolation model. This area is 200 grids × 200 grids or larger. The width of the source is fixed at 62 grids. Gap_{S-D}, L_{SD-G}, and W_G are the gap length between the source and the drain, the length between the source and the gate, and the width of the gate, respectively.

The dependence of P_C on P_O for a Gap_{S-D} of 6 grids is shown in Fig. 3 (a). Open circles and filled rectangles show the P_C of S-D_(G) and that of S-D-G. L_{SD-G} and W_G are 76 grids and 66 grids, respectively. With increasing P_O, the P_C of S-D_(G) increases gradually from a P_O of approximately 0.2 to approximately 1.0 at a P_O of approximately 0.4. The notation S-D_(G) means that S and D are connected and that G is isolated, whereas the notation S-D-G means that S, D, and G are connected. Because the P_C of S-D-G rapidly increases from a P_O of 0.45 to a P_C of 1.0 at a P_O of 0.5, the P_C of S-D_(G) decreases rapidly from a P_O of 0.45 and reaches zero at a P_O of 0.5. This value of P_O (0.5) is consistent with the critical probability in the triangular lattice percolation model [17]. With increasing P_O, the P_C of S-D_(G) increases gradually and then decreases rapidly. $P_{C,MAX}$ and the full-width of half-maximum (FWHM) are defined as the maximum value of the P_C of S-D_(G) and the width of the P_C of S-D_(G) at half of $P_{C,MAX}$, respectively.

Fig. 3 (b) shows the dependence of the P_C of S-D_(G) ($P_{C(S-D_(G))}$) on P_O for Gap_{S-D} of 6, 10, 14, and 20 grids. Open circles, triangles, rectangles, and diamonds are data points for Gap_{S-D}=6, 10, 14, and 20 grids, respectively. L_{SD-G} and W_G in Fig. 3 (b) are 76 and 66 grids, respectively. With increasing P_O, the $P_{C,(S-D_(G))}$ gradually increases from approximately 0.2, 0.25, 0.3, and 0.38 for Gap_{S-D} of 6, 10, 14, and 20 grids. For wider Gap_{S-D}, a larger P_O is needed before the $P_{C(S-D_(G))}$ begins to increase . All of the $P_{C(S-D_(G))}$ decrease rapidly from a P_O of 0.45 and reach zero at a P_O of 0.5. $P_{C,MAX}$ and FWHM decrease with increasing Gap_{S-D}. The conditions for fabricating a C-SET are preferably adjusted via the dispersion of the NPs such that the maximum value of $P_{C(S-D_(G))}$ is high

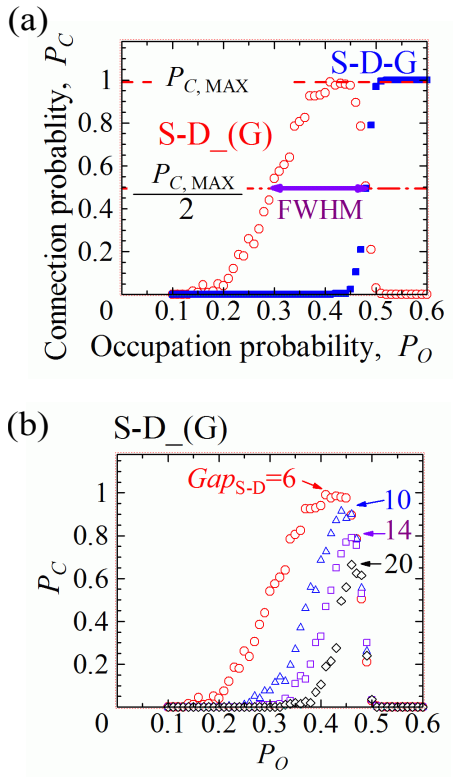

Fig. 3 The dependence of P_C on P_O. L_{SD-G} and W_G are 76 grids and 66 grids, respectively. (a) P_C of S-D_(G) (open circle) and that of S-D-G (filled rectangle) for Gap_{S-D} of 6 grids. (b) P_C of S-D_(G) for Gap_{S-D} of 6 (circle), 10 (triangle), 14 (rectangle), and 20 grids (diamond).

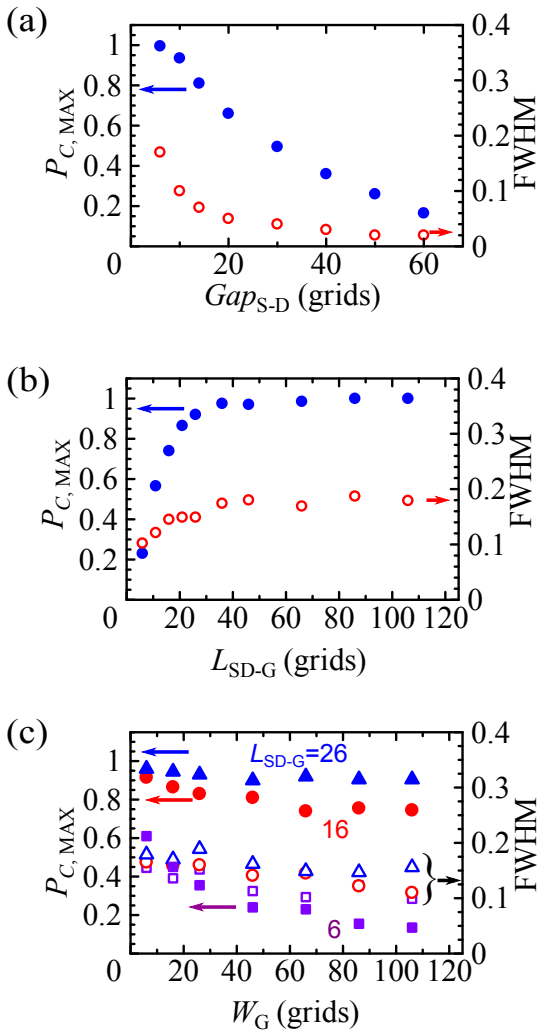

Fig. 4 The dependence of the $P_{C,MAX}$ and the FWHM on (a) the Gap_{S-D}, (b) on the L_{SD-G}, and (c) on the W_G. Filled symbols indicate the $P_{C,MAX}$ and open symbols indicate the FWHM. The L_{SD-G} and the W_G are 76 and 66 grids in (a), and the Gap_{S-D} and the W_G are 6 and 66 grids, respectively in (b). The Gap_{S-D} is 6 grids in (c).

and the FWHM is wide. Thus, we calculated $P_{C,MAX}$ and FWHM for various conditions.

Fig. 4 (a), (b), and (c) show the dependence of the $P_{C,MAX}$ and the FWHM on the Gap_{S-D}, L_{SD-G}, and W_G, respectively, where filled symbols indicate the $P_{C,MAX}$ and open symbols indicate the FWHM. In Fig. 4 (a), L_{SD-G} and W_G are 76 and 66 grids, respectively. With increasing Gap_{S-D}, the $P_{C,MAX}$ decreases gradually, but the FWHM decreases rapidly. Thus, a small gap is better for fabricating a C-SET. In Fig. 4 (b), Gap_{S-D} and W_G are 6 and 66 grids, respectively. With increasing L_{SD-G}, the $P_{C,MAX}$ increases rapidly from 6 to 30 grids of L_{SD-G} and reaches approximately 1.0 at 40 grids of L_{SD-G}. The FWHM increases and becomes almost constant when L_{SD-G} exceeds 40 grids. With respect to the fabrication of SETs, the L_{SD-G} is an important parameter for the gate capacitance, C_G. A long L_{SD-G} makes C_G small and the gate voltage large, resulting in Coulomb oscillation, which is direct evidence of a C-SET. The results in Fig. 4 (b) indicate that 40 grids of L_{SD-G} is sufficient. In Fig. 4 (c), the $P_{C,MAX}$ dependence on W_G is plotted for L_{SD-G}s of 6, 16, and 26 grids; the Gap_{S-D} is 6 grids. With increasing L_{SD-G}, $P_{C,MAX}$ decreases, starting from approximately 0.6 for an L_{SD-G} of 6, from approximately 1.0 for an L_{SD-G} of 16, and that decreases more slightly from about 1.0 for L_{SD-G} of 26. Thus, W_G is not an effective parameter except in cases where the L_{SD-G} is small.

3 Experimental details

3.1 Fabrication and measurement methods

Four chips (chips A, B, C, and D) were used in the experiments. These chips were covered with an SiO_2 layer. The D, S, and G electrodes were fabricated using e-beam lithography (EBL) and shadow evaporation

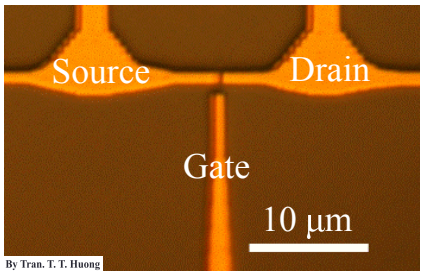

Fig. 5 An optical micrograph of fabricated electrodes.

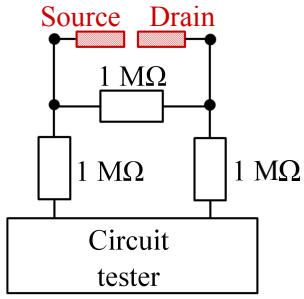

Fig. 6 A schematic of the resistance measuring circuit between the source and the drain. The resistance was measured at room temperature.

[16]. A double layer resist was used for EBL. The bottom layer was 800-nm-thick 11% copolymer, and the top layer was 60-nm-thick 2% PMMA. The accelerating voltage and the beam current were 30 kV and 120 pA, respectively. The area for EBL was square of 200 μm × 200 μm. After the photo-resist was developing in an isopropanol aqueous solution, resist bridges were formed.

Using shadow evaporation, 20-nm-thick gold film was evaporated from an angle of +14°, and 45-nm-thick gold film was evaporated from an angle of -14°. After the photo-resist was lifted off in acetone, 12 gaps between the S and D electrodes were fabricated in an area of 200 μm × 200 μm. The $L_{\mathrm{SD-G}}$ was designed to be 1000 nm, whereas the widths of the S and G electrodes were both designed to be 800 nm. $Gap_{\mathrm{S-D}}$ was an important parameter in these experiments. The gaps between S and D were fabricated using shadow evaporation, and the resist bridges formed by EBL served used as shadow masks during the evaporation. The W_{G} was different for each $Gap_{\mathrm{S-D}}$. The $Gap_{\mathrm{S-D}}$, and W_{G} values are summarized in Table. 1.

Table 1 Table of the $Gap_{\mathrm{S-D}}$, W_{G}, and the number of gaps for each chip, N.

Chip	$Gap_{\mathrm{S-D}}$ /nm	W_{G} /nm	N
A, B, C	300	1100	3
	200	1000	3
	140	940	3
	100	900	3
D	140	940	12

An optical micrograph of fabricated electrodes is shown in Fig. 5.

One micro-liter of citric acid gold colloidal solution was dropped onto the chips. The colloidal solution contained 70 ppm of NPs with a diameter of 15 nm. After the dropping procedure, each chip was dried approximately 20 min. The resistance between the S and D electrodes was then measured. A schematic of the resistance measurement circuit is shown in Fig. 6. The resistance was measured at room temperature. Three resisters with a nominal resistance of 1 MΩ and a circuit tester were used for measuring the resistance . The three resisters were serially connected to the circuit tester, and probes were connected to either side of the middle resistor among the three serially connected resistors. When the probes were connected directly (short circuit), the resistance reading indicated by the circuit tester was 1.98 MΩ. When the probes were placed apart (open circuit), the circuit tester indicated a resistance of 2.97 MΩ. When these two probes were connected to the S and D electrodes, the maximum value of the measurable resistance was approximately 97 MΩ. When the resistance between the S and D electrodes was less than 97 MΩ, we assumed that the gap between the S and D electrodes was bridged by gold NPs. The data for $I_{\mathrm{D}} - V_{\mathrm{DS}}$, where I_{D} and V_{DS} are the drain current and voltage between the drain and the source, respectively, were collected using a semiconductor parameter analyzer. The two-probe technique was used for the measurements.

3.2 Estimation of the occupation probability per drop

To compare the measured resistance results with the values calculated on the basis of percolation theory, the occupation probability of gold NPs per drop of the gold NP solution was estimated. To estimate the occupation probability, we regarded a droplet dropped onto the chip as a half-sphere. A schematic of a droplet is shown in Fig. 7.

The radius of the half sphere for a droplet of 1 μL is 0.8 mm. Each chip contains 12 gaps, and these gaps exist in a 200 μm × 200 μm square area in the center of the chip, whose dimensions are 7 mm × 7 mm. When a droplet is dropped onto the center of a chip, the center of the droplet is the the 200 μm × 200 μm square area that contains all the gaps on the chip. This

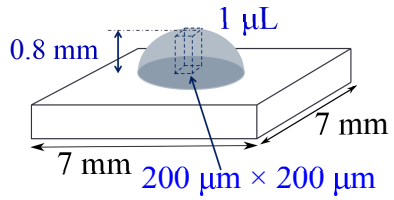

Fig. 7 A schematic of a droplet to estimate an occupation probability of the dispersed NPs. A droplet dropped onto the chip was regarded as a half-sphere. Radius of the half-sphere for a droplet of 1 μL is 0.8 mm. A bottom area of a square pillar enclosed by a dashed line is 200 μm × 200 μm and includes the all gaps on a chip.

square area is shown in Fig. 7 as the bottom layer of a square pillar enclosed by a dashed line. We assumed that NPs included in the square pillar moved down to this area during drying. The specific gravity of the citric acid gold colloidal solution (pH 6.4) was regarded as 1. The colloidal solution contained 70 ppm NPs with a diameter of 15 nm. This square pillar's bottom area was 200 μm × 200 μm and its height is 0.8 mm. The weight of gold included in the square pillar was 2×10^{-9} g, and the number of gold NPs with a of diameter of 15 nm in was 6×10^7. For gold NPs of 15 nm in diameter, GL_{H} and GL_{V} (Fig. 1) are 15 nm and 13 nm, respectively. The number of NPs needed to occupy the whole area of 200 μm × 200 μm on a triangular lattice is 2×10^8. Thus, the occupation probability for one drop is 0.3. Experimental connection probability values, $P_{C,\mathrm{E}}$, were calculated using the equation for each drop on each chip, $P_{C,\mathrm{E}} = N_{\mathrm{C}}/12$, where N_{C} is the number of gaps connected by NPs, and 12 is the total number of gaps on each chip.

In the experiments, after the NP solution was dropped onto the chips, the resistance between the S and D electrodes was measured, whereas that between the S and G electrodes was not measured. For comparison of the resistance measurement results, we calculated $P_{C(\mathrm{S-D})}$ using the following equation,

$$P_{C(\mathrm{S-D})} = P_{C(\mathrm{S-D\_(G)})} + P_{C(\mathrm{S-D-G})} \quad (1)$$

where $P_{C(\mathrm{S-D\_(G)})}$ and $P_{C(\mathrm{S-D-G})}$ are the P_C of $S-D\_(G)$ and that of $S-D-G$, respectively.

The designed values of 1000 nm for $L_{\mathrm{SD-G}}$ and 800 nm for W_{S} correspond to 76 and 62 grids, respectively, for a GL_{V} of 13 nm. The W_{G} of 66 grids used in the calculation corresponds to 990 nm for a GL_{H} of 15 nm. The designed gap distances of 100, 140, 200, and 300 nm on chips A, B, C, and D correspond to 6, 10, 14, and 20 grids, respectively. Because 100, 140, 200, and 300 nm gaps correspond to one-fourth the total number of gaps on Chip A, B, and C, $P_{C,\mathrm{TOTAL}}$ of S-D, $P_{C(\mathrm{S-D})\mathrm{TOTAL}}$ was calculated using the following equation,

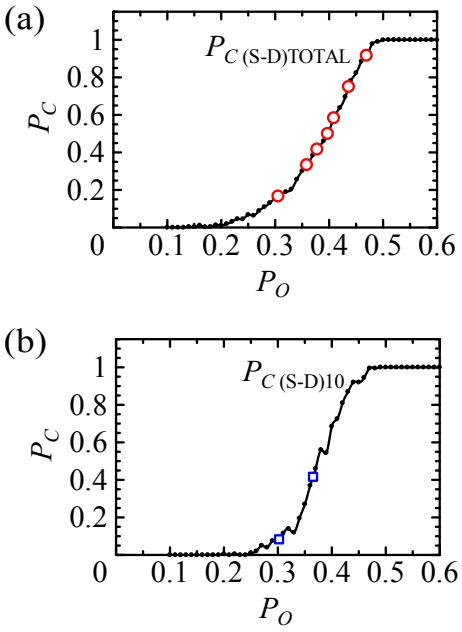

Fig. 8 $P_{C(\mathrm{S-D})}$-P_O curves. (a) For chip A, B, and C. (b) For chip D. $P_{C(\mathrm{S-D})\mathrm{TOTAL}}$ curve calculated by using Eq. 2. By plotting $P_{C,\mathrm{E}}$ on the curve, $P_{O,\mathrm{E}}$ is determined for each $P_{C,\mathrm{E}}$.

$$\begin{aligned} P_{C(\mathrm{S-D})\mathrm{TOTAL}}(P_O) = (&P_{C(\mathrm{S-D})6}(P_O) \\ &+P_{C(\mathrm{S-D})10}(P_O) + P_{C(\mathrm{S-D})14}(P_O) \\ &+P_{C(\mathrm{S-D})20}(P_O)) \times 0.25 \end{aligned} \quad (2)$$

where $P_{C(\mathrm{S-D})\mathrm{N}}(P_O)$ is $P_{C(\mathrm{S-D}))}$ for $Gap_{\mathrm{S-D}}$ of N grids at P_O.

If we assume that the NPs are fixed on the chip after the Mth drop and that NPs occupy vacancies with a probability of $P_{O,INCR}$ at the $(M+1)$-th drop, the occupation probability can be calculated using the following equations:

$$P_O(M+1) = P_O(M) + (1 - P_O(M)) \times P_{O,INCR} \quad (3)$$

$$P_{O,INIT} = P_O(1) \quad (4)$$

where $P_O(M+1)$ and $P_O(M)$ are the occupation probabilities at the $(M+1)$-th drop and at the Mth drop, respectively.

4 Results and Discussion

The $P_{C(\mathrm{S-D})\mathrm{TOTAL}}$ curve calculated using Eq. 2 is shown in Fig. 8.

By plotting $P_{C,\mathrm{E}}$ on the curve, we determined the occupation probability based on the results of the resistance measurements, $P_{O,\mathrm{E}}$ for each $P_{C,\mathrm{E}}$.

Table 2 Determined $P_{O,\mathrm{E}}$ for each $P_{C,\mathrm{E}}$ at the Mth drop. "*" indicates that the dropping of the NP solution was completed, and "-" indicates that the resistance was not measured. $P_{O,\mathrm{E}}$ was not determined for a $P_{C,\mathrm{E}}$ of 0 (shown as "***").

Chip	P	M						
		1	2	3	4	5	6	7
A	$P_{C,\mathrm{E}}$	0.33	0.58	0.58	0.92	*	*	*
	$P_{O,\mathrm{E}}$	0.36	0.41	0.41	0.47	*	*	*
B	$P_{C,\mathrm{E}}$	-	0	-	0.17	-	0.58	0.75
	$P_{O,\mathrm{E}}$	-	***	-	0.31	-	0.41	0.44
C	$P_{C,\mathrm{E}}$	0.50	0.42	0.50	0.17	0.58	*	*
	$P_{O,\mathrm{E}}$	0.40	0.38	0.40	0.31	0.41	*	*
D	$P_{C,\mathrm{E}}$	0.08	0.08	0.08	0.08	0.08	0.42	0.42
	$P_{O,\mathrm{E}}$	0.30	0.30	0.30	0.30	0.30	0.37	0.37

The $P_{C,\mathrm{E}}$ and the $P_{O,\mathrm{E}}$ at the Mth drop on chips A, B, C, and D are summarized in Table 2

, where "*" indicates that the dropping of the NP solution was completed, and "-" indicates that the resistance was not measured. $P_{O,\mathrm{E}}$ was not determined for a $P_{C,\mathrm{E}}$ of 0 (shown as "***") because P_O does not have a unique value for a $P_{C,\mathrm{E}}$ of 0 on the $P_{C(\mathrm{S-D})\mathrm{TOTAL}}$ curve shown in Fig. 8.

For fitting, a combination of $P_{O,INIT}$ and $P_{O,INCR}$ was found to minimize the sum of $(P_O(M)-P_{O,\mathrm{E}}(M))^2$, where $P_O(M)$ is defined in Eq. 3 and Eq. 4 and $P_{O,\mathrm{E}}(M)$ is $P_{O,\mathrm{E}}$ at the Mth drop.

The fitting results for chip A, B, and D are shown in Fig. 9 and the fitting parameters are summarized in Table 3. In the case of chip C, we could not fit the results because the P_C decreased at the fourth drop. We cannot explain this decrease of P_C on the basis of our two-dimensional percolation model. This decrease may be caused by the breaking of a connection between NPs, when the NP solution was added and some of the NPs changed their position.

Table 3 Table of fitting parameter.

Chip name	$P_{O,INIT}$	$P_{O,INCR}$
Chip A	0.36	0.055
Chip B	0.14	0.070
Chip D	0.29	0.015

The P_O for one drop was determined to be 0.3. P_O for the first drop, $P_{O,INIT}$ for the chips A, B, and D are 0.36, 0.14, and 0.29 respectively. These values are of the order as the occupation probability for a single drop: 0.3. However the $P_{O,INCR}$ values are 0.055, 0.070, and 0.015 for chips A, B, and D, respectively. These values are considerably smaller than 0.3, which may be caused by residual citric acid in vacancies preventing additional

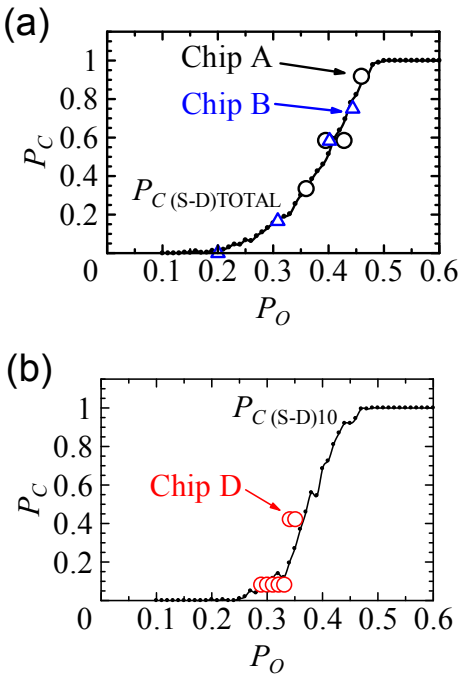

Fig. 9 Fitting results. Experimental results were fitted by using Eq. 3 and Eq. 4. Fitting parameters are listed in Table 3. (a) Results for chip A and B. $P_{C(\mathrm{S-D})\mathrm{TOTAL}}$ was calculated by using Eq. 2. (b) Results for chip D.

NPs from moving into the vacancies. A portion of the NPs may be covered with residual citric acid, which can function as a tunneling barrier.

For chips A and chip B, we collected $I-V$ curves at 77 K for 10 samples. The curves were strongly nonlinear: $G(0\mathrm{V})/G(20\mathrm{V}) < 0.02$, where $G(0\mathrm{V})$ and $G(20\mathrm{V})$ are the conductance at 0 V and at 20 V, respectively, in the case of the two samples. . However, we could not find specific evidence that these two samples worked as single-electron devices.

Fig. 10 shows $I_\mathrm{D} - V_\mathrm{DS}$ curves collected at 77 K and at a gate voltage, V_G, of 0 V for chip D. Fig. 10 (a) includes two $I_\mathrm{D}-V_\mathrm{DS}$ curves. These two curves were obtained by consecutive measurements. These two curves do not overlap in the voltage region beyond approximately 0.8 V. Enlarged views of the regions around 0 V and 0.8 V in Fig. 10 (a) are shown in sub-figures (b) and (c), respectively. There is a current suppressed region at approximately 0 V in Fig. 10 (a). In Fig. 10 (b), the first and second I_D values overlap; however in Fig. 10 (c) those I_D values do not overlap in the region beyond approximately 0.8 V. This mismatch may be caused by charging or by a positional shift of the NPs. Because of these current-suppression effects and the mismatch, we speculate that this sample functioned as a single-electron device. $I-V$ curves collected under various applied gate voltages may be discussed in elsewhere.

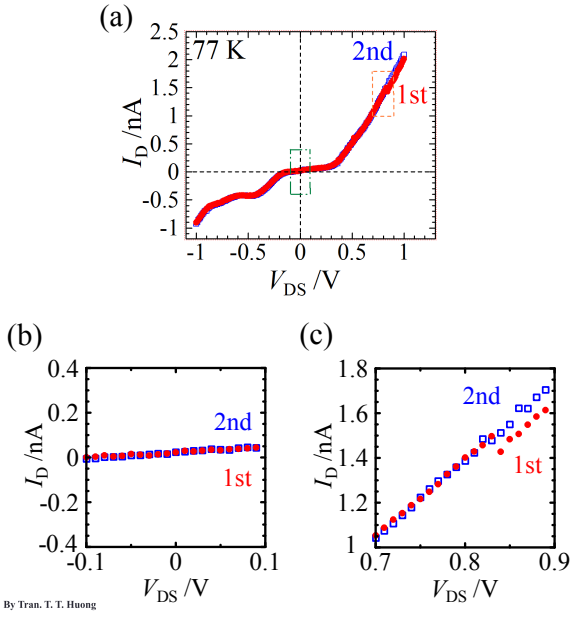

Fig. 10 $I_D - V_{DS}$ curves collected at 77 K and at a gate voltage, V_G, of 0 V for chip D. These curves were obtained by consecutive measurements. The first and second I_D are plotted as filled circle and open square, respectivly. (a) Whole view. (b) Enlarged view of the regions around 0 V enclosed by a dot-and-dash line in (a). (c) Enlarged view of the regions around 0.8 V enclosed by a dashed line in (a).

5 Conclusion

We have calculated the connection probability P_C between the S and D electrodes on the basis of the triangular lattice percolation model to investigate effects of varying the length between electrodes and the width of electrode for fabricating capacitively coupled single-electron transistors. Varying the gap length between the S and D electrodes and also that between the S and G electrodes was effective. Single-electron devices were fabricated via the dispersion of gold NPs. We dispersed the gold NPs by repeatedly dropping a gold NP solution onto a chip, followed by drying the chip. We measured the resistance between the S and D electrodes. To compare the calculated calculated results with the experimental results, we defined $P_{C,E}$ on the basis of resistance measurements and subsequently fitted the results to the calculated $P_{C,E}$ values. The P_O per drop was estimated to be 0.3 and was the same order for the first drop; however, the P_O was small after second drop. On the basis of $I_D - V_{DS}$ curves collected at 77 K, the current was suppressed at approximately 0 V.

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