Second Harmonic Treatment Technique for Bandwidth Enhancement of GaN HEMT Amplifier with Harmonic Reactive Terminations

Jun Enomoto, Ryo Ishikawa, *Member, IEEE,* Kazuhiko Honjo, *Fellow, IEEE*

***Abstract*—Source and load impedance conditions for second harmonics have a great influence on the efficiency of amplifiers. The bandwidth of high-efficiency operation is limited, since efficiency is drastically degraded due to a slight change in source-side second harmonic impedance from the optimum point. For this reason, to avoid steep efficiency degradation, a source-side second harmonic impedance control is introduced. In addition, a harmonic treatment network which reduces the influence on matching-network design is also described here. A fabricated GaN HEMT amplifier has achieved a maximum power-added efficiency (PAE) of 79% with a saturated output power of 48.0 dBm at 2.02 GHz. The amplifier has also achieved a high-efficiency characteristic of more than 70% PAE in the frequency range from 1.68 to 2.12 GHz.**

***Index Terms*—Power amplifier, high efficiency, GaN HEMT, harmonic reactive terminations.**

I. Introduction

Recent advanced wireless communication systems, such as LTE (long term evolution) and WiMax (worldwide interoperability for microwave access), require wider bandwidths due to the increasing transmission rate, in addition to the coverage of multiple frequency bands. Accordingly, microwave power amplifiers are required to be capable of wideband or multiband operation. In the meantime, high-efficiency operation remains an important requirement for microwave power amplifiers. To achieve high-efficiency operation, source and load impedances at higher harmonic frequencies including a fundamental frequency have to be properly treated.

Thus far, many different design approaches to achieve high-efficiency power amplifiers, such as class-F [1], [2], class-E [3], and harmonic reactive load [4], [5], have been reported. In practice, it is difficult to obtain high-efficiency in a wide frequency range for the class-F and class-E amplifiers, since these approaches require precise control for the optimum source and load impedances at harmonic frequencies. Whereas, the load harmonic impedance condition is looser for the harmonic reactive load type, which is theoretically arbitrary pure reactance [4]. However, even in this approach, source second harmonic impedance has a great effect on efficiency [6]–[11]. Efficiency has a steep characteristic due to the change in second harmonic impedance near the optimum point, hence, the bandwidth of high-efficiency becomes narrowed, though optimum high-efficiency is obtained at a single point of the designed frequency [5].

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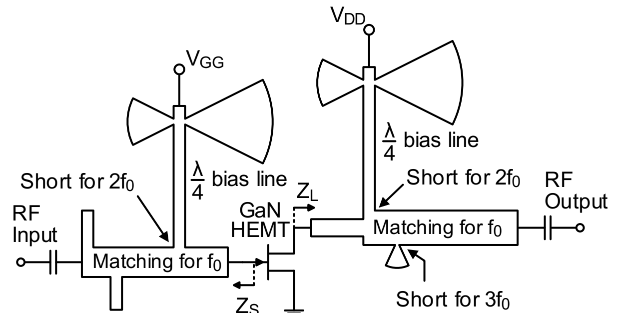


Fig. 1. Circuit configuration of designed GaN HEMT amplifier

In this work, a high-efficiency amplifier is designed based on the harmonic reactive termination approach [4], [5]. A circuit configuration of the designed amplifier is shown in Fig. 1. The second harmonic on the source-side and the second and third harmonics on the load-side were treated for this amplifier. The source impedance dependence of efficiency at the second harmonic frequency was investigated by source-pull simulations, and then the optimum condition for wideband high-efficiency is discussed. In the network design, harmonic treatment networks can be constructed by using quarter-wavelength open-ended stubs for the harmonics so that arbitrary reactance values can easily be obtained [12]. However, these networks affect the design of other harmonic treatment networks or a matching-network at the fundamental frequency. In this study, a second harmonic treatment network was successfully shared with a quarter-wavelength bias network to reduce the influence on the latter matching-network design.

II. Amplifier Design with Second Harmonic Control

The efficiency of an amplifier is expected to be maximized when power dissipation at a transistor is minimized. To reduce power dissipation, the load impedance condition has to be pure reactance at each higher harmonic frequency, and has to be an appropriate condition to balance with the supplied dc power at a fundamental frequency. In addition, the reactance values for the harmonics have to be optimized to shape the voltage and current waveforms at the transistor so as to minimize the overlap between the voltage and current waveforms, which produces power dissipation. To achieve maximum high-

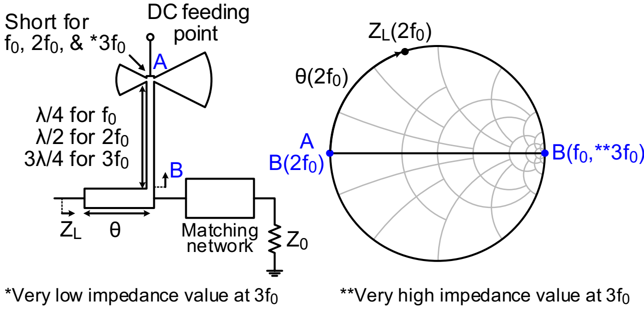
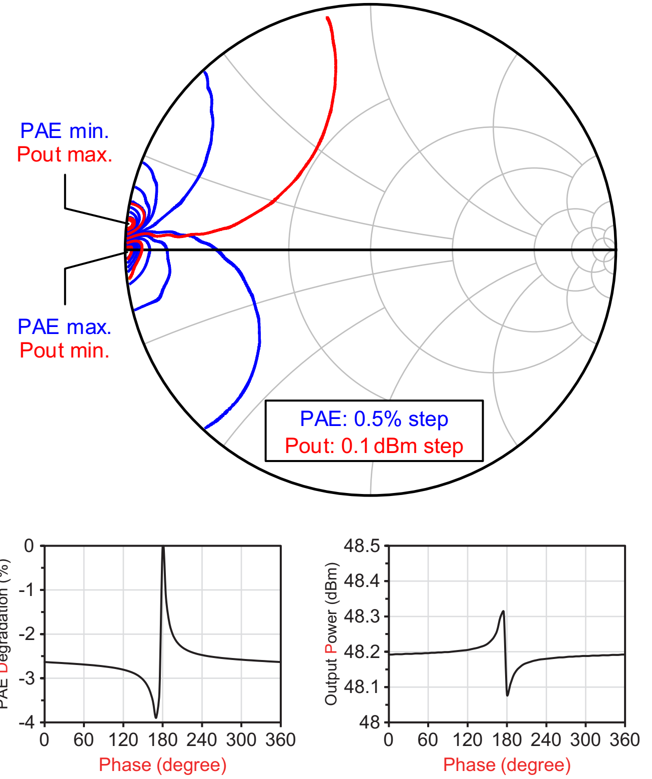


Fig. 2. Schematic diagram of bias network with second harmonic treatment

efficiency operation, source-side harmonic impedance conditions have to be adjusted in addition to those on the load-side. Especially, the source-side impedance at the second harmonic has a remarkable effect on efficiency [6]–[11].

A high-efficiency GaN HEMT amplifier with harmonic reactive termination was designed at $f_0 = 2.1\,\mathrm{GHz}$. Source impedance at the second harmonic frequency and load impedance at the second and third harmonic frequencies were taken into account to achieve higher efficiency operation. All designs and simulations were performed on Keysight ADS software. A 70 W-class bare die GaN HEMT (Cree CGHV1J070D) was used for this amplifier and its large-signal model provided by the manufacturer was used for the design. The device was biased with a drain supply voltage of 40 V and a gate supply voltage of $-2.8\,\mathrm{V}$ (class-B operation). The targeted source- and load-side impedance conditions were set to the optimum conditions based on source- and load-pull simulation results.

For the design of harmonic reactive load amplifiers, the impedance for the harmonics can be adjusted regardless of the latter matching network by using a quarter-wavelength open-ended stub for a harmonic frequency. On the other hand, the configuration of the harmonic treatment network affects the latter matching-network design, though the desired impedance for the harmonic is obtained [13]. A quarter-wavelength bias network with second harmonic treatment has been introduced to reduce the influence on the matching-network design, as described in Fig. 2. The bias network consists of a transmission line as a reactance adjustment line, a quarter-wavelength line for f_0 and quarter-wavelength open-ended stubs for f_0 and $2f_0$. Both of the open-ended stubs are connected to the end of the bias line (**A**). For $2f_0$, the input impedance of the bias network (**B**) becomes zero, since **A** is shorted and the bias line is a half-wavelength. Then, Z_L can reach the desired value of pure reactance by adjusting the electrical length of the reactance adjustment line θ. This network configuration is not to be seen for f_0, therefore, it does not disturb the latter matching-network design. In addition, **B** achieves a very high impedance value for $3f_0$, since **A** is a very low impedance value. Therefore, a third harmonic treatment stub can be optimally connected while being scarcely affected by the configuration of the bias network. This stub barely affects fundamental matching, since its electrical length is short at the fundamental frequency. Generally, the matching network of a single-band amplifier can consist of a transmission line. As a result, the reactance adjustment line can be shared with the matching network.



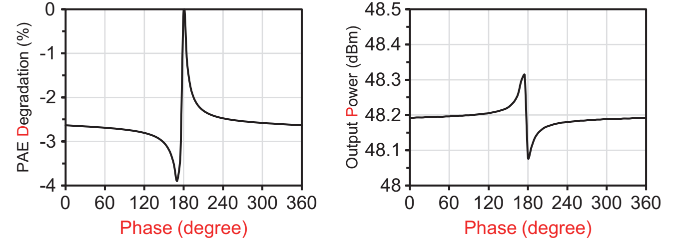
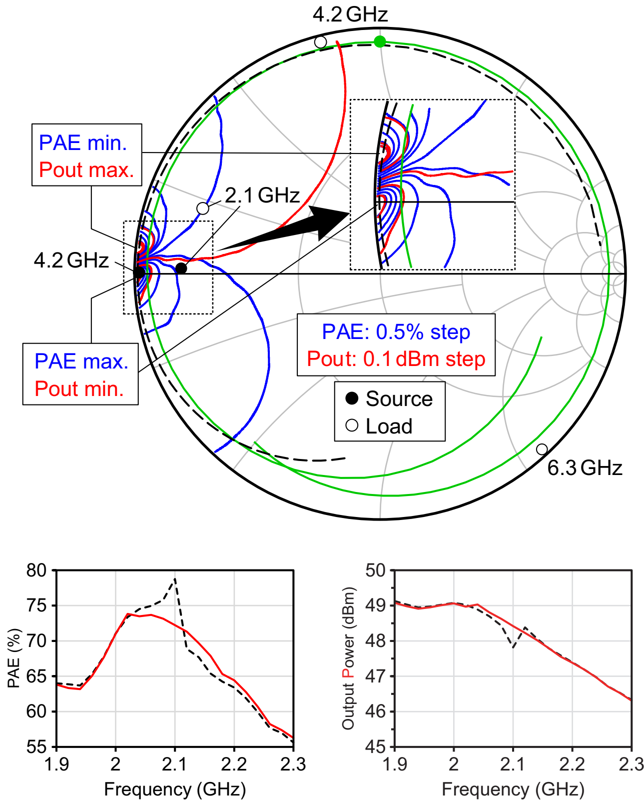


Fig. 3. Source-pull simulation result and PAE degradation from the maximum and output power versus the phase of source reflection coefficient at $2f_0$

To maximize the efficiency of an amplifier, the source-side second harmonic impedance has to be adjusted, as discussed above. However, it has been reported that the bandwidth of high-efficiency operation is limited due to a slight change of source-side second harmonic impedance from the optimum point [5]. For the device used in this work, a steep power-added efficiency (PAE) characteristic due to a change in the phase of the reflection coefficient has also been observed by a second harmonic source-pull simulation, as shown in Fig. 3. Moreover, a steep gain characteristic has also been observed. The amplitude of the reflection coefficient $|\Gamma|$ is fixed to 0.95 in the lower graphs. It is found that the valley and the peak point of efficiency and output power are located close to each other. Hence, in the optimum case, the amplifier has a sharp frequency characteristic of efficiency and gain, though high-efficiency operation is achieved at a single point of the designed frequency. The bandwidth of high-efficiency operation becomes narrowed.

Fig. 4 shows a comparison of impedance variation and simulated PAE and output power between the optimum case and a shifted case of targeted source second harmonic reactance. Filled and unfilled circles in the Smith chart represent source and load impedance conditions at 2.1 GHz, respectively. The network configurations described in Fig. 1 are used in both cases for the simulation, and therefore the impedance values for the other frequencies are almost identical. The load-side



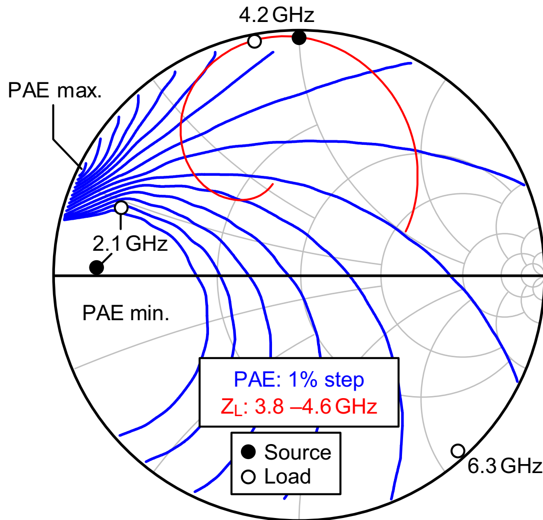


Fig. 4. Comparison of impedance variation and simulated PAE and output power between the optimum case (dashed line) and shifted case (solid line) of targeted source second harmonic reactance

Fig. 5. Second harmonic load-pull simulation result at 2.1 GHz (blue lines) and simulated impedance variation of output network (red line)

network is designed to eliminate a drastic change in efficiency, as shown in Fig. 5. Nevertheless, in the optimum case, a much higher PAE than that in the shifted case is achieved at 2.1 GHz, but a slight variation of 20 MHz reduced the PAE by 9%. A dip in output power has also been observed. As a result, PAEs of the shifted case are higher than those of the optimum case in upper-side frequencies. Accordingly, the frequency characteristic of efficiency is expanded by the shift of targeted source second harmonic reactance. Moreover, the frequency characteristic of the output power is flattened. To achieve a wider frequency characteristic of efficiency and a flat frequency characteristic of output power, the targeted source second harmonic reactance has to be shifted from the optimum at the sacrifice of maximum high-efficiency operation.

TABLE I
TARGETED SOURCE- AND LOAD-SIDE IMPEDANCES

Frequency	$Z_S(\Omega)$	$Z_L(\Omega)$
f_0	$4 + j1$	$5 + j9$
$2f_0$	$0.1 + j50$	$0.1 + j36$
$3f_0$	N/A	$0.1 - j110$

To extend the frequency characteristic of efficiency, the second harmonic on the source-side and the second and third harmonics on the load-side were treated while avoiding a steep efficiency degradation. The targeted source- and load-side impedance conditions are listed in Table I. The input and output networks were designed so that the impedance conditions of the targets would be fulfilled. Bonding wires for connection of the transistor and networks, and parasitic components in the chip dc block capacitors were taken into account for the design.

The input and output networks were designed based on the proposed approach. The third harmonic was treated by a quarter-wavelength open-ended stub in the output network. The layouts of both networks were analyzed and optimized by using electromagnetic (EM) simulations.

III. Fabrication and Measurement of GaN HEMT Amplifier

The designed high-efficiency GaN HEMT amplifier at 2.1 GHz was fabricated, as shown in Fig. 6. Both the input and output networks were fabricated on resin substrates (Panasonic Megtron7) with a board thickness of 0.75 mm and $\varepsilon_r = 3.37$. The size of the amplifier module is 64 mm $\times$ 50 mm excluding protrusions. Feed-through capacitors are mounted at the gate and drain bias points. A series ferrite inductor at the gate bias point and a series parallel-RC network on the RF input

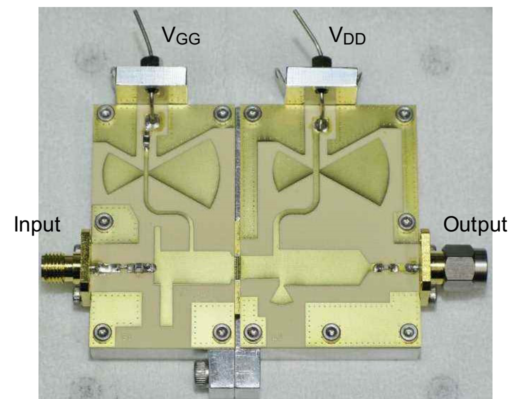


Fig. 6. Photograph of the fabricated GaN HEMT amplifier

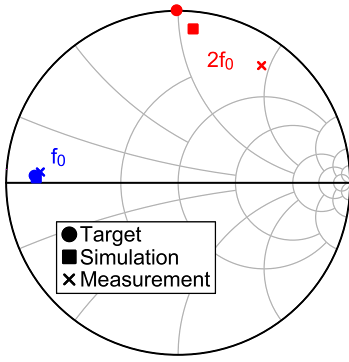


Fig. 7. Comparison between targeted, simulated and measured impedance conditions for the input networks at $f_0 = 2.1\,\mathrm{GHz}$

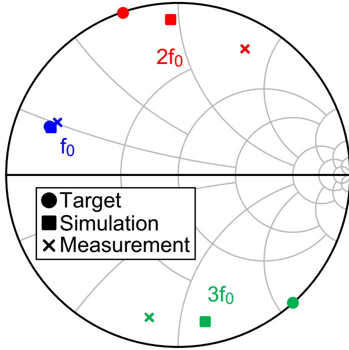


Fig. 8. Comparison between targeted, simulated and measured impedance conditions for the output networks at $f_0 = 2.1\,\mathrm{GHz}$

line were additionally mounted to maintain the stability of the amplifier in measurement.

The impedance conditions for the fabricated input and output networks were measured by a vector network analyzer (Keysight PNA-X) and compared with targets and simulation results. These results are shown in Figs. 7 and 8. The measured and simulated results and targets were almost identical at a fundamental frequency of 2.1 GHz. For the higher harmonic frequencies, the measured impedances deviated clockwise. That can be caused by dispersion in the relative dielectric constant of the resin substrate.

Fig. 9 shows the measured circuit loss of the output network, which is calculated using the following formula:

$$Loss = 10 \log \frac{1 - |S_{11}|^2}{|S_{21}|^2} \text{ dB}. \tag{1}$$

Note that Ports 1 and 2 are provided at the transistor-side end and the load-side end of the output network, respectively. The measured circuit loss was 0.36 dB at 2.1 GHz and was stable over a wide frequency range. Due to underestimated dielectric loss in simulation, the measured loss is greater than the simulated loss. The measured value does not greatly reduce the amplifier's efficiency.

Performance measurements of the fabricated GaN HEMT amplifier were performed under pulsed operation (1 ms with a 3% duty cycle) while gate and drain bias voltages were constantly supplied, in order to suppress heating without influence on RF characteristics. The bias conditions were set to the same values as the designed ones.

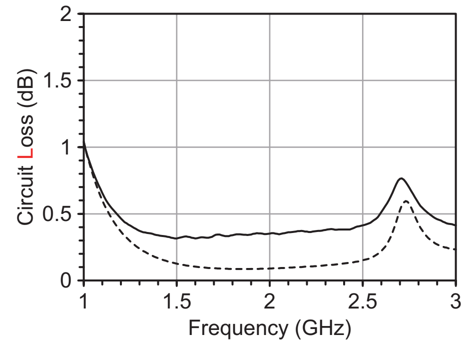


Fig. 9. Measured (solid line) and simulated (dashed line) circuit loss of the output network

A maximum PAE of 79%, a drain efficiency of 84% and a saturated power of 48.0 dBm were obtained at 2.02 GHz for the measurements. An associated gain of 12.4 dB was obtained. The measured results for output power, gain, and efficiency versus input power characteristics for the fabricated GaN HEMT amplifier at 2.02 GHz are shown in Fig. 10.

The measured results for the frequency characteristics of maximum output power, and gain, PAE and drain efficiency associated with output power for the fabricated GaN HEMT amplifier are shown in Fig. 11. Wideband high-efficiency characteristics of more than 70% PAE and more than 77% drain efficiency were obtained in the frequency range from 1.68 to 2.12 GHz (440 MHz bandwidth). The maximum output power and gain varied from 46.9 to 50.0 dBm and from 10.2 to 11.9 dB, respectively, in the same frequency range. The downward shift in the frequency of the peak PAE is due to the clockwise impedance deviations from the designed values, as described in Figs. 7 and 8. A high-efficiency characteristic was obtained even below 2 GHz, since the harmonic impedance loci deviated inward on the Smith chart by the influence of the circuit loss so as to avoid a steep efficiency degradation.

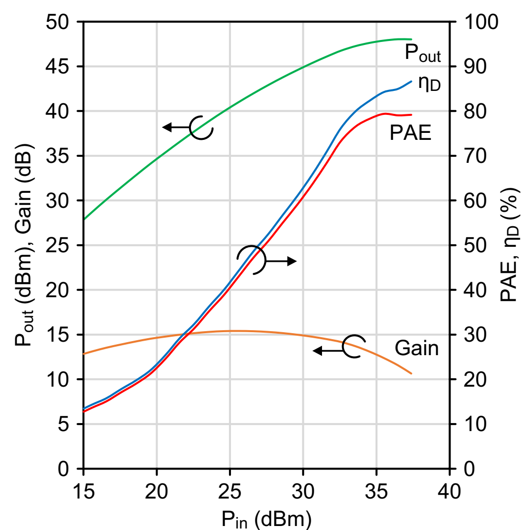


Fig. 10. Pulsed measurement results for output power, gain, PAE and drain efficiency (η_D) versus input power characteristics for the fabricated GaN HEMT amplifier at 2.02 GHz

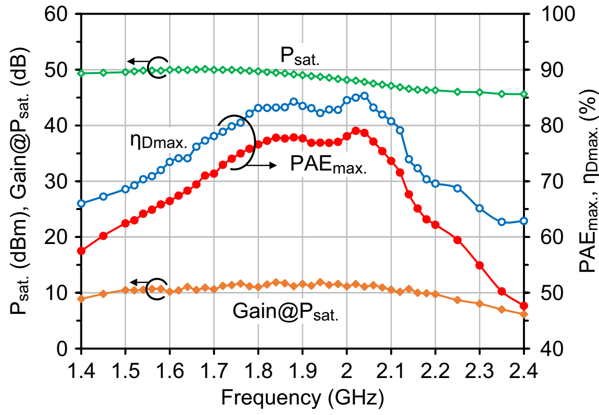


Fig. 11. Pulsed measurement results for frequency characteristics of maximum output power, and gain, PAE and η_D associated with output power for the fabricated GaN HEMT amplifier

The proposed amplifier has transmission zeroes at the second and third harmonic frequencies achieved by the harmonic treatment network on the load-side, and hence it can be expected to suppress the output level of the harmonics. Fig. 12 shows the measured power output spectrum of the fabricated amplifier. A significant level of the second harmonic has been observed, unlike the expected result of the third one. That is possibly due to the loss of the bias network in the output network, which is also used for second harmonic treatment. The fabricated amplifier was also measured for a W-CDMA (wideband code division multiple access) 3GPP (third generation partnership project) signal. The bias conditions were set to the same values as the designed ones. Fig. 13 shows the output spectrum for the modulated input signal with a center frequency of 2.02 GHz. The input power level was set to 23 dBm, which was roughly a 10-dB back-off operation condition. Although the proposed amplifier design was not applied any optimization for the performance under modulated operations, it has a moderate distortion characteristic, which implies the capability of good distortion performance achieved by the further improvement of the design.

The performance of the proposed amplifier compared with that of previously reported harmonic-controlled GaN HEMT amplifiers is summarized in Table II. The proposed amplifier has a broadband high-efficiency performance comparable to

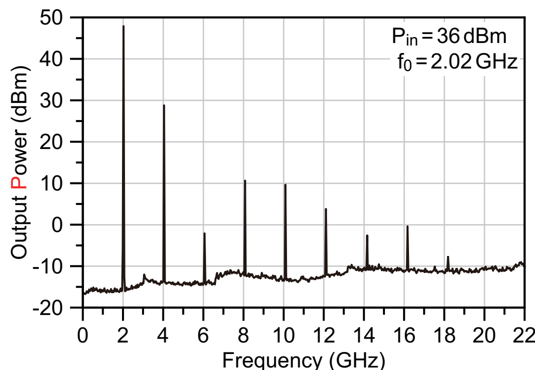


Fig. 12. Measured power output spectrum of the amplifier

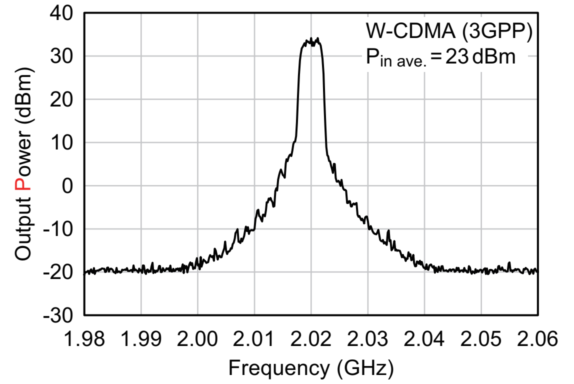


Fig. 13. Measured output spectrum of the amplifier for a W-CDMA 3GPP signal centered at 2.02 GHz

TABLE II
PERFORMANCE COMPARISON WITH OTHER HARMONIC-CONTROLLED GAN HEMT AMPLIFIERS

Ref.	Type	P_{out} (W)	Frequency (GHz)	Bandwidth (MHz)	PAE (%)	η_D (%)
[14]	class-E	12.7	2.0–2.5	500	71–74	74–77.3
[15]	class-E	20	1.2–2.0	800	N/A	80–89
[16]	class-F^{-1}	100	2.5–2.8	300	74.5	61–76.1
[17]	class-F	17.4	1.4–2.5	1100	N/A	73–88.6
[18]	class-BJ	28	1.7–2.8	1100	52–59	58–66
[19]	class-EF	15.5	1.42–1.72	300	62–81	65–85
[20]	class-F^{-1}	19.5	1.7–2.8	1100	N/A	60.3–80.4
This work	Harmonic reactive termination	100	1.68-2.12	440	70–79	77–84

the reported 10 W- to 20 W-class amplifiers [14], [15], [17]-[20]. Though fewer results of 100 W-class broadband high-efficiency GaN HEMT amplifiers have been reported, the proposed amplifier exhibited the best broadband high-efficiency performance among the amplifiers of the same power class.

IV. CONCLUSION

This paper presented the design, fabrication and measurement of a high-efficiency GaN HEMT amplifier with harmonic reactive terminations. A design strategy for source-side second harmonic impedance control to avoid a steep efficiency degradation has been described. This strategy has also avoided the appearance of a gain dip. The fabricated GaN HEMT amplifier achieved a maximum PAE of 79% with a saturated output power of 48.0 dBm at 2.02 GHz. High-efficiency characteristics of more than 70% PAE and more than 77% drain efficiency were obtained in the frequency range from 1.68 to 2.12 GHz.

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