Enhanced Nonlinear Electric Properties and Applications Based on the Coulomb Blockade Phenomena in Arrays of Small Tunnel Junctions

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和文概要

この論文は，単一電子論理デバイスの非線形特性の強化，および単一電子デバイス作製プロセスの開発を目的とするものである。

第一の目的に対しては，単一電子 4 接合インバータや単一電子 NAND ゲート等の単一電子論理ゲートの非線形特性を数値計算手法により改善した。連続的な入力信号に対して，単一電子 4 接合インバータや単一電子 NAND ゲートは，高出力レベルと低出力レベルの間の遷移が緩やかかつ連続的であり，これら遷移領域での出力状態決定が曖昧になる。この欠点を解消するため，入力端子と主たるデバイス（単一電子論理デバイス）の間に単一電子入力離散化器を付加して，入出力特性のスイッチングを急峻にした。入力離散化器では，連続的な入力信号が離散的な中間信号に変換され，それが主たるデバイスへの入力となる。入力離散化器のパラメータを，各接合におけるクーロン閉塞条件を基に設計した。モンテカルロ数値シミュレーションプログラム SIMON を用いて，設計した閾値での急峻なスイッチングを確認した。また，入力離散化器を主たるデバイスの入力端子に接続することで，主たるデバイスのスイッチングが急峻なものとなった。入力離散化器を付加した単一電子 4 接合インバータの遷移幅は，単一電子 4 接合インバータ単体のそれの 1.1% にまで減少した。また，単一電子 NAND ゲートの 2 つの入力端子それぞれに入力離散化器を付加した場合，単一電子 NAND ゲート単体と比較して，遷移幅が 33% に減少した。一方，単一電子 4 接合インバータに 2 個直列接続された入力離散化器を付加することで，ヒステリシス・インバータ特性が得られた。この 2 入力離散化器付き単一電子 4 接合インバータでは，理想的なヒステリシス・インバータモデルと同様に，確率共鳴現象が強化されることが示された。

第二の目的に対しては，単一電子デバイスを金ナノ粒子を用いて実現する新たなプロセスを開発した。まず，ドレイン，ソース，ゲートの各電極を，電子ビームリソグラフィと蒸着法によって作製した。ドレインとソース電極間のギャップを広く（$\geq$ 200 nm）することで，作製プロセスにおける技術的困難さを低減した。電極作製後，金ナノ粒子溶液を滴下することで，微小トンネル接合配列を形成した。77 K の温度にて，容量結合ゲート型，および抵抗結合ゲート型の単一電子トランジスタに似た特性が確認された。さらに，室温（287 K）においても，電気的特性上にクーロン閉塞が現れ，また，ゲート電圧を印加することによってクーロン閉塞領域が変調された。

Abstract

This thesis aims to enhance nonlinear characteristics of single-electron (SE) logic devices and fabricate SE devices.

For the first main goal, the nonlinear characteristics of SE logic gates including SE four-junction inverter (SE FJI) and SE NAND gates were improved by using the numerical method. With a continuous input signal, the SE FJI and SE NAND gates have a disadvantage of gradual switches between high and low output levels, resulting in unclear decisions about output states in the transition region. To overcome this disadvantage, the switching was enhanced to become sharp by adding an SE input discretizer (ID) between an input terminal and a main device (SE logic device). The ID discretizes the continuous input signal into a discrete intermediate signal which is then forwarded into the main device. Parameters of the ID were calculated from the conditions of the Coulomb blockade (CB) phenomena and confirmed from Monte-Carlo simulation using SIMON program to achieve the sharp switching at the designed threshold voltage. On the one hand, the addition of one ID to each input of SE logic device exhibited the sharp switching. Namely, an SE FJI with an ID (ID-FJI) achieved the sharp switching and its unclear region was reduced to 0.011 times in comparison with the solo FJI. An SE NAND gate with two separate IDs (ID-NAND) exhibited the sharp switches and its unclear regions were decreased to 0.33 times in comparison with the solo NAND gate. On the other hand, the addition of two serially-cascaded IDs to the SE FJI (2ID-FJI) formed a hysteretic inverter. In addition, stochastic resonance was enhanced remarkably by using the 2ID-FJI, which was equivalent to the use of an ideal hysteretic inverter.

For the second main goal, SE devices were realized by using gold nanoparitcles (Au NPs). Drain, source, and gate electrodes were fabricated by combining standard electron beam lithography (EBL) and evaporation techniques. The technical difficulty in the fabrication process was reduced by forming the

wide ($\geq$ 200 nm) gap between the drain and source electrodes. After that, arrays of small tunnel junctions were formed by dropping solutions of Au NPs. Characteristics like capacitively-coupled single-electron transistor (C-SET) and resistively-coupled SET (R-SET) were confirmed at 77 K. Moreover, the CB gap was not only observed but also modulated by applying the gate voltage at room temperature (287 K).

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Chapter 1

Introduction

1.1 Background

1.1.1 The development trend from conventional semiconductor devices to single-electron devices

The trend improving the performance of integrated circuits (ICs) has gained great achievements since 1970s [1]. The ICs have had lower cost, higher speed, and ability of processing multiple tasks simultaneously. In 1965, G. Moore presented an observation about the scaling trend of ICs. The Moore's Law shows that a new technology generation at which the size of the circuit is reduced by half is introduced every 18 or 24 months [2]. On the other hand, the International Technology Roadmap for Semiconductors (ITRS) provides a guidance to transform this observation into reality. The ITRS indentifies the requirements, challenges, and possible solutions for semiconductor researches and industry [3].

Among semiconductor devices, MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is the most prevalent device applied in ICs. The MOSFET device has four terminals including source, drain, gate, and body (substrate). There are two types of MOSFET including N-channel MOSFET (N-MOSFET) and P-channel MOSFET (P-MOSFET). The difference between structures of N-MOSFET and P-MOSFET is the type of semiconductor (N-type or P-type)

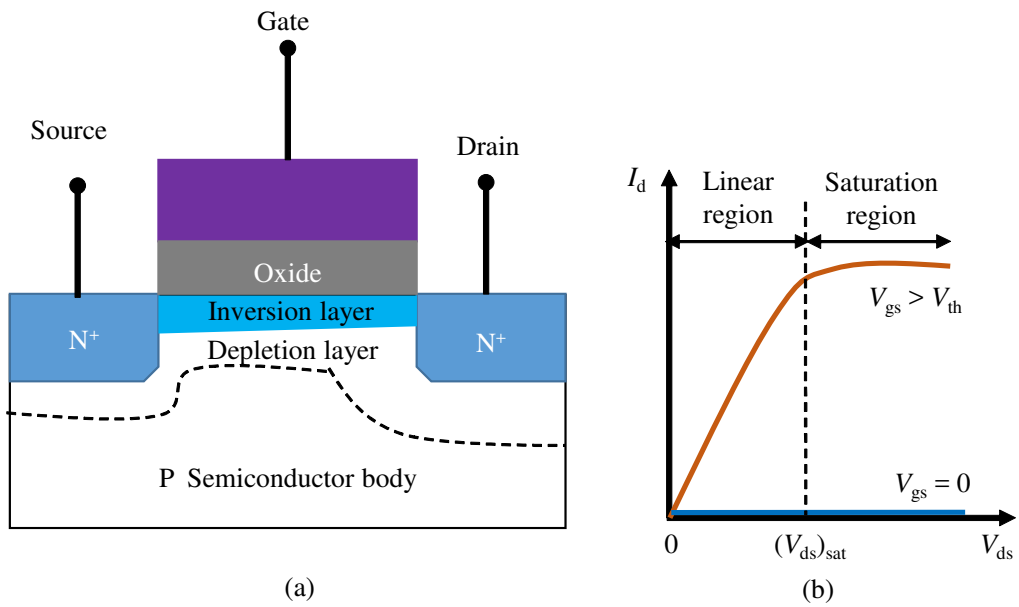


Figure 1.1: a) Basic MOSFET configuration. b) Drain current I_d versus drain-source voltage V_{ds} of the MOSFET.

used for source, drain, and body electrodes. In the N-type semiconductor, the number of electrons is more than the holes whereas, in the P-type semiconductor, the number of holes is more than the electrons. For the N-MOSFET, the source and drain electrodes are N^+ regions and the body is a P region. For the P-MOSFET, the source and drain electrodes are P^+ regions and the body is an N region. A basic configuration and electrical characterisics of a classical N-channel MOSFET are illustrated in Fig. 1.1 [4]. By applying the positive gate-body voltage, distribution of electrons and holes in the body changes, resulting in an inversion layer and a depletion layer between the source and drain electrodes. The inversion layer containing high density of electrons plays the role of a conductive channel where electrons can flow from the source to drain electrode. When gate-source voltage V_{gs} is smaller than a threshold voltage V_{th}, the transistor is switched off. However, there is still a leakage current I_{leak} flowing between the drain and source electrodes, which is called a substhreshold current. The substhreshold current contributes mainly to the

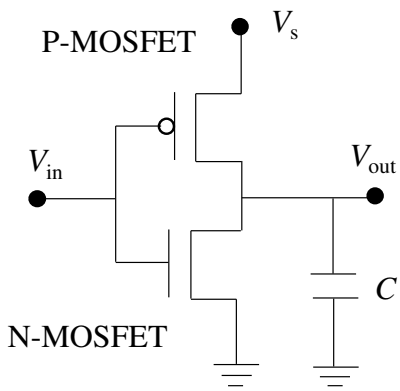


Figure 1.2: Configuration of a CMOS inverter.

off-state current I_{off} of the MOSFET [5]. When $V_{gs} > V_{\text{th}}$, the transistor turns on (Fig. 1.1(b)). In the case of $V_{gs} > V_{\text{th}}$, when drain-source voltage V_{ds} is less than saturation drain-source voltage $(V_{ds})_{\text{sat}}$, $V_{ds} < (V_{ds})_{\text{sat}}$, the MOSFET operates in a linear region; when V_{ds} is larger than $(V_{ds})_{\text{sat}}$, $V_{ds} \geq (V_{ds})_{\text{sat}}$, the MOSFET operates in a saturation region.

Since the MOSFET has the oxide layer between the gate and body electrodes, it has high input resistance resulting in a low input power consumption. Therefore, semiconductor academia and industry has concentrated on developing ICs on the basis of MOSFET [5]. The method of the improvement of ICs has been the MOSFET scaling. Two main objectives of the MOSFET scaling are to increase density and speed of ICs [6]. A reduction in the size can increase the density of transistors on a chip. In addition, the speed of circuit can be increased by reducing the size of the MOSFETs. For instance, we consider the propagation delay of a CMOS inverter composed of a P-MOSFET and an N-MOSFET (Fig. 1.2). The propagation delay τ_d is the time delay for a signal to propagate from the input to the output [4]. According to Ref. [4], τ_d is proportional to CV_s ($\tau_d \propto CV_s$), in which C is the total capacitance connected to the output of the inverter, V_s is the supply voltage. When the size of the device reduces, the capacitances also reduces [5]. Then, the propagation delay decreases, resulting in the rise of the speed of the circuit.

For the conventional MOSFET which has the metal gate electrode, the oxide layer made of SiO_2, and the strucutre as shown in Fig. 1.1, the scaling method has been associated with reducing dimensions of the MOSFET. The reduced dimensions of the MOSFET have included the channel length, oxide thickness, and the depletion layer width [2]. However, one of the serious problems of this method is the short-channel effects. When the MOSFET has the channel length on the same order as the depletion region width of the source and drain junctions, it is called a short-channel device [7]. The short-channel effect causes a reduction ΔV_{th} of the threshold voltage [5],

$$\Delta V_{\text{th}} \propto \exp(-L/l_d), \tag{1.1}$$

in which, L is the channel length; l_d is the characteristics length ($l_d \propto (T_{\text{ox}})^{1/3}$, T_{ox} is the thickness of the oxide layer). For instance, the device with 0.25-μm channel length has V_{th} of 0.7 V, whereas the device with 0.1-μm channel length has V_{th} of $0.33-0.40$ V [2]. Otherwise, $I_{\text{leak}} \propto \exp(\text{-}V_{\text{th}})$ [5]. Consequently, I_{leak} and also I_{off} increase. On the other hand, the static power consumption P_{static} which is consumed in the static (standby) mode of the device is calculated as [5],

$$P_{\text{static}} = V_s I_{\text{off}}. \tag{1.2}$$

The Eq. (1.2) indicates that the increase of the off current causes the rise of the static power consumption. For example, I_{off} is 100 nA per transistor, then a chip contains 100 million transistors could consume 10 A in the standby mode. For the high-speed device whose the channel length is reduced heavily, this problem becomes more serious. The short-channel effect can be decreased by forming the thin oxide layer (small T_{ox}) which helps to decrease ΔV_{th} in Eq. (1.1) [5]. However, when the SiO_2 layer is thinner than 1.5 nm, the tunneling leakage current through the oxide layer become significant [5]. For example, the MOSFET with the 1.2-nm-thick SiO_2 layer leaks 10^3 A/cm^2.

To solve the problem in the MOSFET scaling, two ways have been applied. One way has been the improvement of the semiconductor technology by in-

troducing nonclassical CMOS structures [8]. The nonclassical CMOS has the enhancement in the material and structure of the MOSFET. An example of the material enhancement is that they have used the high dielectric material for the oxide layer. The high dielectric material such as HfO_2 with the relative dielectric constant of 24 which is six times larger than SiO_2 can protest against the tunneling leakage current [5]. Consequently, the very thin oxide layer can be applied for the MOSFET to reduce the short-channel effect. In addition, the new structures like untra-thin-body (UTB) and multigate MOSFET have been introduced to increase the controlling ability of the gate in the off state [8]. Until now, this way has achieved remarkable advances. For example, they could fabricate 14-nm transistor in 2014 and the number of transistors could increase to 25 million per mm^2 in 2016 [9, 10].

Another way is the development of nanodevices to replace MOSFET, such as single-electron (SE) devices [11]. SE devices have two important advantages as follows [12]. With small physical sizes on the order of nanometers, SE devices have the possibility to make ultralarge scale integration. On the other hand, the total power consumption of a device is sum of static and dynamic powers which are dissipated in the off and on modes, respectively. The dynamic power is the main contributor in the total consumption power. Because SE devices can control the electric charge at the level of one electron, there are only a few electrons used for a basic operation resulting in ultralow dynamic power consumption. The advantages of SE devices make them prospective for the future of ICs.

In the field of single electronics, the most important element is a tunnel junction. The tunnel junctions have been realized by using a variety of materials and technologies such as metal-insulator-metal, silicon nanowires, GaAs quantum dots, carbon nanotubes, aluminium nanodots, and gold nanoparticles. The realized tunnel capacitances on the order of 10^{-16} F limits the operation temperature to 1 K [13]. Recently, there have been experiments exhibiting the tunnel capacitances in the range of $10^{-18} - 10^{-20}$ F, resulting in the operation at liquid nitrogen temperature and room temperature [14–17]. How-

ever, these devices have required the high complexity in the fabrication and the difficulty for application in large-scale integrated circuits. Therefore, one of the great expectations in the future is the fabrication of room-temperature SE devices and then the realization of SE integrated circuits.

1.1.2 Early researches on single-electron devices

SE effects were investigated in the period from 1950s to 1970s. In 1951, Gorter explained the increase of resistance of the thin granular metal films in terms of the necessary energy for tranfering electron between the grains [18]. One decade later, Neugebauer mentioned the activation energy required for electrons travelling between two islands, where the activation energy was associated to the charging energy of a single electron [19]. Systems including thin and thick insulators sandwiched between metal electrodes were evaluated by measuring their resistances and $C - V$ (capacitance-voltage) characteristics, where the thin and thick insulators were used for tunnel barriers and capacitor dielectrics [20], [21]. Until 1970s, knowledge about SE effects in granular metal films had been developed well with the addtion of quantitative analyses.

Since 1980s, researches in the field of single electronics have been developed dramatically. Behavior of a single tunnel junction was predicted by Likharev and his co-workers in the mid-1980's [22], [23]. By late 1980s, characteristic like a Coulomb staircase was observed in the devices whose island and tunnel junctions were well defined. The first SE transistor (SET) was demonstrated by Fulton and Dolan [13]. They fabricated $Al/Al_2O_3/Al$ tunnel junctions on a SiO_2/Si substrate. The 14-nm-thick island was made of an Al film while the tunnel barriers were realized by the oxidized Al surface. The source and drain electrodes were made of Al whereas Si substrate worked as the gate electrode. The device measured at 1.1 K showed 1-mV-wide Coulomb gap in current-voltage ($I - V$) characteristics and Coulomb oscillations by applying the gate voltage. From the viewpoint not of physical research but of real usage, operation temperature of these devices were extremely low and not suitable for many practical applications. Therefore, operation of SE devices at higher

temperatures has been an important objective. The first device exhibiting Coulomb staircase at room temperature was realized using a gold nanoparticle and a scanning-tunneling microscopy technique [24].

In the analog applications, the possible applications of SE devices have been reported such as the supersensitivity electrometry, the SE spectroscopy, the dc current standards, the temperature standards, the resistance standards, and the detection of infrared radiation [25]. For the digital applications, several applications have been demonstrated such as SE logic circuits including voltage state logics where logical ("1" and "0") bits are represented by high/low dc voltage levels and charge state logics where the logical bits are presented by the presence/absence of single electrons in conducting islands, SE memories, and electrostatic data storage using SETs and MOSFETs [25]. However, there are two big problems limiting digital applications. The first one is the fabrication of room-temperature SE devices. The number of reports on the fabricated room-temperature SE devices has still been limited. The second one is the randomness of the background charge which shifts the operation point of SE devices composed of capacitively-coupled SETs (C-SETs). There are several solutions for the second problem, for example the use of extremely pure materials, resistively-coupled SET (R-SET) devices, and C-SET devices working independently with the background charge. The solutions for these problems are necessary for realizing the SE integrated circuits in the future.

1.1.3 Orthodox theory

The orthodox theory [25] plays an important role in the field of SE devices. This theory is on the basis of three major assumptions as follows [25]. Firstly, the electron energy quantization in the conductors is ignored. In other words, the electron energy spectrum is considered as continuous. The condition required for this assumption is $E_k \ll k_B T$, in which E_k, k_B, and T are the quantum kinetic energy of electrons, the Boltzman constant, and the electron temperature, respectively. Secondly, time for tunneling through the barrier is assumed to be negligible in comparison with other time scales (in fact, this

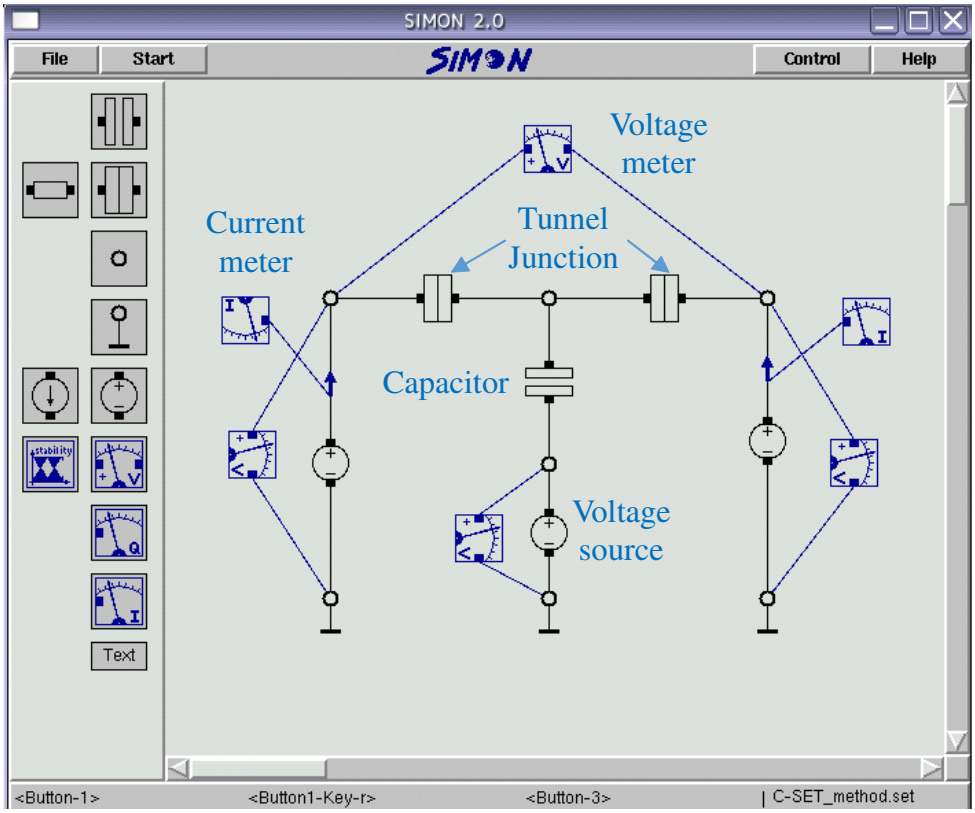
time is on the order of 10^{-15} s). Finally, no cotunneling processes where several electrons simultaneously tunnel through different barries are assumed. This assumption is satisfied if all tunnel resistances are much larger than the quantum resistance: $R \gg R_Q \approx 25.8$ kΩ.

The orthodox theory explains experiments very well if three assumptions are satisfied. However, experimental conditions do not always fullfil the first and third conditions. The first condition is broken by the existence of the discrete energy levels. This happens for ultrasmall islands, resulting in quantum kinetic energy $E_k \gg k_B T$. The third condition is broken by the presence of cotunneling processes. Nevertheless, the orthodox theory explains general aspects of SE phenomena [25].

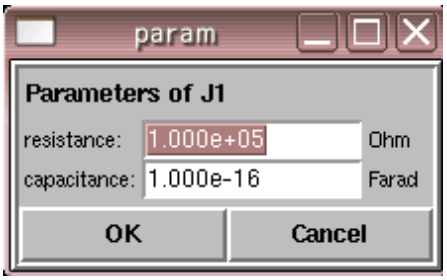
1.2 Single-electron transistor (SET)

A single-electron transistor (SET) is one of the most important devices which have been used for many applications of single electronics. There are two typical types of SETs so-called a capacitively-coupled SET (C-SET) and a resistively-coupled SET (R-SET). The difference between the two types is the coupling structure, capacitive or resistive, between the gate electrode and the center island electrode.

Characteristics of C-SET and R-SET are introduced by my own simulation using typical values. Below, capacitances of tunnel junctions are on the order of 100 aF. The relationship between the tunnel capacitance and the junction area depends on the method of fabrication. For example, $Al/Al_2O_3/Al$ tunnel junction fabricated by using shadow evaporation in Ref. [13] with the junction area of $(0.4\ \mu\text{m})^2$ has the tunnel capacitance on the order of 100 aF. Monte-Carlo simulation was executed using the SIMON program [26] in the conditions of 0 K and no cotunneling. Figure 1.3 shows an interface of the SIMON program. In Fig. 1.3(a), the left-hand side of the interface shows elements used to build the circuit. The right-hand side shows an example of a complete circuit used for simulation. This simulation circuit is composed of tunnel



(a)



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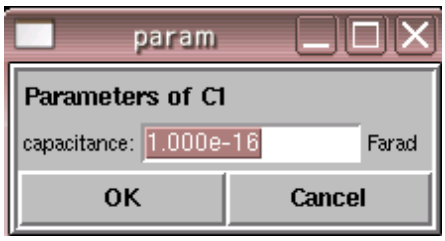

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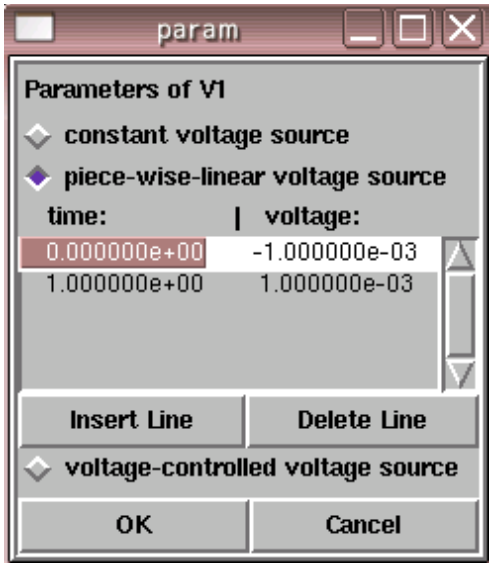


(d)

Figure 1.3: Interface of SIMON program. (a) Simulation circuit model. (b)-(d) Parameter boxes of tunnel junction, capacitor, and voltage, respectively.

junctions, a gate capacitor, and voltage sources. Current and voltage meters are used to measure the current and the voltage in the circuit, respectively. Parameters of the tunnel junction, the capacitor, and the voltage are set by using the parameter boxes in Fig. 1.3(b)-(d), respectively. After that, click "start" option on the top of the interface in Fig. 1.3(a) to simulate the circuit.

1.2.1 Capacitively-coupled single-electron transistor (C-SET)

A C-SET consists of two tunnel junctions (J_1 and J_2) and one gate capacitor (C_G) as shown in Fig. 1.4(a). The tunnel junction J_i has capacitance C_i and resistance R_i, with i = 1, 2. Three voltages including the drain voltage V_D, source voltage V_S, and gate voltage V_G are applied to drain, source, and gate terminals, respectively. The C-SET is biased symmetrically if $V_D = -V_S = V_{DS}/2$; and asymmetrically if $V_D = V_{DS}$ and $V_S = 0$. Below, only the symmetrically biased C-SET is considered. Calculations for conditions of Coulomb blockade (CB) phenomena use the same method as the previous literature [27, 28] as follows.

Charge quantization on the center island is given by

$$-ne = Q_1 - Q_2 + Q_G, \tag{1.3}$$

in which, e is the elementary charge ($e > 0$); n is the number of excess electrons on the center island; Q_i (i = 1, 2) is the charge on the junction J_i; Q_G is the charge on the capacitor C_G.

Changes in electrostatic energy of the circuit, $\Delta E_{i,\text{add}}$ (i = 1, 2), when an electron tunnels across the junction J_i onto the island are calculated as

$$\begin{aligned} \Delta E_{1,\text{add}} &= E_{\text{final}} - E_{\text{initial}} + \text{work}_1 \\ &= \frac{e}{C_\Sigma}\left[e\left(n+\frac{1}{2}\right) + V_{DS}\left(C_2 + \frac{C_G}{2}\right) - C_G V_G\right], \end{aligned} \tag{1.4}$$

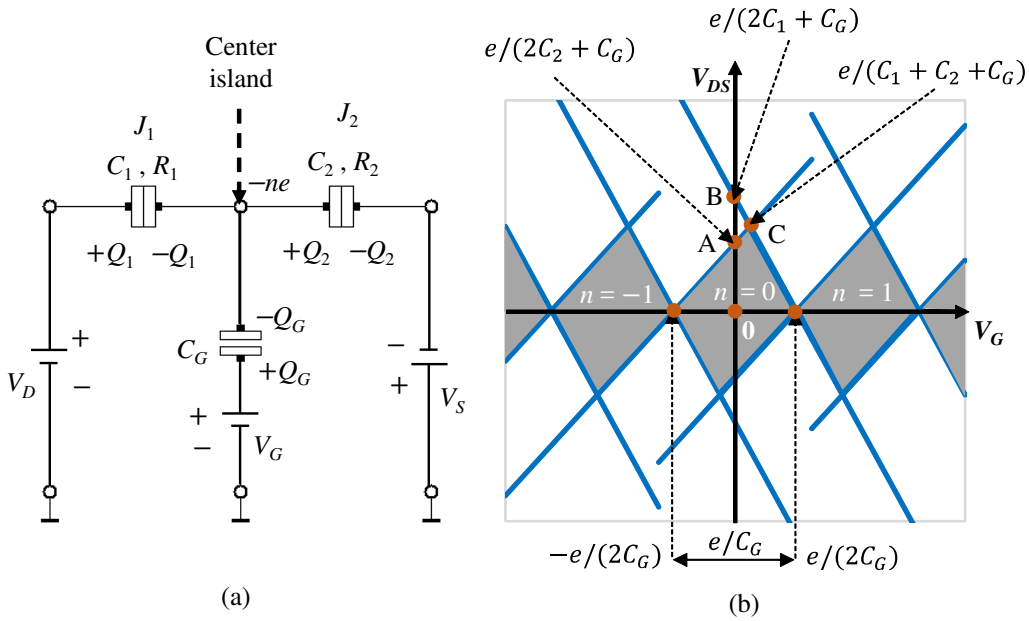


Figure 1.4: a) Schematic diagram of C-SET. b) Stability diagram of C-SET.

$$\begin{aligned}\Delta E_{2,\text{add}} &= E_{\text{final}} - E_{\text{initial}} + \text{work}_2 \\ &= \frac{e}{C_\Sigma}\left[e\left(n+\frac{1}{2}\right) - V_{DS}\left(C_1 + \frac{C_G}{2}\right) - C_G V_G\right]. \end{aligned} \tag{1.5}$$

Here, E_{initial} and E_{final} are respectively the charging energy of the circuit before and after the tunneling event; "work" is done by the drain, source, and gate voltages; $C_\Sigma = C_1 + C_2 + C_G$.

Similarly, changes in electrostatic energy of the circuit, $\Delta E_{i,\text{sub}}$ $(i = 1, 2)$, when an electron tunnels off the island across J_i are in the form of

$$\Delta E_{1,\text{sub}} = \frac{e}{C_\Sigma}\left[-e\left(n-\frac{1}{2}\right) - V_{DS}\left(C_2 + \frac{C_G}{2}\right) + C_G V_G\right], \tag{1.6}$$

$$\Delta E_{2,\text{sub}} = \frac{e}{C_\Sigma}\left[-e\left(n-\frac{1}{2}\right) + V_{DS}\left(C_1 + \frac{C_G}{2}\right) + C_G V_G\right]. \tag{1.7}$$

The electron does not tunnel onto and off the island if $\Delta E_{\text{add}} > 0$ and $\Delta E_{\text{sub}} > 0$ [27]. Hence, the CB regions of J_1 and J_2 are respectively determined as follows,

$$\frac{1}{C_2 + C_G/2}\left[C_G V_G - e(n + \frac{1}{2})\right] < V_{DS} < \frac{1}{C_2 + C_G/2}\left[C_G V_G - e(n - \frac{1}{2})\right], \tag{1.8}$$

$$\frac{1}{C_1 + C_G/2}\left[-C_G V_G + e(n - \frac{1}{2})\right] < V_{DS} < \frac{1}{C_1 + C_G/2}\left[-C_G V_G + e(n + \frac{1}{2})\right]. \tag{1.9}$$

Combination of Eqs. (1.8) and (1.9) shows that the CB regions of the C-SET have the diamond shapes on the $V_{DS} - V_G$ plane, in which each diamond (gray color) corresponds to one stable state of n as shown in Fig. 1.4(b) which is similar to the previous work [28]. The stability diagram (Fig. 1.4(b)) is a two-dimensional map of the stable states. On the $V_{DS} - V_G$ plane, a horizontal cut along the V_G axis through the Coulomb diamonds (for small V_{DS}) results in periodic current oscillations with a period of $\Delta V_G = e/C_G$, which is referred to as a "Coulomb oscillation". [28].

At the state $n = 0$, the conditions for CB regions of J_1 and J_2 are respectively reduced to the following formulas,

$$\frac{2C_G}{2C_2 + C_G}V_G - \frac{e}{2C_2 + C_G} < V_{DS} < \frac{2C_G}{2C_2 + C_G}V_G + \frac{e}{2C_2 + C_G} \tag{1.10}$$

$$-\frac{2C_G}{2C_1 + C_G}V_G - \frac{e}{2C_1 + C_G} < V_{DS} < -\frac{2C_G}{2C_1 + C_G}V_G + \frac{e}{2C_1 + C_G} \tag{1.11}$$

On the plane containing the positive vertical axis, the boundaries in Eqs. (1.10) and (1.11) cut the positive vertical axis at A(0, $e/(2C_2 + C_G)$) and B(0, $e/(2C_1 + C_G)$), and they cross at C($e(C_2 - C_1)/[2C_G(C_1 + C_2 + C_G)]$, $e/(C_1 + C_2 + C_G)$). The crosspoint C is called a peak of the diamond.

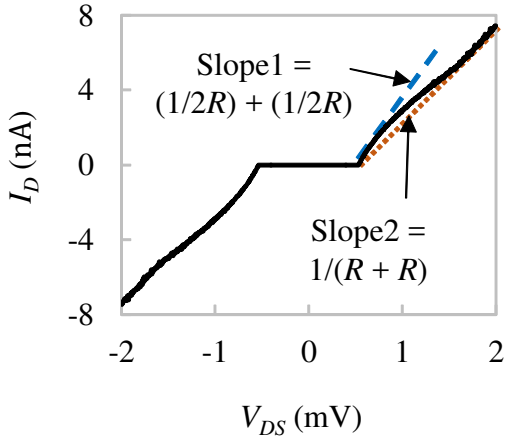


Figure 1.5: $I_D - V_{DS}$ characteristics of the symmetric C-SET ($C_1 = C_2 = C$ = 100 aF, $R_1 = R_2 = R$ = 100 kΩ, C_G = 100 aF) at $V_G = 0$ and $T = 0$ K.

From the relationship between the parameters of the tunnel junctions, the C-SET can be divided into two types including a symmetric C-SET and an asymmetric C-SET. In the symmetric C-SET, the parameters of the two tunnel junctions are the same, i.e., $C_1 = C_2$ and $R_1 = R_2$. In the asymmetric C-SET, the parameters of the two tunnel junctions are different, namely, $C_1 \neq C_2$ and/or $R_1 \neq R_2$.

1.2.1.1 Symmetric capacitively-coupled SET

For a symmetric C-SET with $C_1 = C_2 = C$ and $R_1 = R_2 = R$, its CB threshold voltage for $V_G = 0$ is $|(V_{DS})_{\text{th}}| = e/(C_1 + C_2 + C_G)$. Characteristics of the symmetric C-SET ($C_1 = C_2$ = 100 aF, $R_1 = R_2$ = 100 kΩ, C_G = 100 aF) are illustrated in Figs. 1.5 and 1.6. In Fig. 1.5, the CB threshold voltage $|(V_{DS})_{\text{th}}|$ is 0.53 mV. Figure 1.6 shows current oscillation with a period of ΔV_G = 1.6 mV. Absolute drain current $|I_D|$ on the $V_D - V_G$ plane is illustrated in Fig. 1.7, in which the Coulomb diamonds are represented by black areas surrounded by yellow diamonds. Because of the symmetric structure, the points A, B, and C in Fig. 1.4(b) converge to $(0,\ e/(C_1 + C_2 + C_G))$. Hence, shapes of the diamonds are symmetric to horizontal axis, i.e., they are not tilted relative to

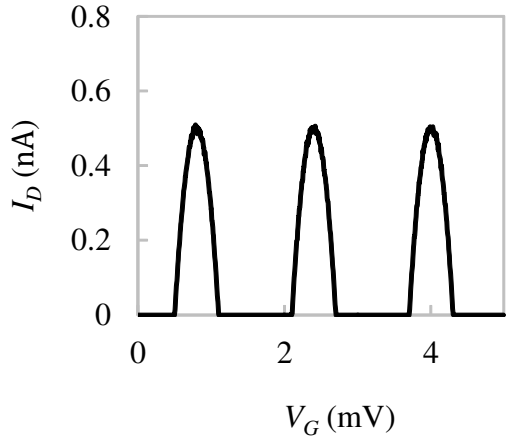


Figure 1.6: $I_D - V_G$ characteristics of the symmetric C-SET ($C_1 = C_2 = 100$ aF, $R_1 = R_2 = 100$ kΩ, $C_G = 100$ aF) at $V_{DS} = 0.2$ mV and $T = 0$ K

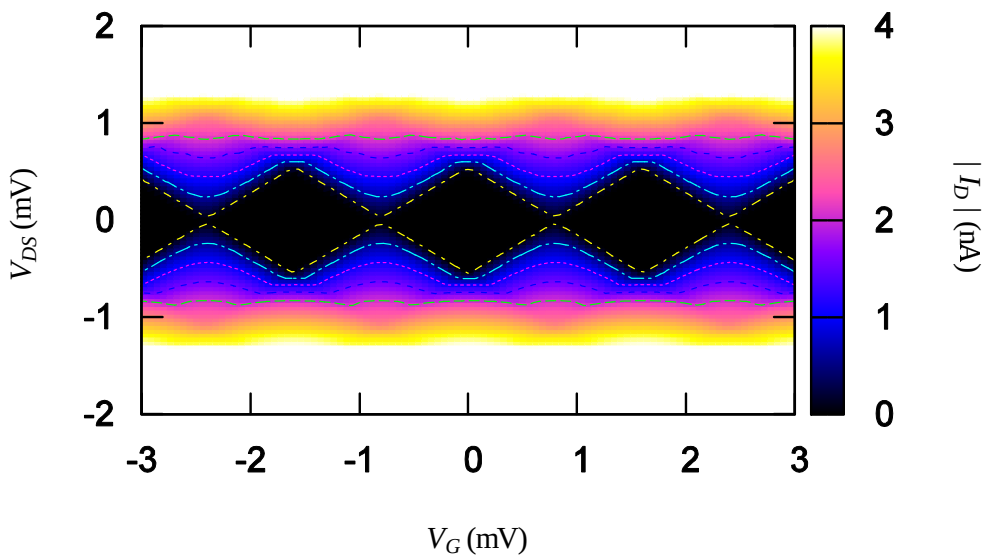


Figure 1.7: $|I_D|$ of the symmetric C-SET ($C_1 = C_2 = 100$ aF, $R_1 = R_2 = 100$ kΩ, $C_G = 100$ aF) is plotted on $V_D - V_G$ plane at $T = 0$ K.

the vertical axis.

It can be seen in Fig. 1.5 that there are two different slopes including slope1 $= (1/2R) + (1/2R)$ at small V_{DS} and slope2 $= 1/(R + R)$ at large V_{DS} [28].

They can be explained as follows [28]. Firstly, at small V_{DS} just beyond the CB threshold, probability for tunneling of electrons through J_1 (C, R) and J_2 (C, R) are the same. Therefore, electrons see two tunnel resistances as like as two parallel channels. If no charges are assumed on the center island, voltage aross J_1 and J_2 are the same $V_{DS}/2$. Then effective resistances of two parallel channels are $2R$ and $2R$, resulting in slope of tunnel current: slope1 = $(1/2R) + (1/2R)$. Secondly, at large V_{DS}, the large voltage overshadows Coulomb interaction. As a result, electrons see two tunnel resistances as R and R in series. $I_D - V_{DS}$ characteristics become linear with slope2 = $1/(R + R)$. Applying this theory for a specific case of the C-SET with $C_1 = C_2$ and $R_1 = R_2$ = 100 kΩ (Fig. 1.5), theoritical and simulated results of slope1 are respectively $1/(1.00\times10^5)$ and $1/(1.13\times10^5)$; those of slope2 are respectively $1/(2.00\times10^5)$ and $1/(1.98\times10^5)$. Therefore, the theoritical and simulated results are in good agreement.

1.2.1.2 Asymmetric capacitively-coupled SET (C-SET)

1.2.1.2.1 Asymmetric C-SET ($C_1 \neq C_2$) Here we deal with an asymmetric C-SET that has different junction capacitances ($C_1 \neq C_2$) but the identical junction resistances $R_1 = R_2$. Namely, the case I has $C_1 > C_2$ whereas the case II has $C_1 < C_2$. In the simulation below, we assume that $C_1 = 2C_2$ for case I and $C_2 = 2C_1$ for case II and that total capacitances of both cases are same. $I_D - V_{DS}$ and $I_D - V_G$ characteristics are illustrated in Figs. 1.8 and 1.9, respectively. The CB threshold voltage for $V_G = 0$, $|(V_{DS})_{\mathrm{th}}|$, of case I is the same as that of case II (Fig. 1.8). In addition, periods of current oscillations, ΔV_G, are the same e/C_G. However, in Fig. 1.9, the currents for these asymmetric C-SET are shifted along the V_G axis in comparison with the current for the symmetric C-SET. The reason can be explained on the basis of Fig. 1.4(b). Because $C_1 \neq C_2$, the peak C$(e(C_2 - C_1)/[2C_G(C_1 + C_2 + C_G)]$ of the diamond is not on the vertical axis, making the diamond tilted relative to the vertical axis. If $C_1 > C_2$, the horizontal coordinate of the peak C is negative, resulting in the diamond tilted to the left-hand side (Fig. 1.10(a)). If $C_1 < C_2$,

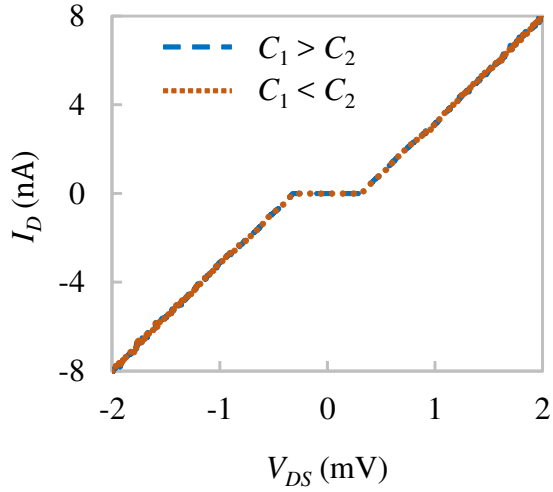


Figure 1.8: $I_D - V_{DS}$ characteristics of the asymmetric C-SET ($C_1 \neq C_2$ and $R_1 = R_2 = 100$ kΩ) at $V_G = 0$ and $T = 0$ K. There are two cases: case I with $C_1 > C_2$ (e.g., $C_1 = 200$ aF and $C_2 = 100$ aF) and case II with $C_1 < C_2$ (e.g., $C_1 = 100$ aF and $C_2 = 200$ aF).

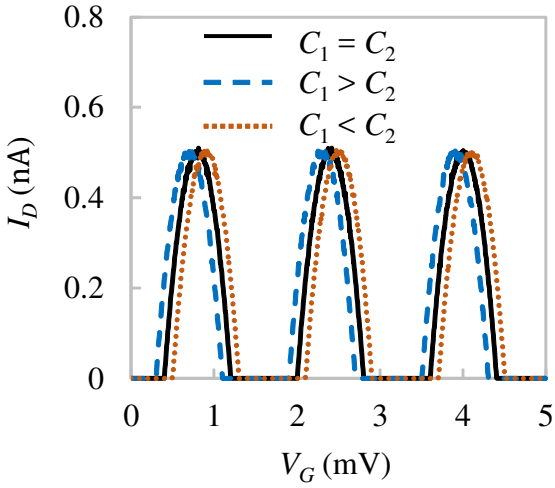


Figure 1.9: $I_D - V_G$ characteristics of the asymmetric C-SET ($C_1 \neq C_2$ and $R_1 = R_2 = 100$ kΩ) at $V_{DS} = 0.2$ mV and $T = 0$ K. There are three cases: case I with $C_1 > C_2$ (e.g., $C_1 = 200$ aF and $C_2 = 100$ aF), case II with $C_1 < C_2$ (e.g., $C_1 = 100$ aF and $C_2 = 200$ aF), and case III with $C_1 = C_2$ (e.g., $C_1 = C_2$ = 150 aF).

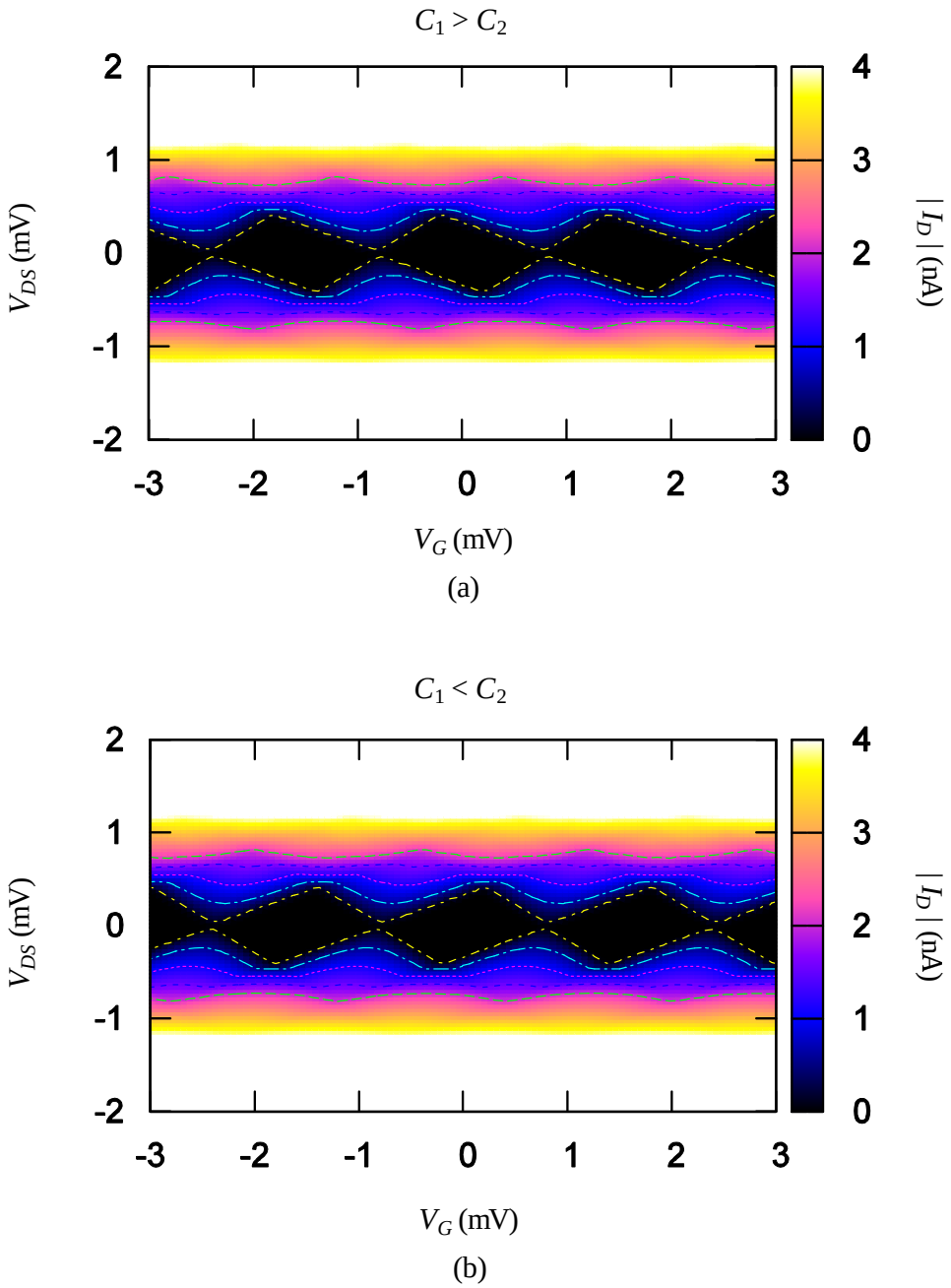


Figure 1.10: $|I_D|$ of the asymmetric C-SET ($C_1 \neq C_2$ and $R_1 = R_2 = 100$ kΩ) is plotted on $V_D - V_G$ plane at $T = 0$ K. a) $C_1 > C_2$ (e.g., $C_1 = 200$ aF and $C_2 = 100$ aF). b) $C_1 < C_2$ (e.g., $C_1 = 100$ aF and $C_2 = 200$ aF).

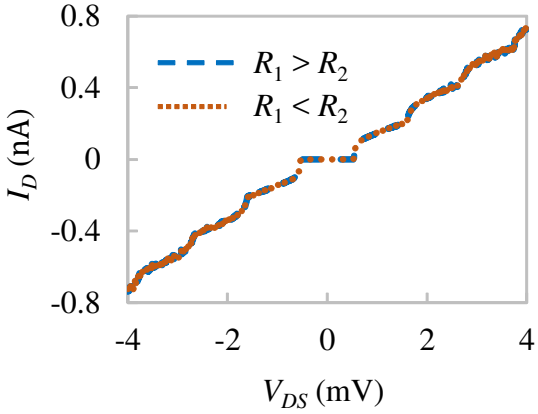


Figure 1.11: $I_D - V_{DS}$ characteristics of the asymmetric C-SET ($R_1 \neq R_2$ and $C_1 = C_2 = 100$ aF) at $V_G = 0$ and $T = 0$ K. There are two cases: case I with $R_1 > R_2$ (e.g., $R_1 = 5$ MΩ and $R_2 = 100$ kΩ) and case II with $R_1 < R_2$ (e.g., $R_1 = 100$ kΩ and $R_2 = 5$ MΩ).

the horizontal coordinate of the peak C is positive, resulting in the diamond tilted to the right-hand side (Fig. 1.10(b)). As a result, current oscillations of the cases $C_1 > C_2$ and $C_1 < C_2$ are respectively shifted to left-hand side and right-hand side in comparation with the case $C_1 = C_2$ (Fig. 1.9).

1.2.1.2.2 Asymmetric C-SET ($R_1 \neq R_2$) For an asymmetric C-SET with $R_1 \neq R_2$ and $C_1 = C_2$, the Coulomb staircase is observed in the $I_D - V_{DS}$ characteristics (Fig. 1.11). The current rises in a stepwise manner where each complete step means that an electron finishes tunneling through the two junctions. The change of the current in each step can be explained as follows [28]. Let us assume that $V_{DS} > 0$ and $V_G = 0$. If $R_1 > R_2$, the tunneling rate through J_1 is smaller than that through J_2. At small V_{DS} just over the CB region, an electron quickly tunnels across J_2 onto the island and accumulates on the island. A larger V_{DS} is needed to push the electron off the island through J_1. In contrast, for the symmetric C-SET with $R_1 = R_2$, the tunneling rates through J_1 and J_2 are the same, the electron tunnels across J_2 onto the island and immediately removes from island through J_1. As a result, the current in

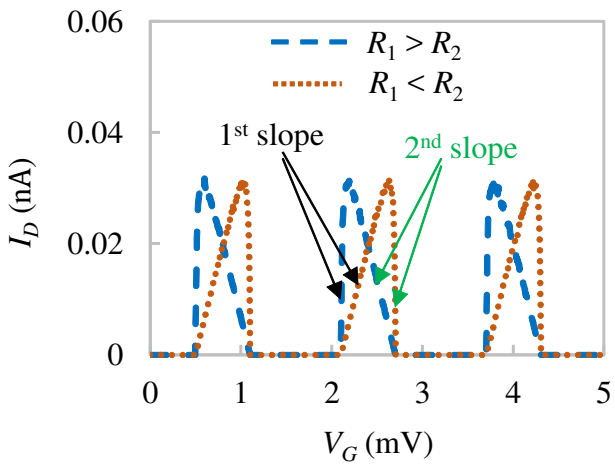
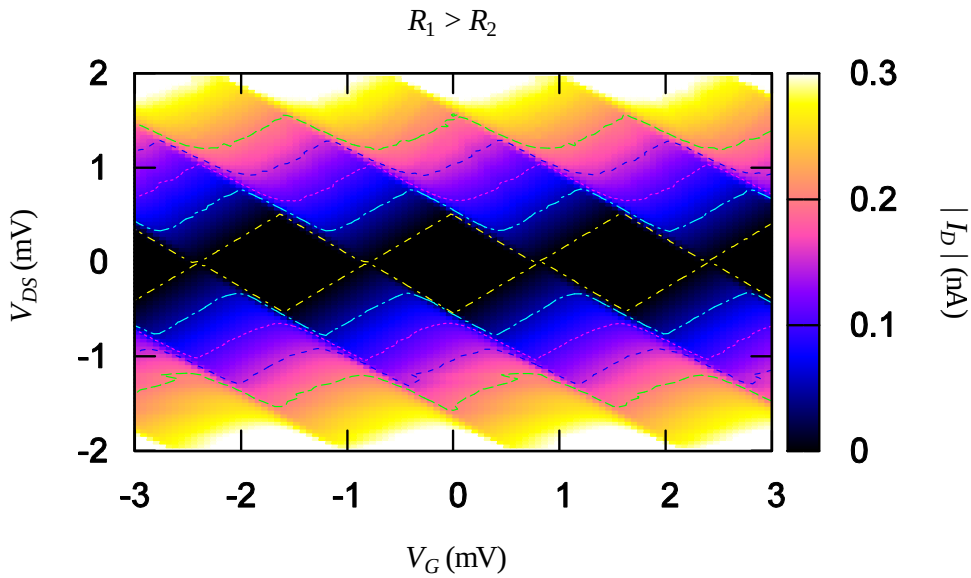


Figure 1.12: $I_D - V_G$ characteristics of the asymmetric C-SET ($R_1 \neq R_2$ and $C_1 = C_2 = 100$ aF) at $V_{DS} = 0.2$ mV and $T = 0$ K. There are two cases: case I with $R_1 > R_2$ (e.g., $R_1 = 5$ MΩ and $R_2 = 100$ kΩ) and case II with $R_1 < R_2$ (e.g., $R_1 = 100$ kΩ and $R_2 = 5$ MΩ).

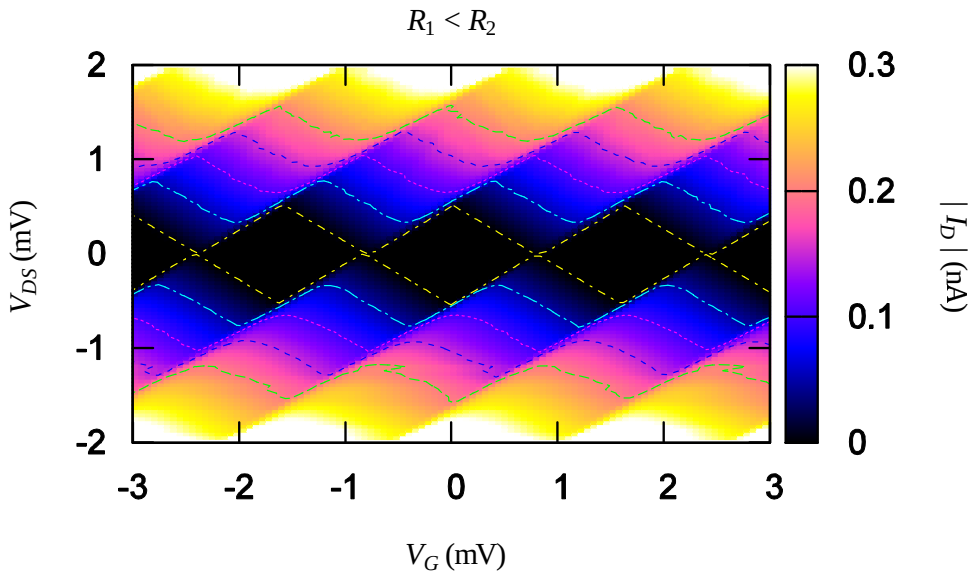
the symmetric C-SET increases linearly.

$I_D - V_G$ characteristics shows the current oscillations as illustrated in Fig. 1.12. It is observed that the current oscillations are tilted to the left-hand/right-hand side against the vertical axis. We consider the case of setting $V_{DS} > 0$ ($V_D > 0$ and $V_S < 0$) and applying $V_G > 0$. When V_G increases, electron firstly tunnels through J_2 and followed by tunneling through J_1. If $R_1 > R_2$ (dashed curves), the tunneling rate through J_2 is larger that through J_1. Consequently, the first slope is sharper than the second slope. Hence, the current oscillations are tilted to the left-hand side of the vertical axis. If $R_1 < R_2$ (dotted curves), the tunneling rate through J_1 larger than that through J_2. As a result, the second slope is sharper than the first slope. Therefore, the current oscillations are tilted to the right-hand side of the vertical axis.

Figure 1.13 illustrates the current magnitude of the asymmetric C-SET. The CB regions surrounded by yellow diamonds for $R_1 > R_2$ (Fig. 1.13(a)) and for $R_1 < R_2$ (Fig. 1.13(b)) are the same since $C_1 = C_2$. An increase of



(a)



(b)

Figure 1.13: $|I_D|$ of the asymmetric C-SET ($R_1 \neq R_2$ and $C_1 = C_2 = 100$ aF) is plotted on $V_D - V_G$ plane at $T = 0$ K. a) $R_1 > R_2$ (e.g., $R_1 = 5$ MΩ and $R_2 = 100$ kΩ). b) $R_1 < R_2$ (e.g., $R_1 = 100$ kΩ and $R_2 = 5$ MΩ).

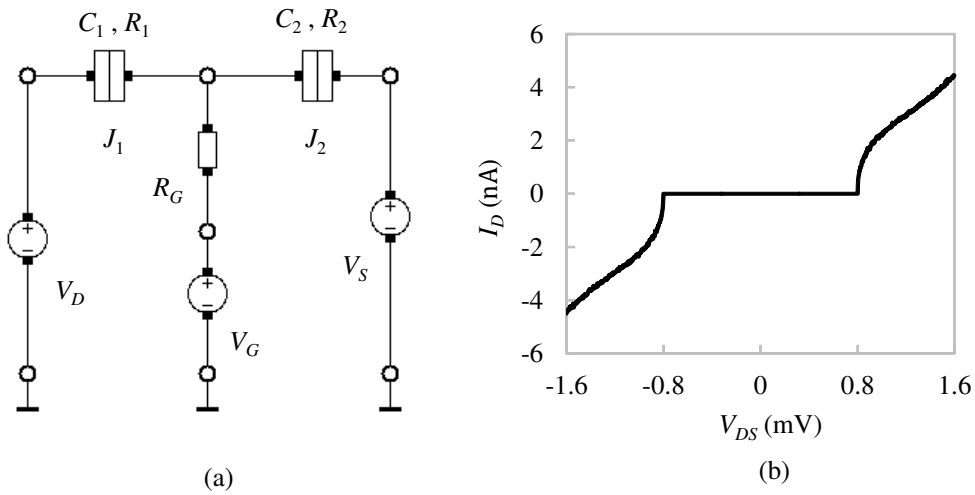
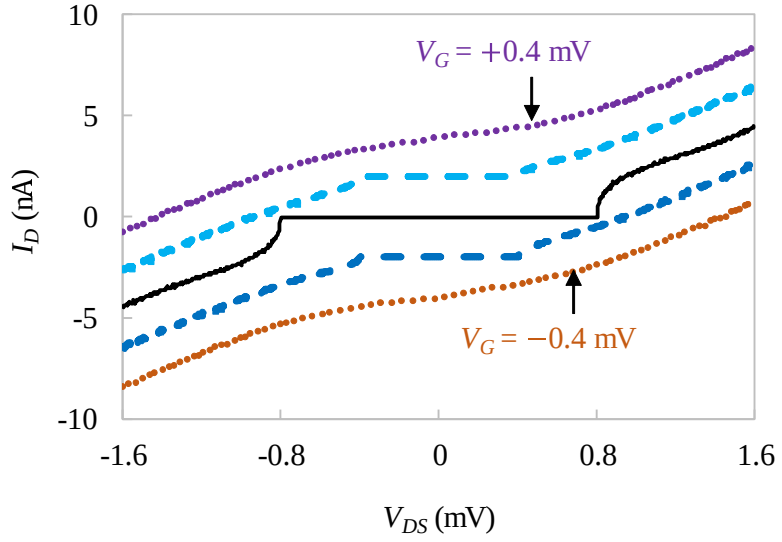


Figure 1.14: (a) Schematic diagram of R-SET. b) $I_D - V_{DS}$ characteristics of R-SET ($C_1 = C_2 = 100$ aF, $R_1 = R_2 = 100$ kΩ, $R_G = 1$ MΩ) at $V_G = 0$ and $T = 0$ K.

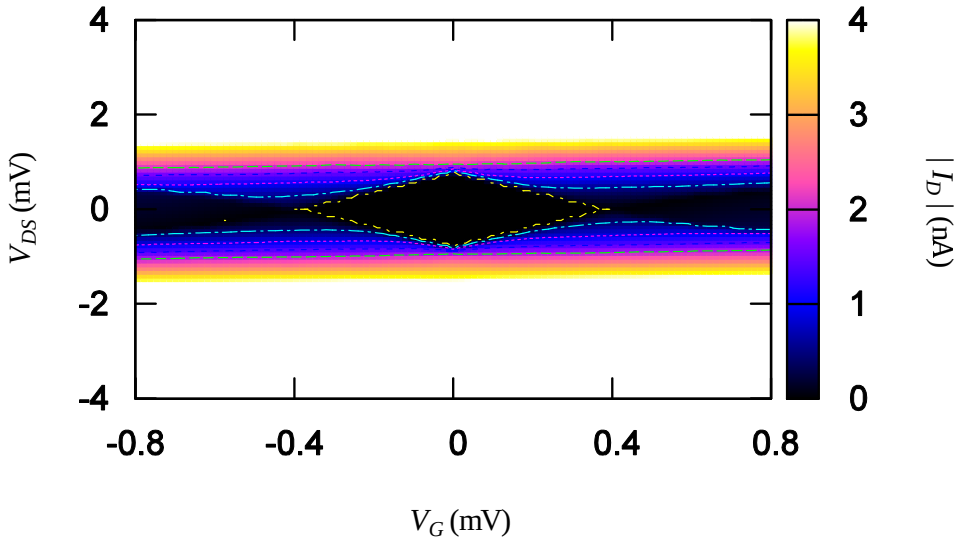
the current is shown by a change of colors from black to yellow. In one period of the Coulomb oscillations ΔV_G which is 1.6 mV, distributions of the colors are observed as follows. For example, we consider the case of small V_{DS} and V_G from 0 to 1.6 mV. In Fig. 1.13(a), the dark area (0 nA $< |I_D| <$ 0.05 nA) between the yellow curves and the blue curves at small V_G is narrower than that at large V_G. This agrees with the result for $R_1 > R_2$ in Fig. 1.12 where a sharper slope is obtained at small V_G. In Fig. 1.13(b), the dark area between the yellow curves and the blue curves at the small V_G is wider than that at the large V_G. This agrees with the result for $R_1 < R_2$ in Fig. 1.12 where a sharper slope is observed at large V_G.

1.2.2 Resistively-coupled single-electron transistor (R-SET)

A structure of a resistively-coupled SET (R-SET) is illustrated in Fig. 1.14(a). The R-SET is composed of two tunnel junctions and one gate resistor. Below, we consider characteristics of R-SET biased symmetrically. ($V_D = -V_S =$



(a)



(b)

Figure 1.15: Characteristics of R-SET ($C_1 = C_2 = 100$ aF, $R_1 = R_2 = 100$ kΩ, $R_G = 1$ MΩ) at $T = 0$ K. a) $I_D - V_{DS}$ characteristics when V_G varies from -0.4 mV to $+0.4$ mV in 0.2 mV steps (from bottom to top). b) $|I_D|$ is plotted on $V_D - V_G$ plane.

$V_{DS}/2$). The CB region should satisfy the following conditions [28],

$$\begin{cases} \left|\frac{V_{DS}}{2} - V_G\right| < \frac{e}{2(C_1 + C_2)} \\ \\ \left|\frac{V_{DS}}{2} + V_G\right| < \frac{e}{2(C_1 + C_2)} \end{cases} \tag{1.12}$$

According to Eq. (1.12), there is only one Coulomb diamond or no Coulomb oscillations. It can be seen in Fig. 1.15(a), when the absolute gate voltage $|V_G|$ increases, the CB region decreases to 0 without restoration. As a result, only one Coulomb diamond is observed in Fig 1.15(b). When $V_G = 0$, the CB threshold voltage is $|(V_{DS})_{\text{th}}| = e/(C_1 + C_2)$. For $V_{DS} = 0$, the CB diamond disappears at $|(V_G)_{\text{limit}}| = e/2(C_1 + C_2)$. For example, the R-SET with $C_1 = C_2 = 100$ aF, $R_1 = R_2 = 100$ kΩ, and $R_G = 1$ MΩ has following parameters: $|(V_{DS})_{\text{th}}| = e/(C_1 + C_2) = 0.8$ mV (Fig. 1.14(b)), $|(V_G)_{\text{limit}}| = e/2(C_1 + C_2) = 0.4$ mV (Fig. 1.15).

1.3 Purpose of this thesis

On the basis of the principle of the CB phenomena in arrays of small tunnel junctions in SE devices, this thesis intends to reach two main goals as follows.

The first objective of the thesis is to improve the nonlinear characteristics of SE logic devices by using simulation. SE logic devices including SE inverter and SE NAND gates have a disadvantage of the gradual switches between high and low output levels [29, 30]. Figure 1.16 shows an example of the gradual switching. The SE inverter (Fig. 1.16(a)) has a continuous input signal V_{in}, a source voltage V_s, and an output signal V_{out}. Schematic input-output characteristics of the SE inverter at 0 K are shown in Fig. 1.16(b). When V_{in} is low, V_{out} is high and vice versa. However, for V_{in} in the region AB, while V_{in} increases, V_{out} gradually decreases from the high to low level, resulting in a gradual switching as shown by the arrow in Fig. 1.16(b). Then,

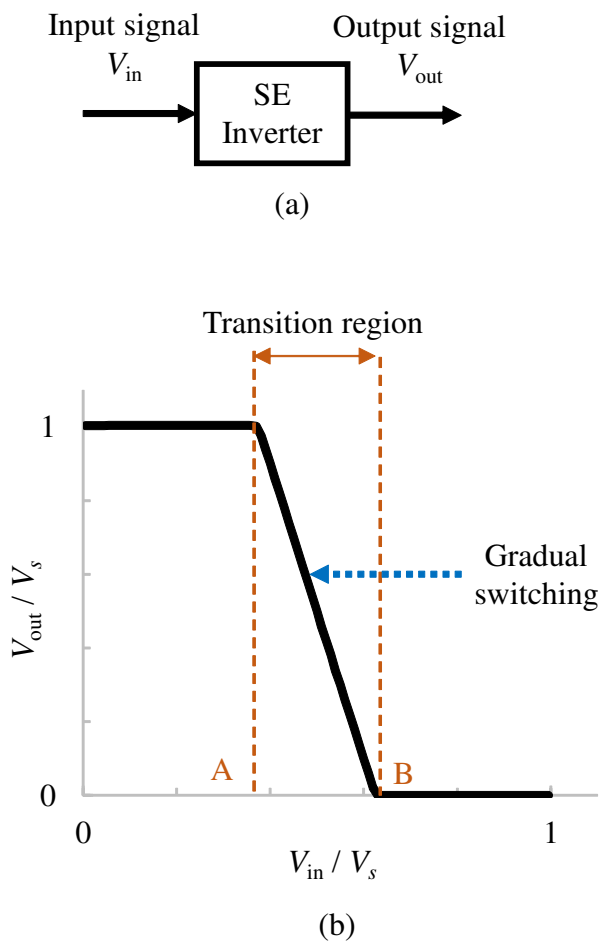


Figure 1.16: (a) Block diagram of a single-electron inverter. (b) Schematic drawing of gradual switching of the SE inverter at 0 K.

the region AB is called the transition region where output states are unclear.

To improve the gradual switching of SE logic devices, a model of an input discretizer (ID) [31] is added between an input terminal and a main device (SE logic device) as shown in Fig. 1.17(a). The addition of the ID which discretizes a continuous input signal into a discrete intermediate signal is expected to make the switching sharp (Fig. 1.17(b)). Configuration of the ID is modified from the previous work [31]. Parameters of the ID are calculated and then confirmed by simulation to obtain the sharp switching at the designed threshold voltage. The method and results of the enhancement of SE logic gates by using the ID will be described in Chapter 2.

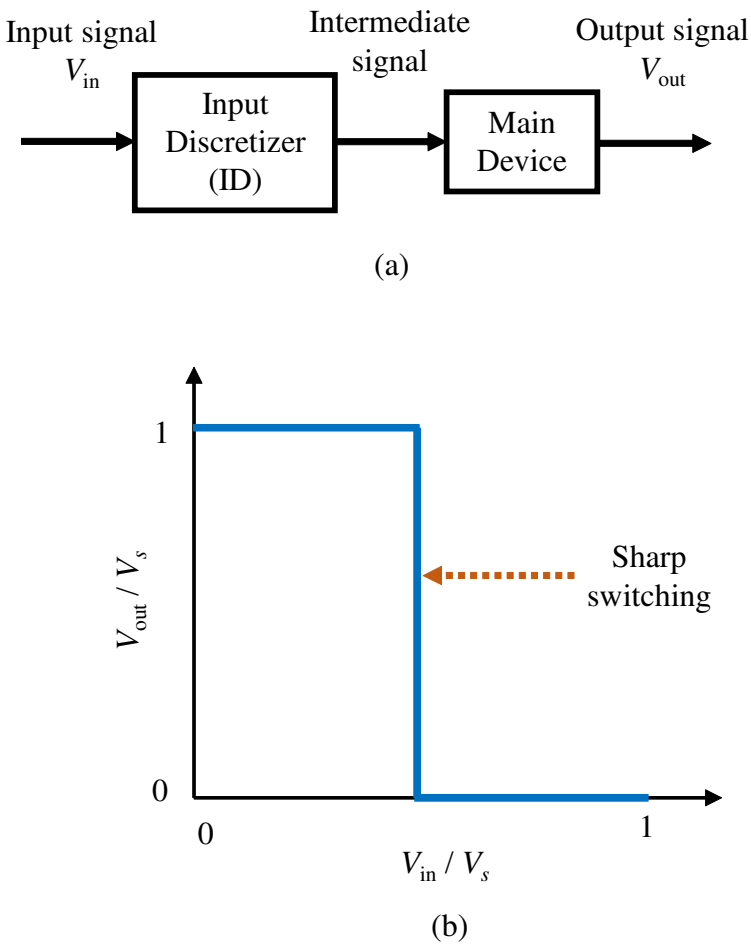


Figure 1.17: (a) Model shows the addition of an input discretizer (ID) to the main device (SE logic device). (b) Schematic drawing of sharp switching of SE inverter at 0 K.

On the other hand, if two serially-cascaded IDs are added to the SE inverter (Fig. 1.18(a)), the difference between the switching voltages for V_{in} increasing and decreasing, V_{H} and V_{L}, can form hysteretic characteristics as shown in Fig. 1.18(b). This SE hysteretic inverter is designed to improve stochastic resonance phenomena, so that correlation coefficient between the input and output signals of the SE hysteretic inverter is equivalent to that of the ideal hysteretic inverter. The improvement of stochastic resonance by designing the SE hysteretic inverter will be presented in Chapter 3.

The second objective of the thesis is to fabricate SE devices. Since, in the

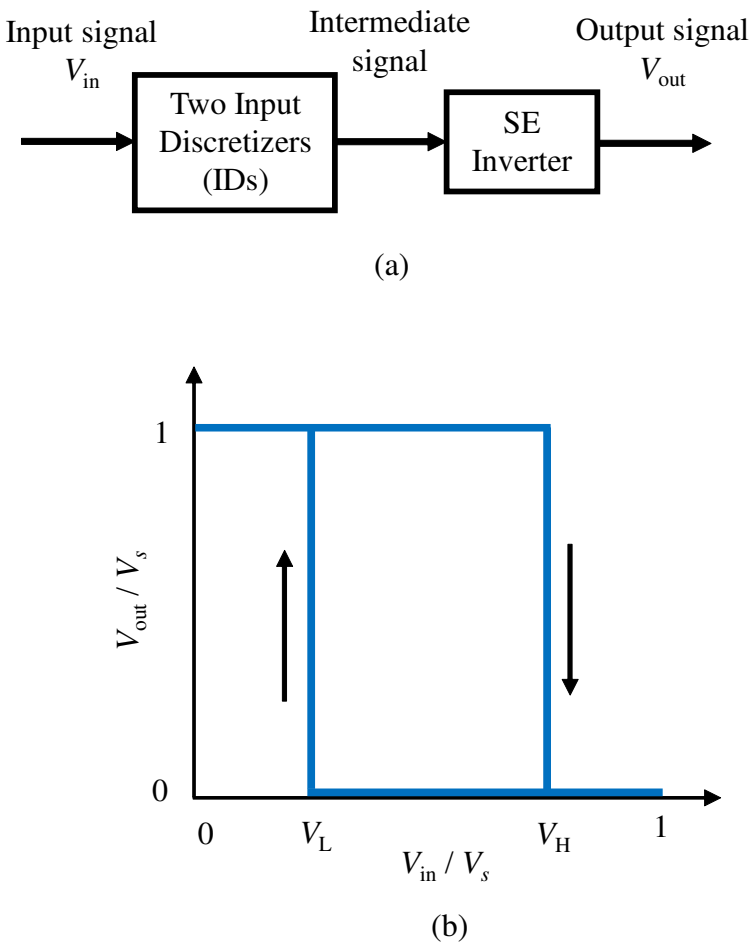


Figure 1.18: (a) Model shows the addition of two serially-cascaded input discretizers (IDs) to the main device (SE inverter). (b) Schematic drawing of hysteretic characteristics of SE inverter at 0 K.

simulation, SE logic devices are built on the basis of SETs, fabrication of SETs is the key to realize the simulation results. Hence, the thesis tries to focus on fabricating SE devices which have the characteristics like SETs. Because SET consists of three terminals, three electrodes including source, drain, and gate as shown in Fig. 1.19 are firstly formed. The gap size is defined as the distance between the source and drain electrodes. The drain, source, and gate electrodes are fabricated by combining standard electron beam lithography (EBL) and evaporation techniques. Next, arrays of small tunnel junctions are formed by dropping solutions of gold nanoparticles (Au NPs). After that, the fabricated

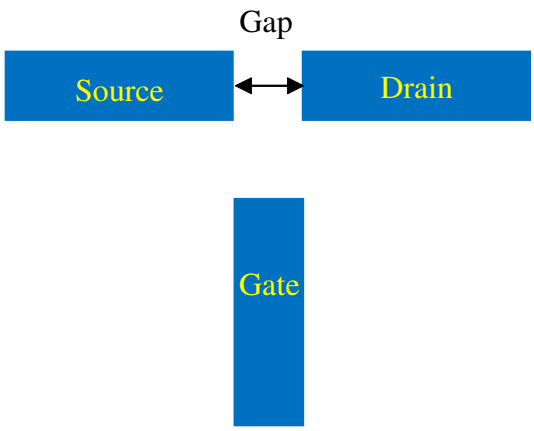


Figure 1.19: Schematic drawing of drain, source, and gate electrodes of SE device.

devices are measured to confirm their characteristics. The similar fabrication process using Au NPs was reported in the previous works [14,32] whose devices had the narrow (< 50 nm) gaps and exhibited the C-SET characteristics at 4.2 K [32] and 80 K [14]. Hence, the thesis tries to reduce the technical difficulty by forming a wider (≥ 200 nm) gap to exhibit the characteristics like C-SET at almost equivalent temperature (77 K) in comparison with the previous work [14] (80 K). Besides, there were reports about realization of the R-SET characteristics [33–35]. In these previous works, they did not use Au NPs in the fabrication process and observed the R-SET characteristics at sub-1-K. Therefore, the thesis tries to use a method with the presence of Au NPs to obtain the characteristics like R-SET at higher temperature (77 K) compared to the previous works [33–35] (sub-1-K). The fabrication processes and typical experimental results of SE devices using Au NPs will be demonstrated in Chapter 4.

In addition, Chapter 1 will give a background of SE devices and Chapter 5 will summarize the main results of the thesis.

Chapter 2

Enhancement of single-electron digital logic gates by using input discretizers

2.1 Introduction

Single-electron (SE) devices have been developed by a plenty of researches over three decades [25]. In comparison with conventional semiconductor devices, SE devices have two important advantages as follows. The first one is the size of SE elements on the order of nanometer. The second one is the possibility of saving power consumption [36]. Hence, they are prospective for intergrated circuit applications [37].

Applications of SE devices have been studied in both fields of analog and digital electronics. For the former, several analog applications have been carried out by using SE devices, such as the supersensitive electrometer [38], the standard of dc current [39] using the SE pump [40], and the absolute thermometer [41]. For the latter, fabrication of SE devices have been performed [42–46]. Nonetheless, in logic circuits, the prospect of SE logic (SEL) [47–50] and SE transitor (SET) [51] has faced obstacles and uncertainty. Among these logic devices, SET logic circuits have two following convenient factors. Firstly, SET logic circuits on the basis of capacitively-coupled SET (C-SET) [52–54] use

voltage levels to represent logic "0" and logic "1" as usual. Secondly, we can use schematics of CMOS circuits to contruct functionality of SET logic circuits [55]. Therefore, the development of SET logic circuits has been the objective of the researches. Two of the basic elements of the SET logic gates are SE four-junction inverter (SE FJI) [29, 56] and SE NAND gates [30].

On the one hand, the SE logic gates (SE FJI and SE NAND) have the same typical disadvantage in common, which are gradual switches between output logic levels (Fig. 1.16(b)) resulting in unclear decisions about output states in the transition region. Hence, performance of the SE logic gates can be improved by making their switches sharp.

On the other hand, it was confirmed that the addition of an input discretizer (ID) between the input terminal and the main device (SE transistor, SE turnstile) resulted in the sharp switches in the input-output characteristics [31]. Therefore, in this thesis, structure of the ID is modified to make the switches of SE logic gates sharp. In addition, in the previous design [31], the current played the role of the circuit output, which makes it difficult to increase the number of fan-ins and fan-outs. To solve this problem, in this thesis, the IDs are designed for SE devices whose outputs are the voltages charging the output capacitors. The voltage-input and voltage-output scheme enables us to connect devices in straightforward styles.

In comparison with the previous work [31], there are four significant enhancements as follows. Firstly, the structure of the ID is modified from one to two output capacitors. Secondly, the main devices are changed from the fundamental SE devices (SE transistor and SE turnstile) to SE logic gates (SE inverter and SE NAND gates) which are composed of several SE transistors. Thirdly, the main device has output voltage instead of output current. Finally, parameters of the ID are calculated to satisfy that the sharp switching happens at the designed threshold voltage, which aims to enhance the reliability of state decisions of the logic circuits.

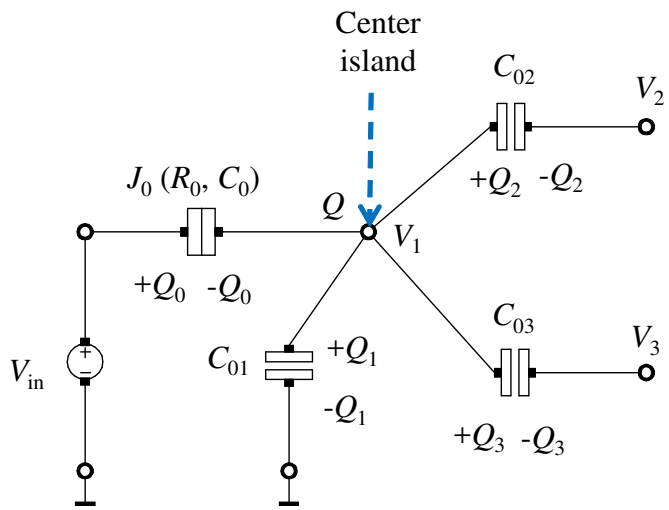


Figure 2.1: Schematic diagram of input discretizer (ID).

2.2 Analysis of parameters design of input discretizer (ID)

A conventional ID has one output capacitor [31]. To couple the ID with logic devices having two input gate capacitors (SE inverter and SE NAND), a configuration of the ID is modified from one to two output capacitors as shown in Fig. 2.1. The ID is composed of a tunnel junction J_0 (tunnel resistance R_0 and tunnel capacitance C_0), a grounded capacitor C_{01}, and two output capacitors C_{02} and C_{03}. A continuous input voltage V_{in} is applied to the ID. There are two output voltages V_2 and V_3.

Polarization charges on the junction and the individual capacitors can be expressed as follows,

$$Q_0 = C_0(V_{\text{in}} - V_1), \tag{2.1}$$

$$Q_1 = C_{01}V_1, \tag{2.2}$$

$$Q_2 = C_{02}(V_1 - V_2), \tag{2.3}$$

$$Q_3 = C_{03}(V_1 - V_3). \tag{2.4}$$

Here, Q_0 is the charge on the junction; Q_i ($i = 1, 2, 3$) is the charge on the capacitor C_{0i}; V_1 is the voltage across the capacitor C_{01}.

Charge quantization on the center island is written as

$$Q = -Q_0 + Q_1 + Q_2 + Q_3 = Ne + Q_P, \tag{2.5}$$

in which, N, e (> 0), and Q_P are respectively the number of excess electrons on the center island, the elementary charge, and the background polarization charge [57]. In this chapter, the backround polarization charge is assumed to be eliminated, i.e., $Q_P = 0$. (The origin of the backround polarization charge drives from charged impurities in the insulating environment, for example on the substrate surface. Several suggestions for solving this problem have been carried out by Likharev [25], Lambe and Jaklevic [58].) To get the same V_2 and V_3, we set

$$C_{02} = C_{03}. \tag{2.6}$$

Voltage V_0 across the junction J_0 is calculated by combining Eqs. (2.1)-(2.6),

$$\begin{aligned} V_0 &= V_{\text{in}} - V_1 \\ &= \frac{V_{\text{in}}(C_{01} + 2C_{02}) - C_{02}(V_2 + V_3) - Ne}{C}. \end{aligned} \tag{2.7}$$

Here the total capacitance C between the center island and its environment is given by,

$$C = C_0 + C_{01} + 2C_{02}. \tag{2.8}$$

Forward tunneling (the charge $+e$ tunnels from left to right) through the junction happens when the voltage across the junction is larger than the following

threshold voltage [29]

$$V_{0\mathrm{T}} = e/2C. \tag{2.9}$$

Subsitution of Eqs. (2.8) and (2.9) into Eq. (2.7), the input threshold voltage V_{inT} for tunneling through the junction is as follows,

$$V_{\mathrm{inT}} = \frac{(N + 1/2)e + C_{02}(V_2 + V_3)}{C_{01} + 2C_{02}}. \tag{2.10}$$

The input voltage is assumed to be linear in the range from 0 to source voltage V_s. A standard threshold voltage is defined as a half of V_s, i.e., $(V_{\mathrm{T}})_{\mathrm{Std}} = V_s/2$. When the tunneling event causes the switching between the output logic levels, V_{inT} is called V_{inS} (the switching threshold voltage). According to Eq. (2.10), since C_{02} (and C_{03}), which is the output capacitor of the ID, also plays the role of the input capacitor of the main device, value of C_{01} must be adjusted to make V_{inS} as close to $(V_{\mathrm{T}})_{\mathrm{Std}}$ as possible.

2.3 Improvement of single-electron four-junction inverter (SE FJI) using input discretizer (ID)

2.3.1 Characteristics of single-electron four-junction inverter (SE FJI)

A schematic diagram of an SE four-junction inverter (FJI) is shown in Fig. 2.2(a) [29]. The FJI consists of two SETs (an upper SET and a lower SET) in series among the power supply and ground [29]. The upper SET (SET1) of the FJI includes two junctions (J_1 and J_2), a gate capacitor (C_G), and a bias capacitor (C_B). The lower SET (SET2) of the FJI is composed of two junctions (J_3 and J_4) and two capacitors (C_G and C_B). The FJI is supplied

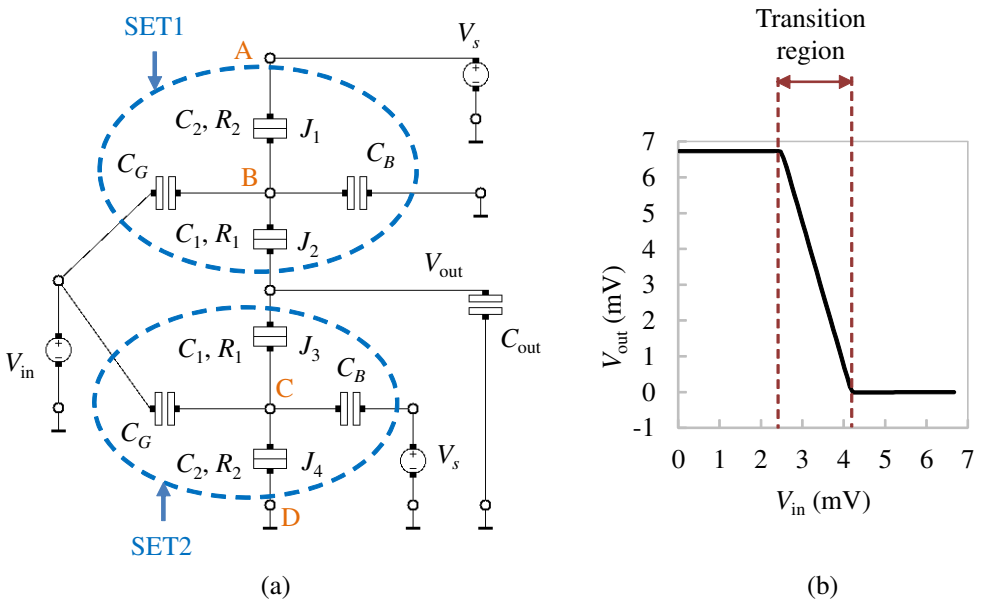


Figure 2.2: (a) Schematic diagram of a single-electron (SE) four-junction inverter (FJI). (b) Input-output characteristics of the FJI at $T = 0$ K.

by a source voltage V_s and its input terminal is applied by the signal voltage V_{in}. An output signal V_{out} is the voltage across an output capacitor C_{out}.

Parameters of the FJI are similar to those in the previous literature [29]: $C_1 = 2C_2$, $C_G = 8C_2$, $C_B = 7C_2$, $C^* = C_1 + C_2 + C_G + C_B$, $V_s = 1.5e/2C^*$. Here, C_G is assumed to be larger than the junction capacitances (C_1 and C_2) so that the voltage gain of the inverter can be greater than unity. The capacitance relationships of $C_G > C_1$ and $C_G > C_2$ were realized in the previous experiment [56]. The voltage $V_s = 1.5e/2C^*$, which is equivalent to $C_B V_s \approx 0.29e$, is also applied to the SET2 to make the transition region symmetrical to $0.5V_{\text{in}}/V_s$ [29]. On the basis of the same capacitance relationships as in the previous literature [29], we set a typical value of C_2, $C_2 = 1$ aF, and calculate the other capacitances. Then, in the numerical simulation described in this chapter, values of the FJI parameters are assumed that $C_1 = 2$ aF, $R_1 = 50$ kΩ, $C_2 = 1$ aF, $R_2 = 100$ kΩ, $C_G = 8$ aF, $C_B = 7$ aF, $V_s = 6.7$ mV, and $C_{\text{out}} = 1$ fF. Monte-Carlo simulation was executed by using SIMON program [26] in the conditions of 0 K and no cotunneling [59, 60].

Input-output voltage ($V_{\text{in}} - V_{\text{out}}$) characteristics of the solo FJI is illustrated in Fig. 2.2(b). A transition region between high and low output levels is defined as the region between two operation points at which slopes are -1 [61]. The FJI exhibits a gradual switching in the transition region between 2.48 mV and 4.22 mV. As a result, decisions about output states of the FJI in the transition region become of unclarity. The logic levels are defined as: logic "1" corresponds to the high level of the voltage; logic "0" is equivalent to the low level of the voltage.

2.3.2 Characteristics of a single-electron four-junction inverter with an input discretizer (ID-FJI)

To improve the characteristics of the solo FJI, an input discretizer (ID) is coupled to the FJI as shown in Fig. 2.3. Here, the output capacitances of the ID play the role of gate capacitances of the FJI, i.e., $C_{02}(C_{03}) \equiv C_G$. To make the switching threshold voltage V_{inS} of the ID-FJI close to the standard threshold voltage $(V_{\text{T}})_{\text{Std}}$, the appropriate parameters of the ID in Fig. 2.3 are chosen as: $C_0 = 1$ aF, $R_0 = 100$ kΩ, $C_{01} = 72$ aF. The output capacitances of the ID are 8 aF since $C_G = 8$ aF.

The number of excess electrons, $N = Q/e$, and the voltage V_{ID} on the center island versus the input voltage V_{in} are demonstrated by solid triangles and open circles in Fig. 2.4, respectively. It is observed that the charge on the center island is discretized into distinct states (N). A transistion between two states is caused by a tunneling event.

The simulated $V_{\text{in}} - V_{\text{out}}$ characteristics of the solo FJI and the ID-FJI are respectively represented by open circle points and solid triangle points as illustrated in Fig. 2.5. It can be seen that a sharper switching achieved by the ID-FJI than by the solo FJI. Namely, the switching region of the solo FJI expands from 2.48 mV to 4.22 mV, which is $(4.22 - 2.48) \times 100\%/6.7 \approx 25.97\%$ of the input voltage range (V_{in} from 0 to 6.7 mV). In contrast, the ID-FJI exhibits a sharp switching in the region between 3.38 mV and 3.40 mV, which is $(3.40 - 3.38) \times 100\%/6.7 \approx 0.30\%$ of the input voltage range. The swiching

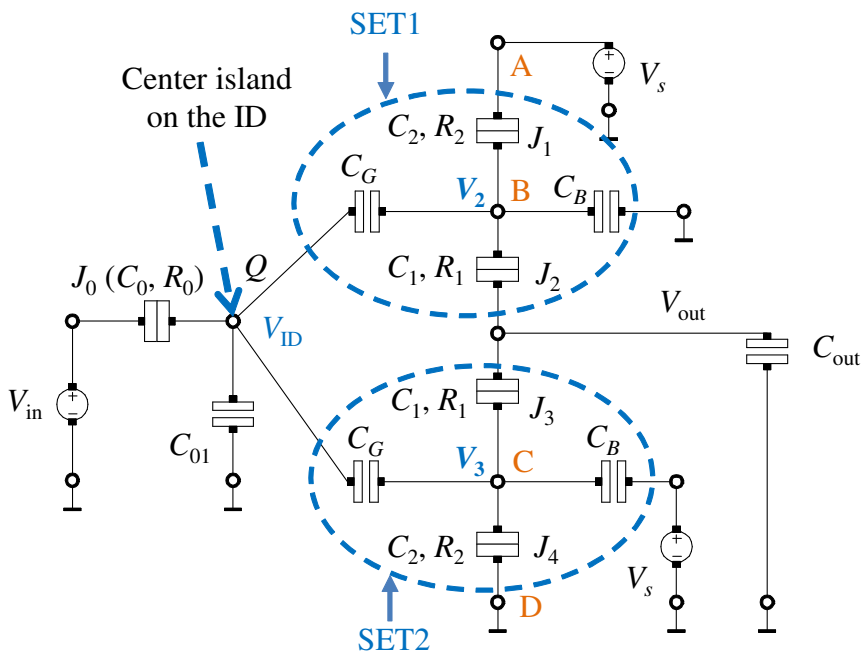


Figure 2.3: Schematic diagram of a single-electron (SE) four-junction inverter with an input discretizer (ID-FJI).

region of the ID-FJI is reduced to 0.011 times in comparison with that of the solo FJI.

Besides, in Fig. 2.5, the sharp swiching of the ID-FJI appears at the simulated threshold voltage $(V_{\mathrm{inS}})_{\mathrm{sim}}$ of 3.38 mV where there is a tunneling event from $N = 1$ to $N = 2$ (Fig. 2.4). On the other hand, in Fig. 2.2, the tunnel junctions J_1 and J_4 have the same parameters (C_2 and R_2). Then, the absolute voltage $|V_{\mathrm{AB}}|$ across J_1 is approximately equal to the absolute voltage $|V_{CD}|$ across J_4 (Fig. 2.2). In the transition region, the current flows through the tunnel junctions with the same direction, resulting in $V_{\mathrm{AB}} \approx V_{CD}$. As a result, the total voltage $V_{BD}+V_{CD}$ is approximately V_s in the transition region of the FJI. Applying this result for Fig. 2.3, the total output voltage of the ID in the transition region, V_2+V_3, is approximately V_s. Subsituting the simulated parameters of the ID and $N = 1$ to Eq. (2.10), the calculated threshold voltage $(V_{\mathrm{inS}})_{\mathrm{cal}}$ is 3.34 mV. Therefore, the simulated threshold voltage $(V_{\mathrm{inS}})_{\mathrm{sim}}$ and

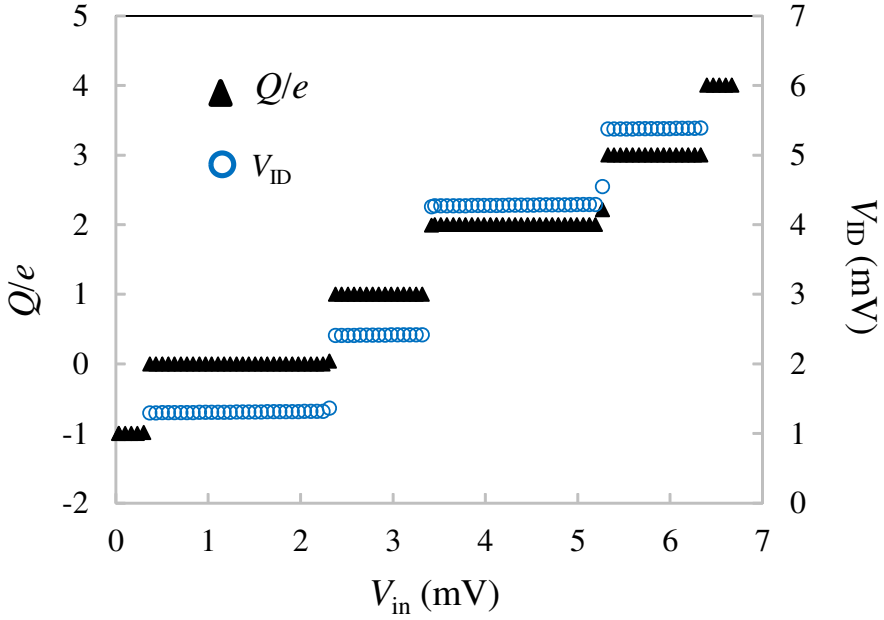


Figure 2.4: Characteristics of the ID in the ID-FJI at $T = 0$ K. Number of excess electrons in the center island of the ID, $N = Q/e$, is plotted as a function of the input voltage V_{in}. The voltage V_{ID} between the center island of the ID and ground versus V_{in}.

the calcultated threshold voltage $(V_{\mathrm{inS}})_{\mathrm{cal}}$ are close to each other.

The enhancement of the sharpness of the ID-FJI can be explaind as follows. For the solo FJI, the gradual swiching is observed between the high and low output voltages because of the continuous input signal V_{in}. For the ID-FJI, since the ID processes the continuous V_{in} into a discrete intermediate signal V_{ID} forwarded to the main device FJI, the ID-FJI exhibits the sharp switching. In addition, the operation principle of an inverter is still ensured in the ID-FJI as follows. In the ID-FJI, the direct input voltage of the main device FJI is V_{ID}. Hence, for the ID-FJI, the switching between the high and low output levels only occurs when V_{ID} is in the switching region of the FJI which is between 2.48 mV and 4.22 mV. In Fig. 2.4, V_{ID} can be divided into three regions: under 2.48 mV, between 2.48 mV and 4.22 mV, and over 4.22 mV. In the first region, since the levels of V_{ID} are less than 2.48 mV, the output of the ID-FJI (Fig.

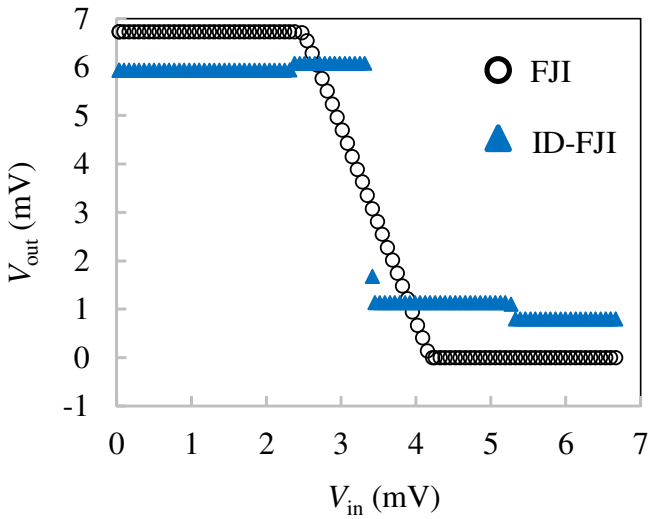


Figure 2.5: Input-output characteristics of the solo FJI and the ID-FJI at T = 0 K.

2.5) remains high (logic "1"). In the third region, because the levels of V_{ID} are greater than 4.22 mV, the output of the ID-FJI (Fig. 2.5) keeps low (logic "0"). Hence, the discreteness of V_{ID} in both the first and the third regions does not degrade the logic states of the inverter. Since the second region of V_{ID} corresponds to the switching region of the solo FJI, changes of V_{ID} in this region cause the switching of the ID-FJI. It is observed in Fig. 2.4 that in the range of 2.48 mV and 4.22 mV, there is only one tunneling event, resulting in only one switching between the high and low output states in the ID-FJI (Fig. 2.5).

2.3.3 Evaluation of switching characteristics of the solo FJI and ID-FJI

Dynamic characteristics of the solo FJI and the ID-FJI are shown in Fig. 2.6. A transient input signal in the shape of a triangle is applied to the solo FJI and the ID-FJI for two periods (Fig. 2.6(a)). Transient output signals of the solo FJI and the ID-FJI are respectively observed in Figs. 2.6(b) and (c). The dynamic characteristics in Fig. 2.6(c) indicates that the ID-FJI is able

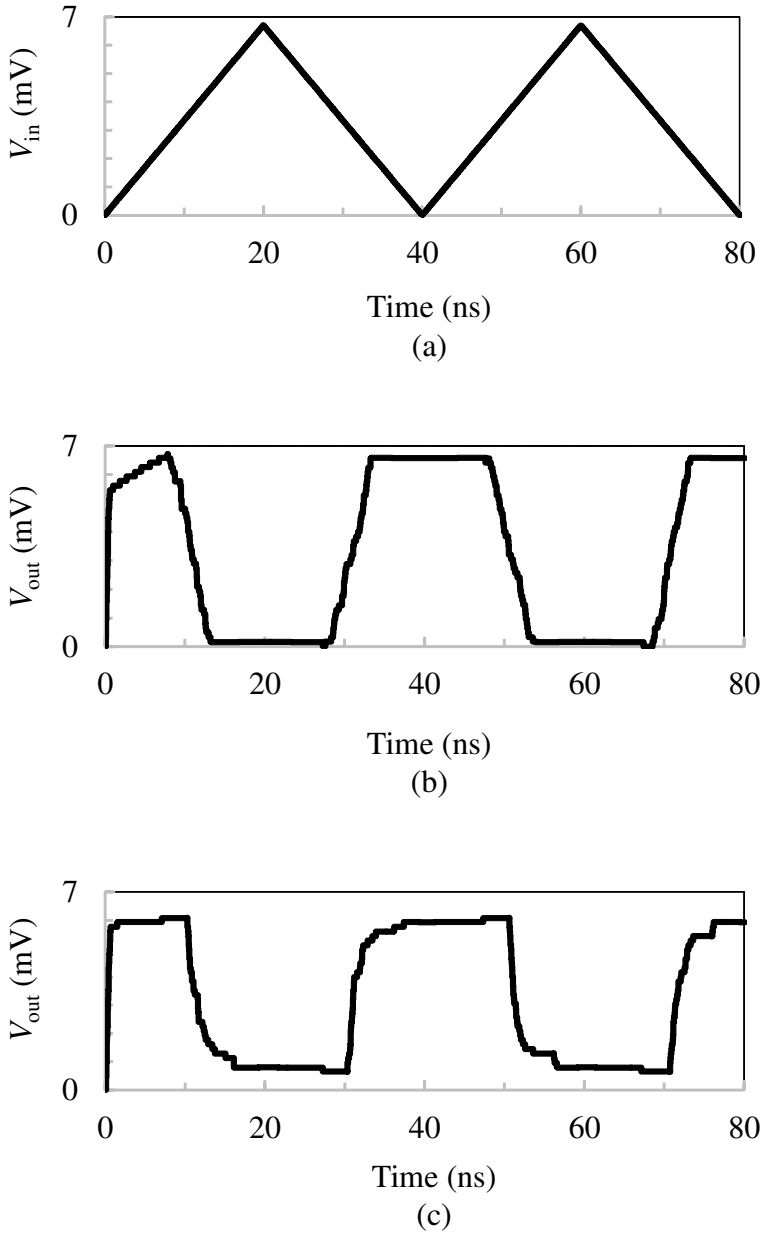


Figure 2.6: Dynamic characteristics of the solo FJI and the ID-FJI at $T = 0$ K. (a) Transient input voltage. (b) Transient output voltage of the solo FJI. (c) Transient output voltage of the ID-FJI.

to operate well in continuous time due to two following points. Firstly, the result obeys the principle of an inverter where the states of the output signal is inverse to those of the input signal. Secondly, the sharp switching is always

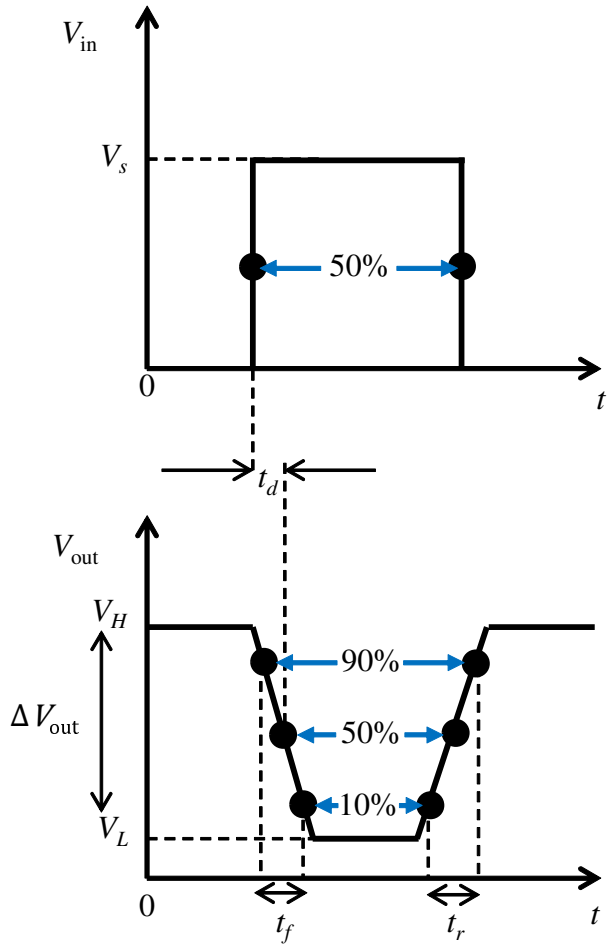


Figure 2.7: Schematic drawing of waveforms for analyzing the switching characteristics of an inverter.

obtained in the output. Therefore, the ID-FJI has possibility of achiving the sharp switching without an ideal square input signal.

Figure 2.7 shows a schematic drawing of waveforms for analyzing the switching characteristics of an inverter [62]. The input signal V_{in} is assumed as a square pulse with the amplitude V_s. Then, 50% of the input signal is given by

$$V_{\mathrm{in}}(50\%) = V_s/2. \tag{2.11}$$

The output signal V_{out} has two levels including high level V_H and low level V_L.

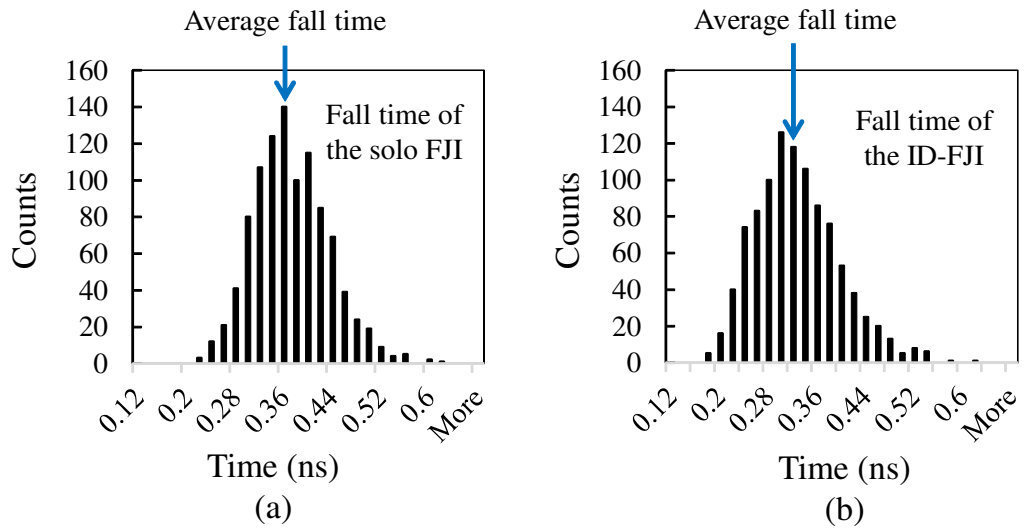


Figure 2.8: Histograms describe fall times of the output voltages of the solo FJI and the ID-FJI.

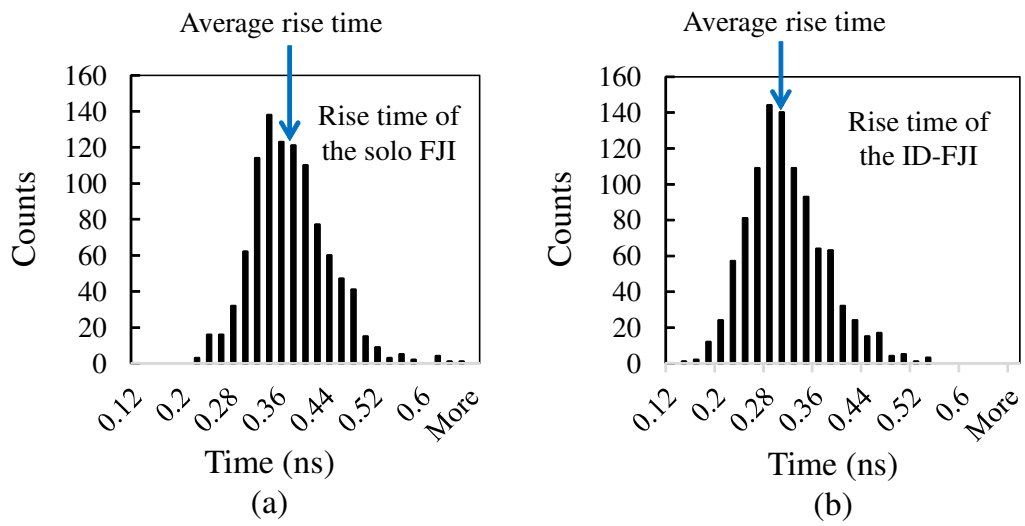


Figure 2.9: Histograms describe rise times of the output voltages of the solo FJI and the ID-FJI.

The difference between two output levels is estimated as

$$\Delta V_{\text{out}} = V_H - V_L. \tag{2.12}$$

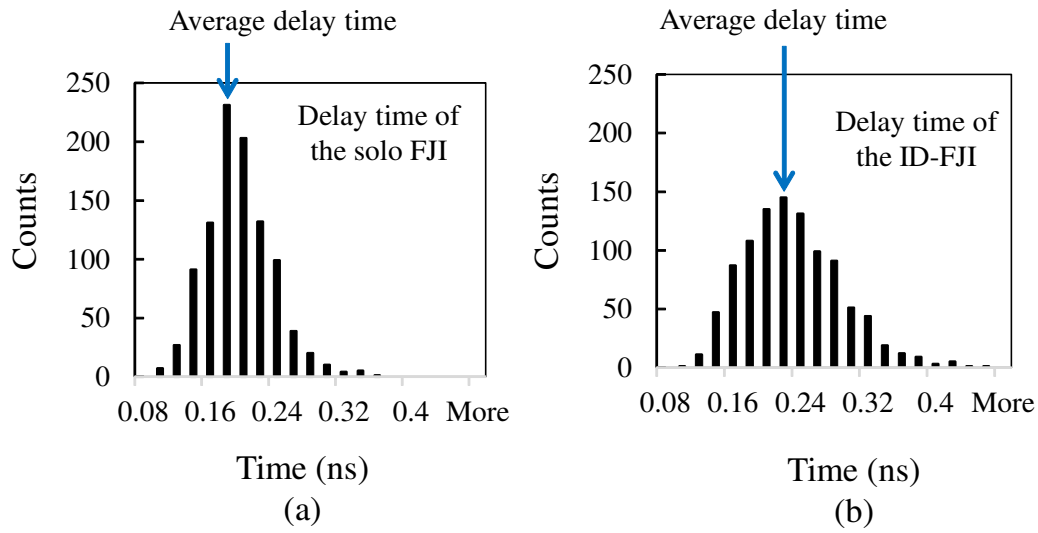


Figure 2.10: Histograms describe delay times between the input and output voltages of the solo FJI and the ID-FJI.

The output signals at 10%, 50%, and 90% of the logic level difference are respectively calculated as

$$V_{\text{out}}(10\%) = V_L + 10\%\Delta V_{\text{out}}, \tag{2.13}$$

$$V_{\text{out}}(50\%) = V_L + 50\%\Delta V_{\text{out}}, \tag{2.14}$$

$$V_{\text{out}}(90\%) = V_L + 90\%\Delta V_{\text{out}}. \tag{2.15}$$

Time parameters are defined similar to the previous work [62] as follows. Fall time t_f of the output signal is the time that the output signal falls from $V_{\text{out}}(90\%)$ to $V_{\text{out}}(10\%)$. Rise time t_r of the output signal is the time that the output signal rises from $V_{\text{out}}(10\%)$ to $V_{\text{out}}(90\%)$. Delay time is the time difference between the time at $V_{\text{in}}(50\%)$ and the time at $V_{\text{out}}(50\%)$. To describe the switching characteristics of the solo FJI and the ID-FJI, historgrams were made on the basis of 1000 transient simulations using an ideal square input pulse in the conditions of 0 K and no cotunneling processes.

2.3. Improvement of single-electron four-junction inverter (SE FJI) using input discretizer (ID)

The fall times of the solo FJI and the ID-FJI are illustrated in Figs. 2.8(a) and (b), respectively. The average fall time (shown by the arrow) of the ID-FJI is 0.04 ns shorter than that of the solo FJI. In the fall state of the output signal, an increase of the input signal from 0 mV to V_s makes the lower part of the solo FJI (SET2) turn on. Simulation for the SET2 shows the on-state fall resistance $R_{\text{on_fall}}$ of 426 kΩ. Hence, the fall time of the ID-FJI is calculated as 0.32 ns $\approx 0.75 R_{\text{on_fall}} C_{\text{out}}$ whereas that of the solo FJI is estimated as 0.36 ns $\approx 0.84 R_{\text{on_fall}} C_{\text{out}}$. In other words, to change the state of the output from high to low, the ID-FJI switches $0.09 R_{\text{on_fall}} C_{\text{out}}$ faster than the solo FJI. Therefore, if the input signal is an ideal square pulse (For the ideal square pulse, the transition between high and low input levels is instaneous. In fact, the ideal square pulse is not realizable in physical system), the improvement of the ID-FJI in the falling state is insignificant in comparison with the solo FJI.

The rise time of the solo FJI and the ID-FJI are shown in Figs. 2.9(a) and (b), respectively. The average rise time (shown by the arrow) of the ID-FJI is 0.07 ns less than that of the solo FJI. In the rise state of the output signal, a decrease of the input signal from V_s to 0 mV causes the upper part of the solo FJI (SET1) switch on. Simulation for the SET1 indicates the on-state rise resistance $R_{\text{on_rise}}$ of 434 kΩ. Therefore, the rise time of the ID-FJI is evaluated as 0.30 ns $\approx 0.69 R_{\text{on_rise}} C_{\text{out}}$ while that of the solo FJI is calculated as 0.37 ns $\approx 0.85 R_{\text{on_rise}} C_{\text{out}}$. In other words, to change the state of the output from low to high, the ID-FJI switches $0.16 R_{\text{on_rise}} C_{\text{out}}$ faster than the solo FJI. Hence, in the rising state, if the input signal is an ideal square pulse, there is a little improvement of the ID-FJI in comparison with the solo FJI.

Figures 2.10(a) and (b) illustrate the delay times of the solo FJI and the ID-FJI. The average delay time of the ID-FJI is 0.04 ns longer than that of the solo FJI. This situation arises from the addition of the ID, which makes the logic transition from the input to the output of the ID-FJI longer than that of the solo FJI.

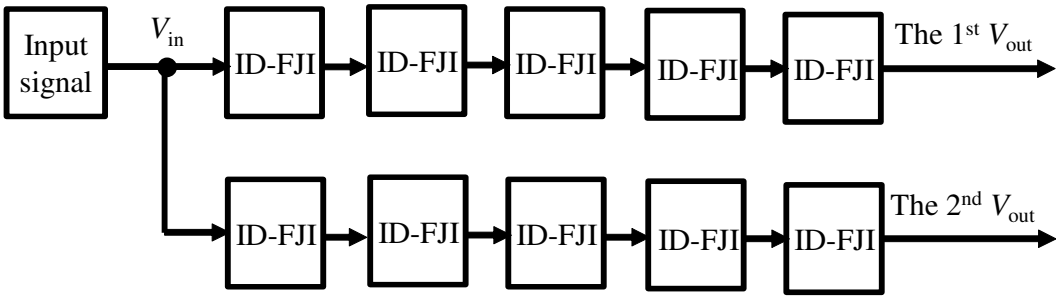


Figure 2.11: Block diagram of a parallel two-branch circuit which consists of 5 ID-FJIs in series on each branch.

2.3.4 Parallel two-branch array of the ID-FJIs

To evaluate the ability of combination of the ID-FJIs, the ID-FJIs are connected to each other in series and parallel. Then, in the serial connection, the output signal is compared to the input signal to determine whether the ID-FJI still works as an inverter; in the parallel connection, output signals are compared to each other to determine whether the operations of the parallel branches are equivalent. We simulated the circuit shown in Fig. 2.11, where a parallel two-branch circuit contains the five serially-cascaded ID-FJIs on each branch. Simulation was implemented with following conditions: $T = 0$ K; no cotunneling processes; the triangle input signal (Fig. 2.12(a)). The first output voltage (1st V_{out}) and the second output voltage (2nd V_{out}) are described as in Figs. 2.12(b) and (c), respectively.

It is clear that the operation of the circuit follows the principle of a digital inverter since number of ID-FJIs on each branch is odd. Firstly, on each branch, the output voltage is in inverse relation to the input voltage (in other words, the high output voltage corresponds to the low input voltage and vice versa). Secondly, the outputs of two parallel branches, 1st V_{out} (Fig. 2.12(b)) and 2nd V_{out} (Fig. 2.12(c)), are the same.

Two advantages of the circuit can be obtained as follows. The sharp switching between the high and low output levels is still ensured when the ID-FJIs are connected to each other. In addition, the high and low output levels are

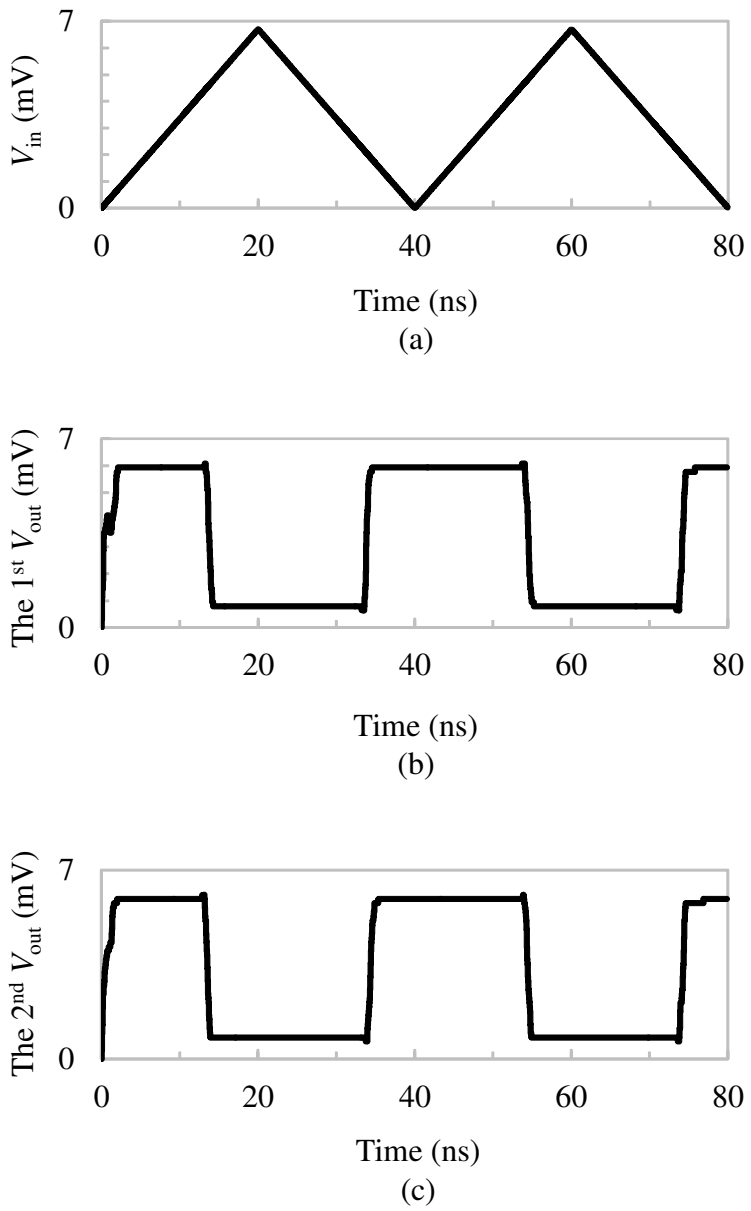


Figure 2.12: Dynamic characteristics of the parallel two-branch circuit of the ID-FJIs. (a) Input voltage V_{in}. (b) The first output voltage (1st V_{out}). (c) The second output voltage (2nd V_{out}).

stable, resulting in stable states during the operation process of the circuit.

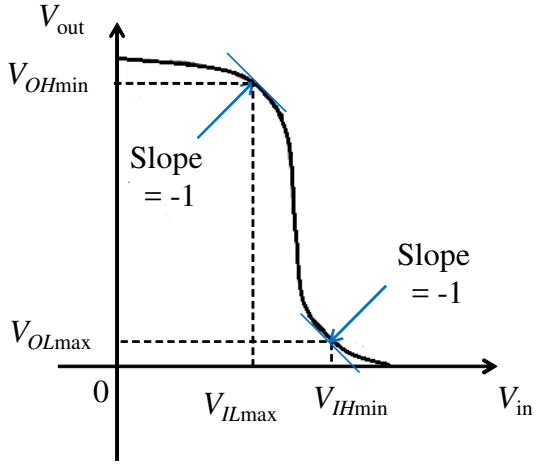


Figure 2.13: Schematic drawing for determining noise margin of an inverter.

2.3.5 Margins of capacitances

Values of the capacitances in the ID-FJI affect its input-output voltage characteristics. Since the noise margin is an important parameter for evaluating the input-output characteristics [61], it is used as a criterion to determine the capacitance margins of the ID-FJI. Figure 2.13 shows a schematic drawing for determining the noise margin of an inverter [61]. In Fig. 2.13, $V_{IL\max}$ and $V_{IH\min}$ are respectively the maximum low input voltage and the minimum high input voltage; $V_{OL\max}$ and $V_{OH\min}$ are respectively the maximum low output voltage and the minimum high output voltage. ($V_{IH\min}$, $V_{OL\max}$) and ($V_{IL\max}$, $V_{OH\min}$) are the first and the second points where the slope becomes -1 for V_{in} decreasing from V_s to 0 [61].

The noise margin is characterized by two terms including the low noise margin NM_L and the high noise margin NM_H. Definitions of these terms are the same as in the previous literature [61]. NM_L is the difference in magnitude between $V_{IL\max}$ and $V_{OL\max}$ as follows,

$$NM_L = |V_{IL\max} - V_{OL\max}|. \tag{2.16}$$

Table 2.1: Capacitance margins in the ID-FJI

Capacitances	Origin (aF)	Margins (aF)	
		Minimum	Maximum
C_0 (J_0)	1	1×10^{-4}	100
C_{01}	72	58	79
C_1 (J_2, J_3)	2	0.90	5.3
C_2 (J_1, J_4)	1	1×10^{-4}	19
C_G	8	7.2	18
C_B	7	6.6	9.8
C_{out}	10^3	30	5×10^5

NM_H is the difference in magnitude between $V_{IH\text{min}}$ and $V_{OH\text{min}}$ as follows,

$$NM_H = |V_{IH\text{min}} - V_{OH\text{min}}|. \tag{2.17}$$

NM_L and NM_H should be larger than a minimum threshold voltage V_{min} to avoid switching errors induced by the noise on the input [61]. The value of V_{min} is chosen on the basis of the specific application of the circuit. Here, we chose $0.1V_s$ as an example of V_{min} to determine the capacitance margins of the ID-FJI. We simulated input-output characteristics of the ID-FJI with different capacitances under the conditions of 0 K and no cotunneling. NM_L and NM_H calculated from the input-output characteristics. The capacitance ranges were chosen so that both NM_L and NM_H are larger than $0.1V_s$. The capacitance margins obtained numerically are summarized in Table 2.1. In Table 2.1, the "Origin" column lists the original values of the capacitances which were described in Sects. 2.3.1 and 2.3.2; the "minimum" and "maximum" columns are respecitvely the possibly minimum and maximum values of the capacitances. The margins of C_0 and C_{out} are wider than the others since the switching curve of the ID-FJI mainly depends on the C_{01} of the ID (according to Eq. (2.10))

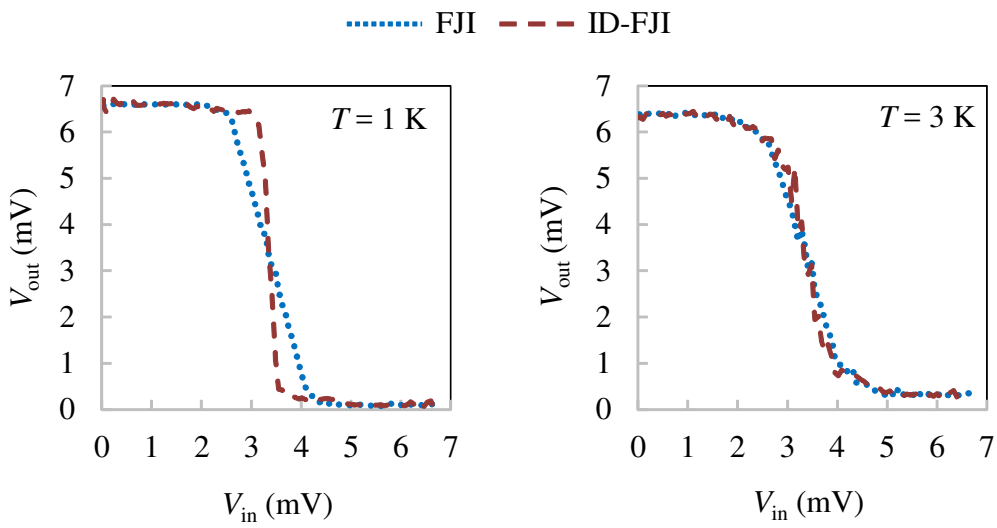


Figure 2.14: Input-output voltage characteristics of the solo FJI and the ID-FJI at finite temperatures. (a) $T = 1$ K. (b) $T = 3$ K.

and parameters of two SETs in the FJI (as illustrated in Eq. (32) of Ref. [29]).

2.3.6 Limiting operation temperature

One of the important parameters affects the operation of SE devices is the temperature. To avoid thermal fluctuation which can smear out Coulomb blockade states, SE devices are usually operated at temperatures where the condition of $k_B T \ll E_C$ is satisfied [25]. The charging energy in the ID (Fig. 2.1) can be calculated as

$$E_C = \frac{e^2}{2(C_0 + C_{01} + C_{02} + C_{03})}. \tag{2.18}$$

Using the parameters of the ID in Sect. 2.3.2: $C_0 = 1$ aF, $C_{01} = 72$ aF, $C_{02} = C_{03} = C_G = 8$ aF, a ratio $(E_C/k_B)_{\text{limit}}$ is calculated to be 10.4 K.

Input-output characteristics of the solo FJI and the ID-FJI at finite temperatures are respectively illustrated by dotted and dashed curves in Fig. 2.14. At $T = 1$ K (Fig. 2.14(a)), the switching of the ID-FJI is still sharper than

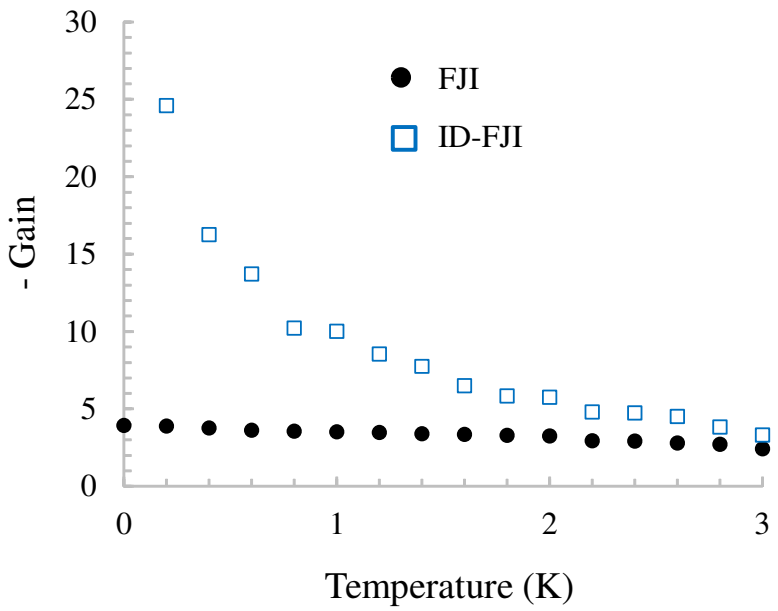


Figure 2.15: Gain characteristics of the solo FJI and the ID-FJI at different temperatures.

that of the solo FJI. However, at $T = 3$ K (Fig. 2.14(b)), the switching of the ID-FJI has the same slope as that of the solo FJI. Therefore, when the temperature increases, the switching of the ID-FJI gradually approaches to that of the solo FJI.

To compare the effect of temperature on the input-output characteristics of the solo FJI and the ID-FJI, gain characteristics are used as an evaluation parameter. The gain is defined as the $(V_{OL\max} - V_{OH\min})/(V_{IH\min} - V_{IL\max})$ (Fig. 2.13). $(V_{IH\min}, V_{OL\max})$ and $(V_{IL\max}, V_{OH\min})$ are determined on $V_{\text{in}} - V_{\text{out}}$ characteristics which are obtained from simulating the solo FJI and the ID-FJI at different temperatures and no cotunneling. Figure 2.15 shows the gain characteristics of the solo FJI and the ID-FJI which are respecitvely represented by solid circles and open squares. They exhibit a downward trend when the temperature increases. It can be seen that at very low temperatures ($T \leq 1$ K), the absolute gain of the ID-FJI, $|G|_{\text{ID-FJI}}$, is much greater than that of the solo FJI, $|G|_{\text{FJI}}$, since 1 K is equivalent to $0.1(E_C/k_B)_{\text{limit}}$. Namely, under

$T = 1$ K, the ratio $|G|_{\text{ID-FJI}}/|G|_{\text{FJI}}$ is larger than 2. However, the absolute gain of the ID-FJI reduces to that of the solo FJI at 3 K. Hence, $T = 3$ K corresponding to $0.3(E_C/k_B)_{\text{limit}}$ is the limiting operation temperature above which the ID in the ID-FJI has no advantage from the gain viewpoint.

2.4 Improvement of single-electron NAND gate using input discretizers (ID-NAND)

2.4.1 Characteristics of single-electron NAND gate

Figure 2.16 shows a schematic diagram of an SE NAND gate [30]. Two input signals V_{in1} and V_{in2} are applied to the NAND gate. Source voltage V_s is supplied to the NAND gate. The output signal V_{out} is the voltage on the output capacitor C_{out}. The NAND gate is composed of two upper SETs (SET1 and SET2) in parallel between V_s and V_{out}, and two lower SETs (SET3 and SET4) in series between V_{out} and ground. To avoid fluctuations in the output voltage, both capacitances C_{out} and C_L should be chosen to be large enough [30].

Parameters of the NAND gate are similar to those in the previous literature: $C_1 = 2C_2$, $C_G = 8C_2$, $C_B = 7C_2$, $C^* = C_1 + C_2 + C_G + C_B$, $V_s = 1.5e/2C^*$ [30]. On the basis of these capacitance relationships, we set a typical value of C_2, $C_2 = 1$ aF, and calculate the other capacitances. Then, in the numerical simulation below, the parameters were assumed as: $C_1 = 2$ aF, $R_1 = 50$ kΩ, $C_2 = 1$ aF, $R_2 = 100$ kΩ, $C_G = 8$ aF, $C_B = 7$ aF, $C_L = C_{\text{out}} = 1$ fF, and $V_s = 6.7$ mV. Simulations were executed in the conditions of 0 K and no cotunneling.

Input-output characteristics of the NAND gate are described in 3-D splot (Fig. 2.17(a)) and 2-D plot (Fig. 2.17(b)). Again, definitions of logic levels are as follows: logic "1" equivalent to the high voltage level; logic "0" corresponding to the low voltage level. When the input vector $[V_{\text{in1}}\ V_{\text{in2}}]$ changes from [0 1] to [1 1], the output V_{out} switches from logic "1" to logic "0" via a sloping region in Fig. 2.17(a) or a gradual change of colors from yellow to black in Fig. 2.17(b). This area expands from V_{in1} of 2.7 mV to 4.1 mV, which occupies

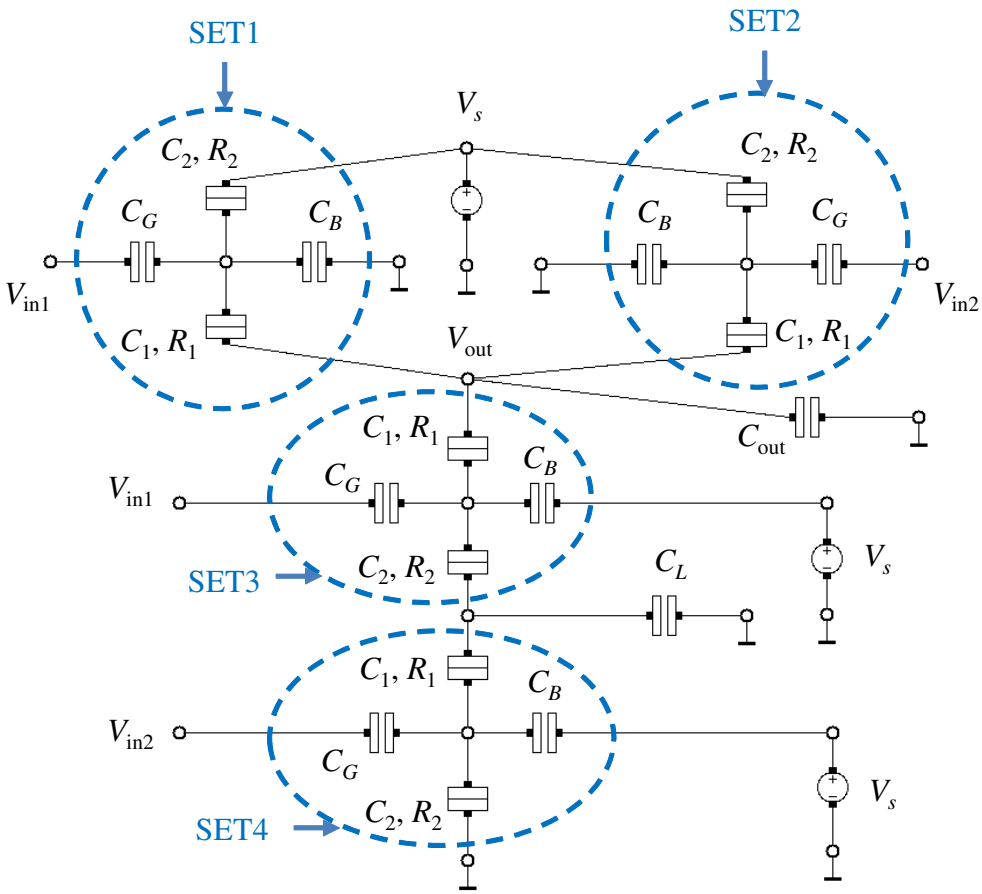
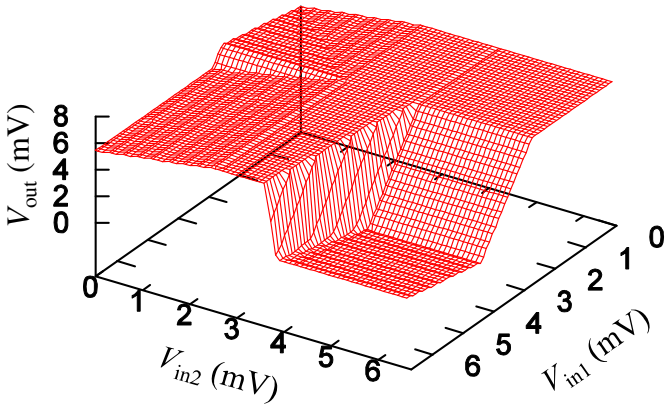
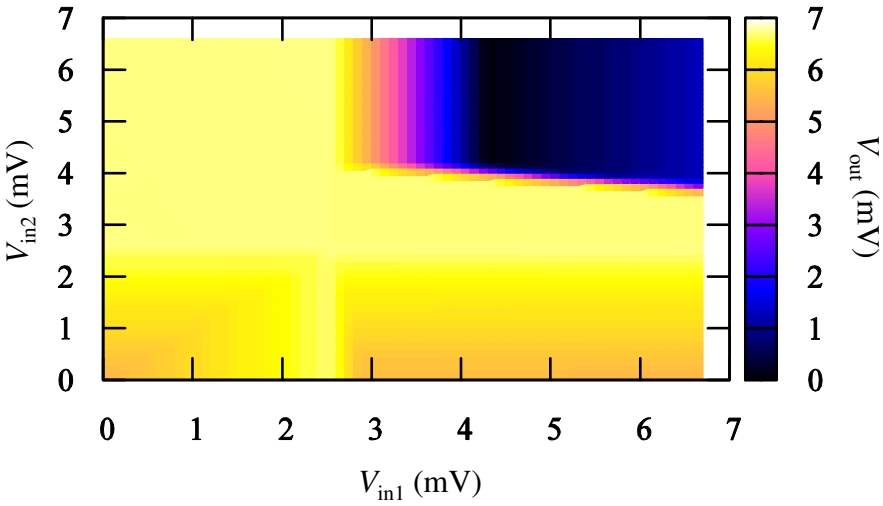


Figure 2.16: Schematic diagram of single-electron NAND gate.

$(4.2 - 2.7) \times 100\%/6.7 \approx 22.39\%$ of the input voltage range (V_{in} from 0 to 6.7 mV). Similarly, when the input vector $[V_{in1}\ V_{in2}]$ changes from [1 0] to [1 1], V_{out} gradually switches from logic "1" to logic "0" in the region from V_{in2} of 3.6 mV to 4.2 mV. This region corresponds to $(4.2 - 3.6) \times 100\%/6.7 \approx 8.96\%$ of the input voltage range. As a result, in these transition regions, the output of the NAND gate is not well-determined, resulting in unclear decisions about the output states. This drawback is the same as that of the solo FJI. Hence, operation of the NAND gate is also improved by the addition of the IDs.



(a)



(b)

Figure 2.17: Input-output characteristics of the SE NAND gate. (a) 3-D splot. (b) 2-D plot.

2.4.2 Improvement of single-electron NAND gate using input discretizers (ID-NAND)

Combination of the NAND gate with the IDs into ID-NAND configuration is illustrated in Fig. 2.18. Because the NAND gate has two inputs, two IDs (ID1 and ID2) are added between the inputs and the main device NAND gate.

The structures of the ID1 and the ID2 are similar to those in Fig. 2.1. The ID1 consists of one junction J_{01}, one grounded capacitor C_{01}, and two output capacitors. The ID2 is composed of one junction J_{02}, one grounded capacitor C_{01}^*, and two output capacitors. Here, the output capacitors of the ID1 and the ID2 play the role of the gate capacitors (C_G) of the NAND gate.

Since the ID-NAND and the ID-FJI devices have the same structure of the ID, the threshold voltages for tunneling through the junctions in the ID1 and the ID2 can be calculated using Eq. (2.10). Then, threshold voltages of the ID1 and the ID2 are respectively in the form of

$$V_{\mathrm{inT1}} = \frac{(N_1 + 1/2)e + C_G(V_2 + V_3)}{C_{01} + 2C_G}, \tag{2.19}$$

$$V_{\mathrm{inT2}} = \frac{(N_2 + 1/2)e + C_G(V_2^* + V_3^*)}{C_{01}^* + 2C_G}, \tag{2.20}$$

in which N_1 and N_2 are the number of exess electrons on the center islands of the ID1 and the ID2, respectively; V_2 and V_3 are the output voltages of the ID1; V_2^* and V_3^* are the output voltages of the ID2. When the tunneling events through J_{01} and J_{02} cause the switches between the output logic levels of the ID-NAND, V_{inT1} and V_{inT2} are called V_{inS1} and V_{inS2} (the switching threshold voltages). Because V_{inS1} and V_{inS2} depend on C_{01} and C_{01}^* according to Eqs. (2.19) and (2.20), values of C_{01} and C_{01}^* must be adjusted to make V_{inS1} and V_{inS2} as close to $(V_{\mathrm{T}})_{\mathrm{Std}}$ as possible. In addition, for simplicity, tunnel capacitances and resistances of the J_{01} and J_{02} are assumed to be the same as those of the tunnel junction (C_2, R_2) in the NAND. The appropriate parameters were chosen in the simulation as follows: ID1 ($C_0 = 1$ aF, $R_0 = 100$ kΩ, $C_{01} = 67$ aF), ID2 ($C_0 = 1$ aF, $R_0 = 100$ kΩ, $C_{01}^* = 66$ aF). The output capacitances of the ID1 and the ID2 are 8 aF since $C_G = 8$ aF.

The switching threshold voltages are calculated as follows. In the transition, the sum of the output voltages of the ID2 (Fig. 2.18), $V_2^* + V_3^*$, is approximately V_s because the tunnel junction between V_s and V_2^* and the tun-

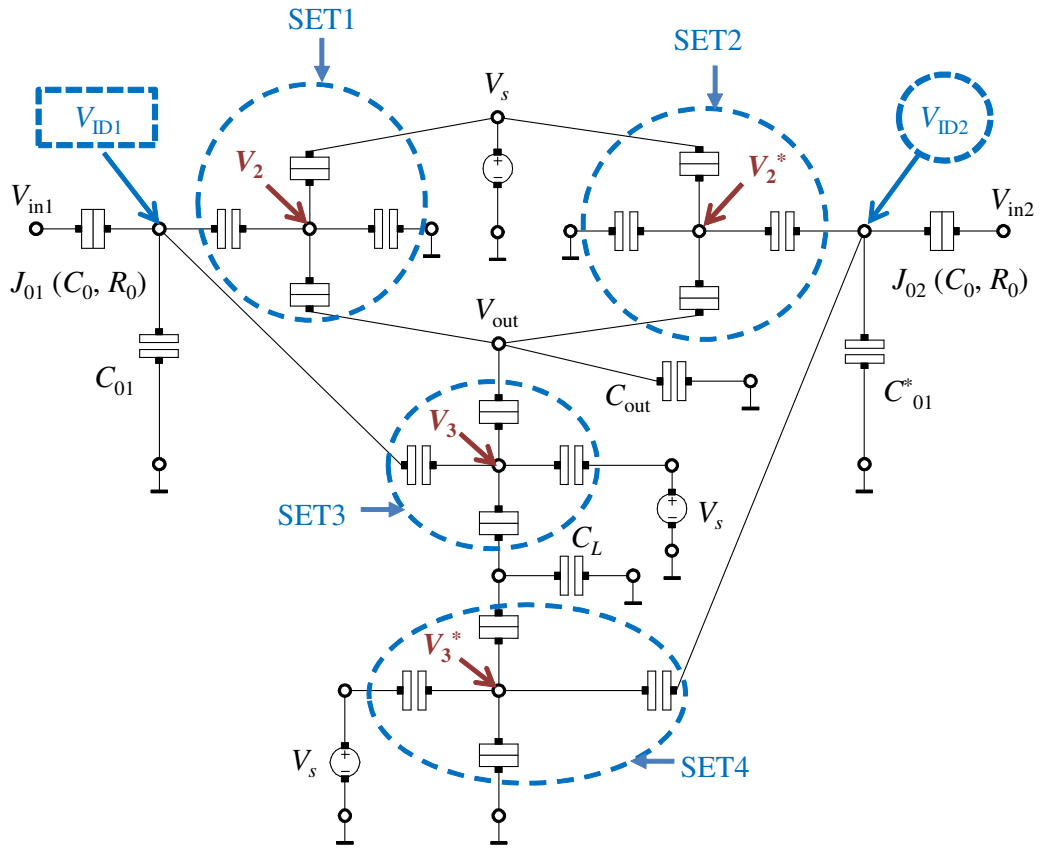


Figure 2.18: Schematic diagram of SE NAND gate with two IDs (ID-NAND).

nel junction between V_3^* and ground have the same parameters (C_2, R_2). In Fig. 2.18, the capacitance C_L is much larger than the other capacitances except C_{out}, then V_3 is approximately V_3^*. In addition, $V_2 \approx V_2^*$ since the SET1 is parallel to SET2 (Fig. 2.18). As a result, in the transition region, the sum of the output voltages of the ID1, $V_2 + V_3$, is approximately V_s. Substituting above parameters into Eqs. (2.19) and (2.20), the calculated switching threshold voltages, $(V_{\text{inS1}})_{\text{cal}}$ and $(V_{\text{inS2}})_{\text{cal}}$, for tunneling from $N_i = 1$ to $N_i = 2$ ($i = 1, 2$) are estimated as 3.54 mV and 3.58 mV, respectively.

Simulation was implemented in the conditions of 0 K and no cotunneling. Input-output characteristics of the ID-NAND device are illustrated by 3-D splot and 2-D plot in Figs. 2.19(a) and (b), respectively. When the input vector [V_{in1} V_{in2}] changes from [0 1] to [1 1], a sharp switching from logic "1" to logic

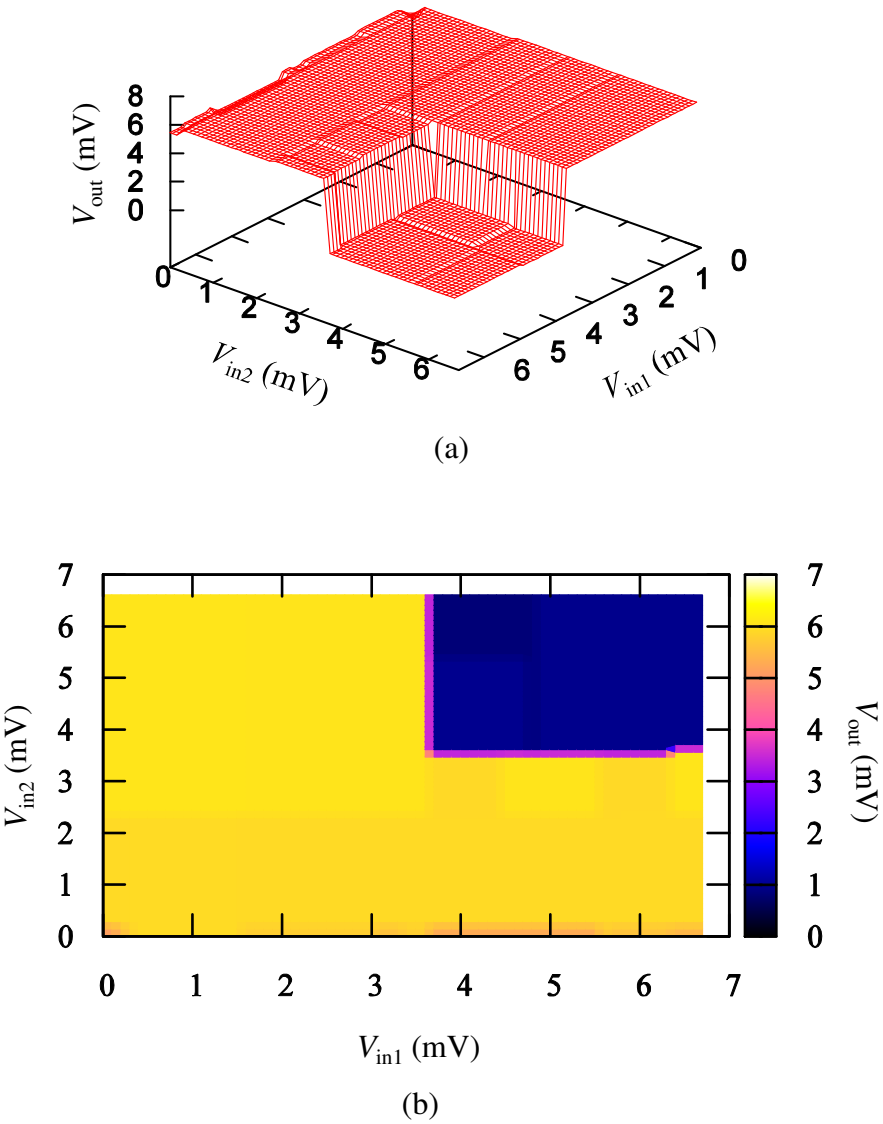


Figure 2.19: Input-output characteristics of the ID-NAND. (a) 3-D splot. (b) 2-D plot.

"0" of the output is observed at $(V_{\mathrm{inS1}})_{\mathrm{sim}}$ of 3.6 mV. Similarly, when the input vector $[V_{\mathrm{in1}}\ V_{\mathrm{in2}}]$ changes from [1 0] to [1 1], a sharp switching from logic "1" to logic "0" of the output appears at $(V_{\mathrm{inS2}})_{\mathrm{sim}}$ of 3.5 mV. Thus, the calculated threshold voltages, $(V_{\mathrm{inS1}})_{\mathrm{cal}}$ and $(V_{\mathrm{inS2}})_{\mathrm{cal}}$, are in the reasonable agreement with the simulated threshold voltages, $(V_{\mathrm{inS1}})_{\mathrm{sim}}$ and $(V_{\mathrm{inS2}})_{\mathrm{sim}}$. Besides, since

the NAND gate has two inputs, the objective to achieve the sharp switches with the switching threshold voltages close to $(V_{\mathrm{T}})_{\mathrm{Std}}$ becomes more complicated than the ID-FJI device. Hence, the difference between $(V_{\mathrm{inSi}})_{\mathrm{sim}}$ (i = 1, 2) of the ID-NAND and $(V_{\mathrm{T}})_{\mathrm{Std}}$ is larger than the difference between $(V_{\mathrm{inS}})_{\mathrm{sim}}$ of the ID-FJI and $(V_{\mathrm{T}})_{\mathrm{Std}}$.

The switching regions between the high and low output levels of the ID-NAND are calculated as follows. When vector $[V_{\mathrm{in1}}\ V_{\mathrm{in2}}]$ changes from [0 1] to [1 1], the switching region appears from 3.6 mV to 3.7 mV, which occupies $(3.7 - 3.6) \times 100\%/6.7 \approx 1.49\%$ of the input voltage range (V_{in} from 0 to 6.7 mV). When vector $[V_{\mathrm{in1}}\ V_{\mathrm{in2}}]$ changes from [1 0] to [1 1], the switching region appears from 3.5 mV to 3.7 mV, which corresponds to $(3.7-3.5)\times 100\%/6.7 \approx 2.99\%$ of the input voltage range. In comparison with the switching regions of the NAND gate which are calculated in Sect. 2.4.1, the switching regions of the ID-NAND are reduced to 0.33 times.

2.5 Conclusion

With the addition of the IDs, the characteristics of the SE logic gates including SE inverter and NAND gates were enhanced. The input-output characteristics of the ID-FJI exhibit the sharp switching instead of the gradual switching as in the solo FJI. The transition region of the ID-FJI is reduced to 0.011 times that of the solo FJI. In dynamic characteristics, the average switching times (the fall and rise times) of the ID-FJI are shorter than those of the solo FJI. For the parallel two-branch circuit of the serially-cascaded ID-FJIs, the ID-FJIs still operate well, which is prospective for the possibility of integration of the ID-FJIs. The capacitance margins of the ID-FJI were also determined numerically from the criterion of the noise margin. From the viewpoint of gain, the operation of the ID-FJI is better than that of the solo FJI under 1 K ($\sim 0.1(E_C/k_B)_{\mathrm{limit}}$) and same as that of the solo FJI at the limiting temperature of 3 K ($\sim 0.3(E_C/k_B)_{\mathrm{limit}}$). Besides, the ID-NAND achieves the sharp switches between the high and low output levels. The transition regions of the ID-

NAND are decreased to 0.33 times those of the solo NAND. On the whole, the nonlinear characteristics of the SE inverter and SE NAND gates can be improved by adding the IDs.

Chapter 3

Improvement of stochastic resonance by designing a single-electron hysteretic inverter

3.1 Introduction

Stochastic resonance (SR) has been attracted a large variety of researches. SR is a nonlinear phenomenon whereby the addition of noise can enhance the detectability of a weak signal [63]. This phenomenon requires three fundamental ingredients including a form of threshold, a weak coherent input and a source of noise [64]. With these ingredients, the response of the system versus the noise level behaves like a resonance curve. Namely, the enhancement of the detectability is the best at a sufficient noise level which is called the optimal noise level, whereas it degrades if the noise level increases further [63]. SR does not appear in the strictly linear systems where the additon of noise only degrades the quality of the signal [63]. SR has been applied in many systems such as nonlinear optics, solid state devices, and neurophysiology [64]. These systems can be divided into the continuous systems (e.g the double-well system) and the discrete systems (e.g the two-state system).

On the one hand, one of the interesting characteristics which realizes stochastic resonance well is the hysteretic characteristic [65, 66]. The hysteresis has a range of the input for which the circuit is bistable. For realization of stochastic resonance, the switching time of the hysteresis is required to be fast enough, that is, the hysteresis has sharp switches between output states.

On the other hand, SE devices with advantages of nanoscales and low power consumption have become prospective candidates for many applications [25]. SR has been studied in the fields of nanometer-scale electronics including SE devices [67, 68]. One example is a neural network of SE boxes where the SR phenomenon was confirmed in the condition of thermal noise [68].

In this study, stochastic resonance is investigated in another SE device that is an SE inverter. Evaluation of stochastic resonance in the inverter shows the improvement of the hysteretic inverter in comparison with the non-hysteretic inverter from the viewpoint of correlation coeffient CC. Moreover, CC is better if the width of the hysteresis is wider. Therefore, an SE hysteretic inverter with a wide hysteresis is designed to improve stochastic resonance.

On the other hand, the previous work [69] introduced an SE device which exhibited the hysteretic characteristics by combining two serially-cascaded IDs and an SE transistor. Hence, there is possibility that the combination of two serially-cascaded IDs with the SE non-hysteretic inverter (SE FJI [29]) (2ID-FJI) can make a hysteretic inverter. In addition, the ID discretizes the continuous input signal into the discrete output signal [31], so the switches of the hysteresis are expected to be sharp.

In comparison with the SE hysteretic device in the previous work [69], the 2ID-FJI discussed in this chapter has four significant differences as follows. Firstly, the main device is the FJI instead of SE transistor. Secondly, the output of the 2ID-FJI is the voltage but not the current. Thirdly, the numbers of excess electrons on the center islands of two IDs are determined by numerical simulation but not assumed to be 0 or 1. Finally, parameters of the IDs are designed to obtain a wide hysteresis. Stochastic resonance is significantly improved by using the 2ID-FJI, which is better than stochastic resonance in the

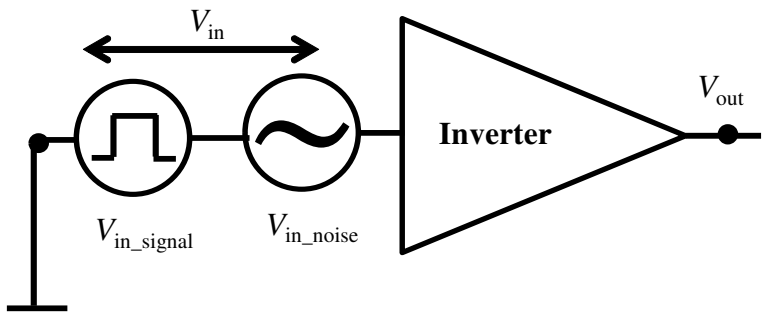


Figure 3.1: Model uses an inverter for stochastic resonance.

FJI and equivalent to that in the ideal hysteretic inverter from the viewpoint of CC.

3.2 Method for improvement of stochastic resonance

Stochastic resonance phenomenon in an inverter is evaluated by using a model as shown in Fig. 3.1. The inverter has a noisy input signal $V_{\rm in}$ and an output signal $V_{\rm out}$. $V_{\rm in}$ includes an input signal $V_{\rm in_signal}$ and an input noise $V_{\rm in_noise}$.

Definitions of some parameters discussed in this chapter as follows. The input signal is a unipolar rectangular wave with an ampitude $V_{\rm in_signal}$ (low level $V_{\rm in_signal_low} = 0$, high level $V_{\rm in_signal_high} = V_{\rm in_signal}$) and a period $T_s =$ 200 ns (frequency $f_s = 1/T_s = 5$ MHz). The input noise is a pseudo-random white noise has uniform distribution in a range from $-V_{\rm in_noise}/2$ to $+V_{\rm in_noise}/2$. $V_{\rm in_noise}$ is called the noise level. The input noise has a discretized step $\Delta t = 1$ ns. The noisy input signal $V_{\rm in}$ is expressed as the sum of $V_{\rm in_signal}$ and $V_{\rm in_noise}$, that is, $V_{\rm in} = V_{\rm in_signal} + V_{\rm in_noise}$.

Schematic drawings of $V_{\rm in_signal}$, $V_{\rm in}$, and $V_{\rm out}$ are illustrated in Figs. 3.2(a)−(c), respectively. A threshold voltage $V_{\rm th}$ is defined as a minimum voltage at which the output of an inverter responds to its input. $V_{\rm in_signal}$ is a subthreshold input signal which is less than $V_{\rm th}$. Without noise, $V_{\rm out}$ is always high since

$V_{\mathrm{in}}(= V_{\mathrm{in_signal}}) < V_{\mathrm{th}}$. With the sufficient addition of a noise source, at some instants when V_{in} crosses V_{th}, V_{out} switches from high to low level, i.e., the output responds to the input.

Characteristics of stochastic resonance are evaluated by using correlation coefficient CC between the input signal and the output signal. CC is in the form of

$$CC = \frac{\sum_{i=1}^{M} \left\{ \left[V_{\mathrm{in_signal}}(i) - \overline{V_{\mathrm{in_signal}}} \right] \left[V_{\mathrm{out}}(i) - \overline{V_{\mathrm{out}}} \right] \right\}}{\sqrt{\sum_{i=1}^{M} \left[V_{\mathrm{in_signal}}(i) - \overline{V_{\mathrm{in_signal}}} \right]^2} \sqrt{\sum_{i=1}^{M} \left[V_{\mathrm{out}}(i) - \overline{V_{\mathrm{out}}} \right]^2}} \tag{3.1}$$

in which,

$V_{\mathrm{in_signal}}(i)$ is the ith sample of the input signal;

$V_{\mathrm{out}}(i)$ is the ith sample of the output signal;

$\overline{V_{\mathrm{in_signal}}} = \dfrac{\sum_{i=1}^{M} V_{\mathrm{in_signal}}(i)}{M}$ is the averaged input signal;

$\overline{V_{\mathrm{out}}} = \dfrac{\sum_{i=1}^{M} V_{\mathrm{out}}(i)}{M}$ is the averaged output signal.

Because the output of an inverter is in inverse relation to its input, the ideal CC for an inverter is -1. The excellent CC are assumed to be less than -0.90.

An inverter is categorized into hysteretic or non-hysteretic inverter on the basis of whether or not its input-output characterisics exhibit a hysteresis. The inverter is assumed to be ideal, i.e., its switching between high and low output levels is sharp. The non-hysteretic inverter has input-output ($V_{\mathrm{in}} - V_{\mathrm{out}}$) characteristics as shown in Fig. 3.3. When the input voltage V_{in} is smaller than a threshold voltage V_{th}, the output voltage V_{out} is high; when $V_{\mathrm{in}} > V_{\mathrm{th}}$, V_{out} is low. The ideal hysteretic inverter has input-output characteristics as shown in Fig. 3.4. High and low threshold voltages, V_{H} and V_{L} ($V_{\mathrm{H}} > V_{\mathrm{L}}$), are defined as the threshold voltages for switching from the high output level to the low output level and vice versa. The ith sample of the output signal $V_{\mathrm{out}}(i)$ is

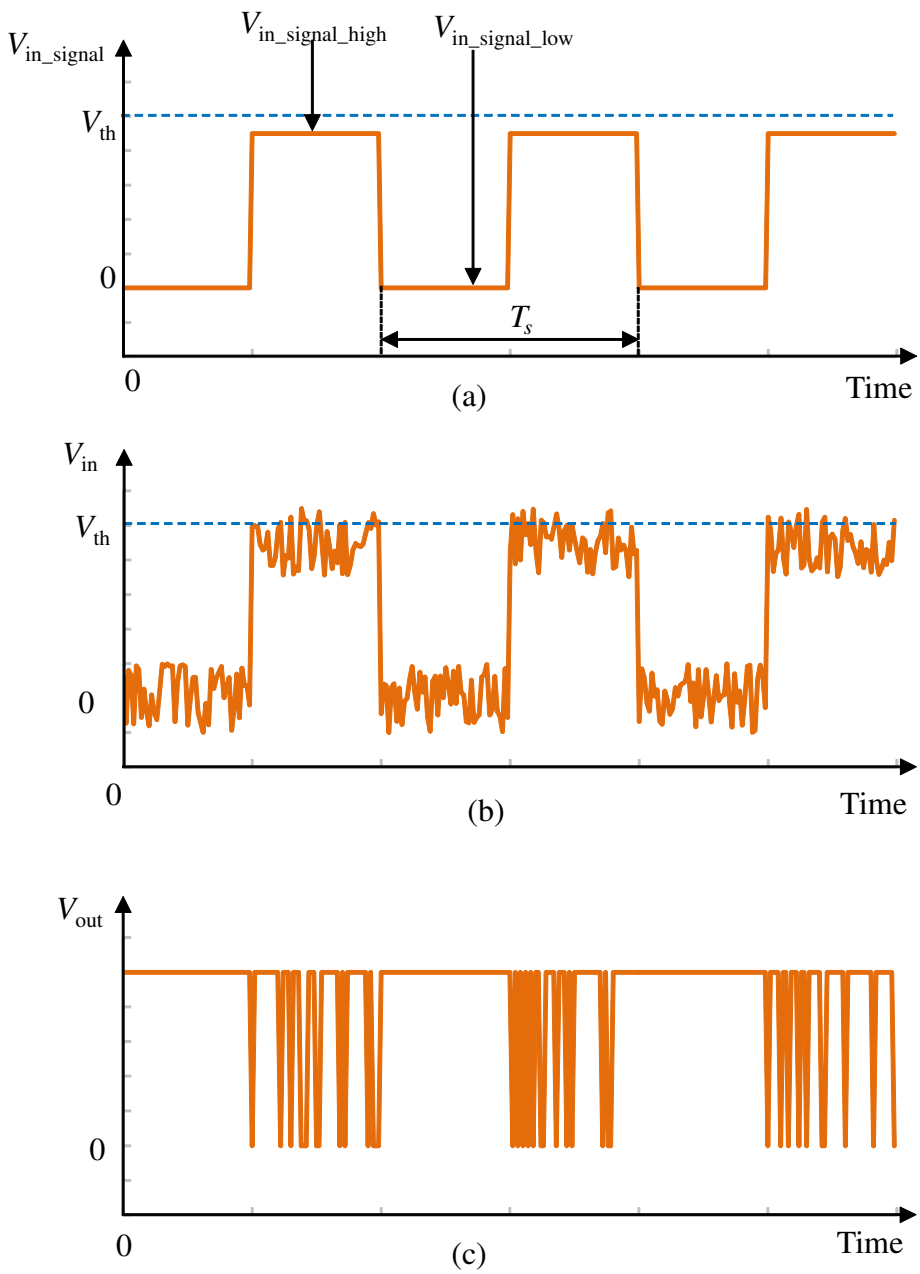


Figure 3.2: (a) Input signal is a unipolar rectangular wave with an amplitude V_{in_signal} (a high level $V_{in_signal_high}$ and a low level $V_{in_signal_low}$) and a period T_s. V_{in_signal} is a subthreshold input signal which is smaller than a threshold voltage V_{th}. (b) Noisy input signal V_{in} including V_{in_signal} and noise. (c) Output signal V_{out} of an inverter in stochastic resonance.

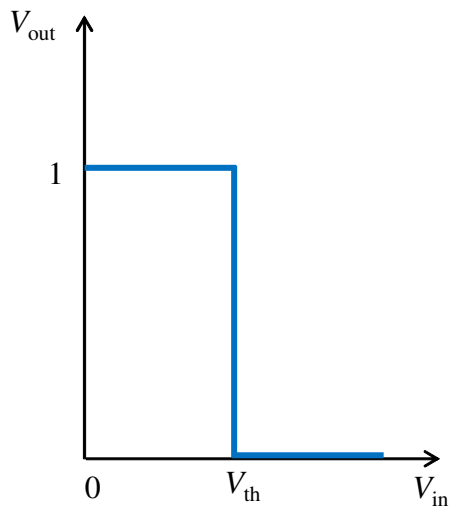


Figure 3.3: Input-output characteristics of an ideal non-hysteretic inverter.

expressed as follows,

$$V_{\mathrm{out}}(i) = \begin{cases} 0 & \text{if} \quad V_{\mathrm{in}}(i) \geq V_{\mathrm{H}} \\ V_{\mathrm{out}}(i-1) & \text{if} \quad V_{\mathrm{L}} < V_{\mathrm{in}}(i) < V_{\mathrm{H}} \\ 1 & \text{if} \quad V_{\mathrm{in}}(i) \leq V_{\mathrm{L}} \end{cases} \tag{3.2}$$

Here, $V_{\mathrm{out}}(i-1)$ is the $(i-1)^{\mathrm{th}}$ sample of the output signal. This means that if $V_{\mathrm{out}}(i)$ is the present state, $V_{\mathrm{out}}(i-1)$ is the previous state. For the hystereretic inverter, several parameters are defined as follows. Normalized magnitudes of the input signal and noise are respectively $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$ and $V_{\mathrm{in_noise}}/V_{\mathrm{H}}$. The width and then normalized width of the hysteresis are W_{Hys} $(= V_{\mathrm{H}} - V_{\mathrm{L}})$ and $W_{\mathrm{Hys}}/V_{\mathrm{H}}$, respectively.

First of all, we consider stochastic resonance in the ideal non-hysteretic inverter. Stochastic resonance was evaluated by simulating the model in Fig. 3.1 in the conditions: the normalized input signal $V_{\mathrm{in_signal}}/V_{\mathrm{th}}$ is set at 0.60, 0.70, 0.80, and 0.90; the normalized input noise $V_{\mathrm{in_noise}}/V_{\mathrm{th}}$ is swept from 0.00 to 5.00 with a step of 0.025. CC are plotted as functions of $V_{\mathrm{in_noise}}/V_{\mathrm{th}}$ in

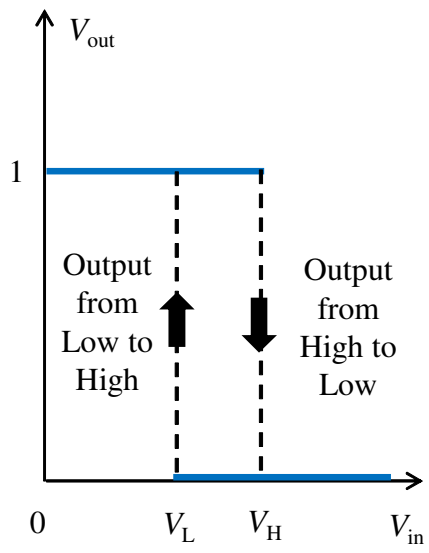


Figure 3.4: Input-output characteristics of an ideal hysteretic inverter.

Fig. 3.5. It can be seen that CC behave like resonance curves with dips at the smallest values. All of dips of CC are larger than -0.6 which is far from -1.

Next, to determine which inverter is better for stochastic resonance, we simulate the model in Fig. 3.1 for both non-hysteretic and hysteretic inverters. When $W_{\mathrm{Hys}}/V_{\mathrm{H}} = 0$, it is a non-hysteretic inverter; when $W_{\mathrm{Hys}}/V_{\mathrm{H}} \neq 0$, it is a hysteretic inverter. For the hysteretic inverter, the width of hysteresis can be adjusted by changing $W_{\mathrm{Hys}}/V_{\mathrm{H}}$. Simulation was executed in the following conditions. $V_{\mathrm{in_noise}}/V_{\mathrm{H}}$ was swept from 0.00 to 5.00 with a step of 0.025. $W_{\mathrm{Hys}}/V_{\mathrm{H}}$ was varied from 0.00 to 1.00 with a step of 0.025. CC were calculated at different $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$ of 0.50 (Figs. 3.6(a) and (b)), 0.70 (Figs. 3.6(c) and (d)), and 0.90 (Figs. 3.6(e) and (g)). Behaviors of CC are like resonance curves with dips at the smallest values (Figs. 3.6(a), (c), and (e)).

On the one hand, we compare stochastic resonance in the hysteretic inverter with that in the non-hysteretic inverter. At the same $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$, dips of CC of the hysteretic inverter are closer to -1 than those of the non-hysteretic inverter (Figs. 3.6(a), (c), and (e)). For example, at $V_{\mathrm{in_signal}}/V_{\mathrm{H}} = 0.70$ (Figs. 3.6(c) and (d)), dips of CC of the non-hysteretic are larger than -0.6 whereas

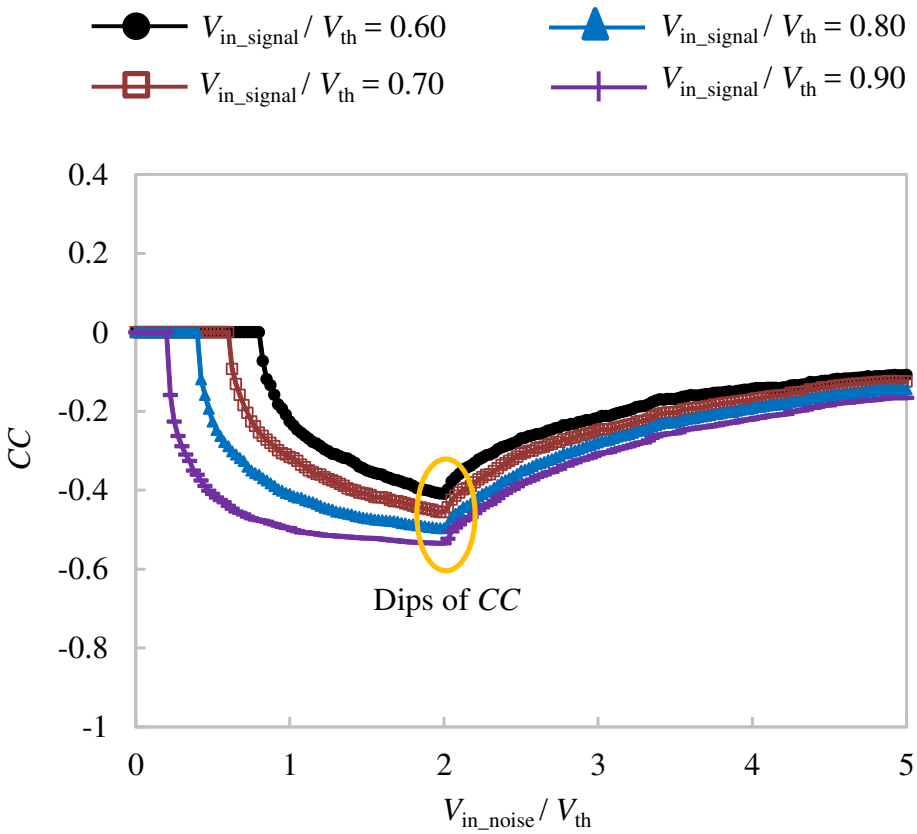


Figure 3.5: Correlation coefficients CC between input and output signals of the ideal non-hysteretic inverter are plotted as functions of normalized input noise $V_{\mathrm{in_noise}}/V_{\mathrm{th}}$ at different normalized input signals $V_{\mathrm{in_signal}}/V_{\mathrm{th}}$ of 0.60, 0.70, 0.80, and 0.90.

those of the hysterertic inverter are approximately -1. This indicates that stochastic resonance in the hysteretic inverter is better than that in the non-hysteretic inverter from the viewpoint of CC.

On the other hand, we evaluate CC characteristics in the hysteretic inverter as follows. Firstly, as $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$ is increased, the dips of CC go towards the ideal value (-1). For example, the dips for $V_{\mathrm{in_signal}}/V_{\mathrm{H}} = 0.50$ are approximately -0.60, whereas those for $V_{\mathrm{in_signal}}/V_{\mathrm{H}} = 0.70$ are -1. Secondly, the greater $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$ is, the wider the region of the excellent CC is. Namely, the region of the excellent CC reperesented by black color does not exist for $V_{\mathrm{in_signal}}/V_{\mathrm{H}} = 0.50$ (Figs. 3.6(a) and 3.6(b)) and increases as

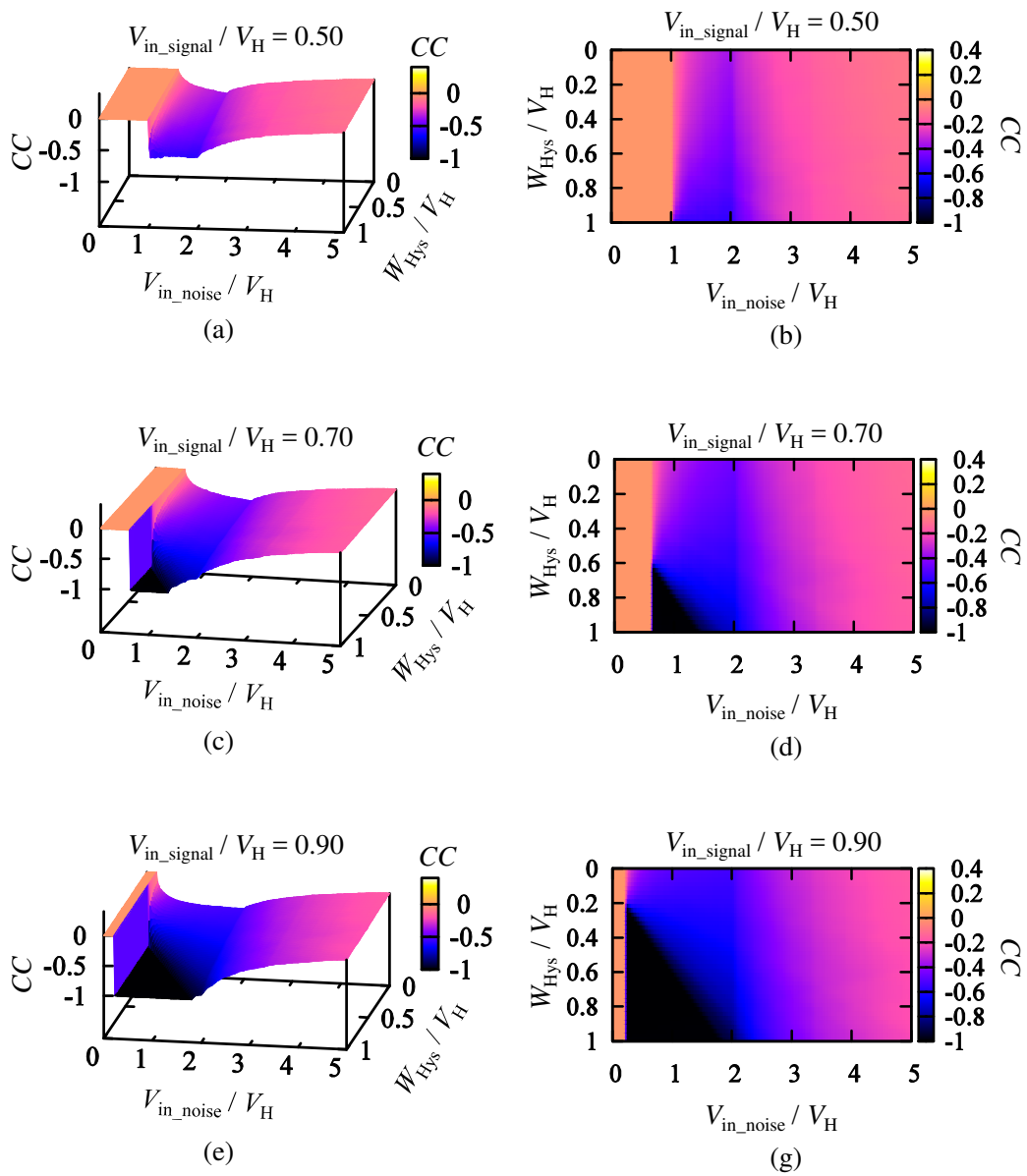


Figure 3.6: Correlation coefficients CC between input and output signals of the ideal inverter (The ideal inverter means that it has the sharp switching at the threshold voltage). They are plotted as functions of normalized input noise $V_{\text{in_noise}}/V_{\text{H}}$ and normalized width of the hysteresis $W_{\text{Hys}}/V_{\text{H}}$ in 3-D splots (a, c, e) and 2-D plots (b, d, g) at different normalized input signals $V_{\text{in_signal}}/V_{\text{H}}$. (a) and (b) $V_{\text{in_signal}}/V_{\text{H}} = 0.50$. (c) and (d) $V_{\text{in_signal}}/V_{\text{H}} = 0.70$. (e) and (g) $V_{\text{in_signal}}/V_{\text{H}} = 0.90$.

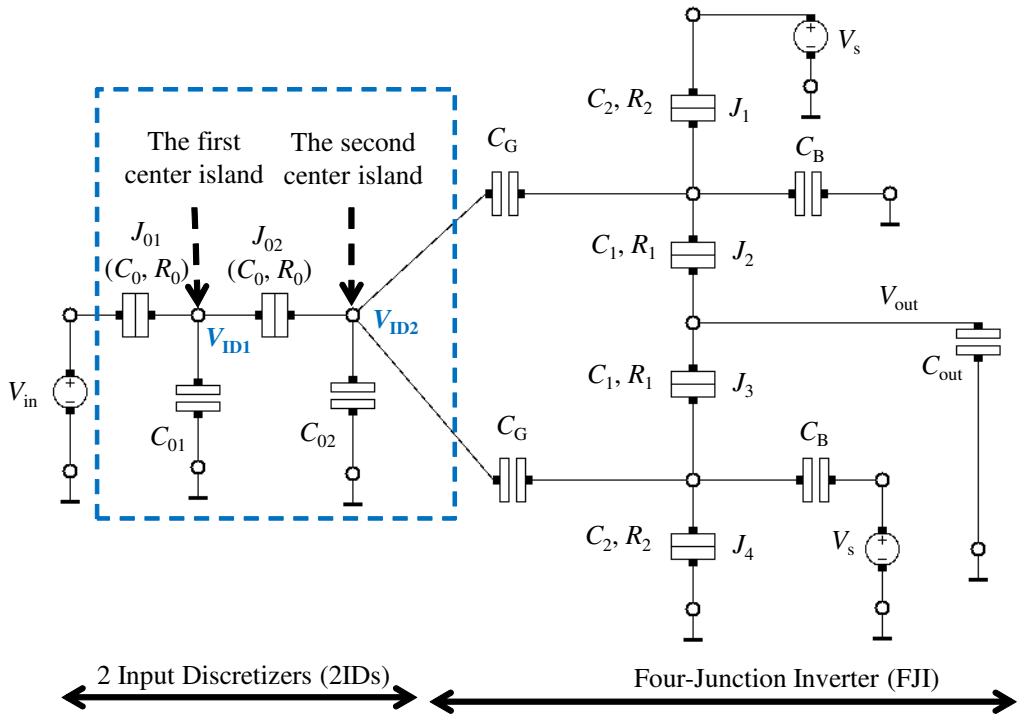


Figure 3.7: Schematic diagram of SE hysteretic inverter (2ID-FJI).

$V_{\text{in_signal}}/V_{\text{H}}$ increases from 0.70 to 0.90 (Figs. 3.6(c)−(g)). Finally, with the same $V_{\text{in_signal}}/V_{\text{H}}$, the larger $W_{\text{Hys}}/V_{\text{H}}$ is, the wider the range of $V_{\text{in_noise}}/V_{\text{H}}$ for the excellent CC is. For example, at $V_{\text{in_signal}}/V_{\text{H}} = 0.90$ (Fig. 3.6(g)), the range of $V_{\text{in_noise}}/V_{\text{H}}$ for the excellent CC at $W_{\text{Hys}}/V_{\text{H}} = 0.80$ is wider than that at $W_{\text{Hys}}/V_{\text{H}} = 0.60$.

Thus, CC of stochastic resonance in an inverter can be enhanced by designing the hysteretic inverter with a wide hysteresis (large $W_{\text{Hys}}/V_{\text{H}}$).

3.3 A single-electron hysteretic inverter designed for enhancement of stochastic resonance

On the basis of the analysis in Sect. 3.2, an SE hysteretic inverter should be designed with $W_{\text{Hys}}/V_{\text{H}}$ as large as possible to realize stochastic resonance well.

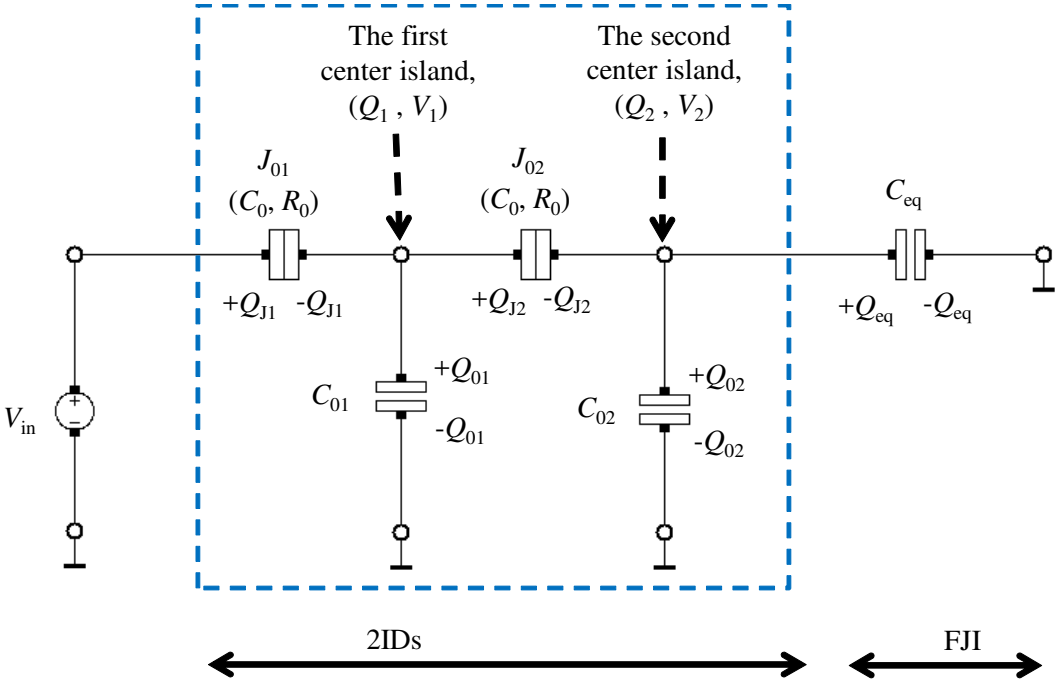


Figure 3.8: Simplified circuit model used for analysis of the 2ID-FJI.

An SE hysteretic inverter is designed by combining two IDs and the FJI (2ID-FJI) as shown in Fig. 3.7. The FJI is composed of upper and lower parts [29]. The upper part consists of two junctions (J_1 and J_2), a gate capacitor (C_G), and a bias capacitor (C_B). The lower part includes two junctions (J_3 and J_4), a gate capacitor (C_G), and a bias capacitor (C_B). Two IDs consisting of two junctions (J_{01} and J_{02} having the same capacitance C_0 and resistance R_0) and two grounded capacitors (C_{01} and C_{02}) are serially-cascaded and connected to two gate capacitors (C_{G}) of the FJI. Figure 3.8 shows a simplified circuit model used for analysis of the 2ID-FJI. Looking from the second island of the 2IDs to the FJI, since C_{out} is much larger than the other capacitances, we approximate FJI by two parallel branches. In each branch, C_G is in series with a group which is composed of C_1, C_2, and C_B in parallel. Capacitance C_{eq} equivalent to an FJI as follows,

$$C_{\mathrm{eq}} \approx 2\frac{C_G(C_1 + C_2 + C_B)}{C_G + (C_1 + C_2 + C_B)} \tag{3.3}$$

Polarization charges on the individual junctions and capacitors are in the form of

$$Q_{\mathrm{J1}} = (V_{\mathrm{in}} - V_1)C_0, \tag{3.4}$$

$$Q_{01} = V_1 C_{01}, \tag{3.5}$$

$$Q_{\mathrm{J2}} = (V_1 - V_2)C_0, \tag{3.6}$$

$$Q_{02} = V_2 C_{02}, \tag{3.7}$$

$$Q_{\mathrm{eq}} = V_2 C_{\mathrm{eq}}. \tag{3.8}$$

Here

Q_{J1} and Q_{J2} are respectively the charges on the junctions J_{01} and J_{02};

Q_{01} and Q_{02} are the charges on the capacitors C_{01} and C_{02}, respectively;

Q_{eq} is the charge on the capacitor C_{eq};

V_1 and V_2 are the voltages across the capacitors C_{01} and C_{02}, respectively.

Quantization of the charges on the first and second center islands of the 2IDs can be expressed as follows,

$$-Q_{\mathrm{J1}} + Q_{01} + Q_{\mathrm{J2}} = N_1 e + Q_{P1}, \tag{3.9}$$

$$-Q_{\mathrm{J2}} + Q_{02} + Q_{\mathrm{eq}} = N_2 e + Q_{P2}. \tag{3.10}$$

Here

N_1 and N_2 are the numbers of excess electrons on the first and second center islands of the 2IDs, respectively;

Q_{P1} and Q_{P2} are respectively background polarization charges.

In this chapter, the background polarization charges are assumed to be zero, i.e., $Q_{P1} = Q_{P2} = 0$.

Substitutions of Eqs. (3.4) − (3.6) to Eq. (3.9) and Eqs. (3.6) − (3.8) to Eq. (3.10), Eqs. (3.9) and (3.10) are transformed respectively as the followings,

$$-(V_{\rm in}-V_1)C_0+V_1C_{01}+(V_1-V_2)C_0 = N_1e, \quad (3.11)$$

$$-(V_1-V_2)C_0+V_2C_{02}+V_2C_{\rm eq} = N_2e. \quad (3.12)$$

Eliminating V_2 from Eqs. (3.11) and (3.12) gives

$$-V_{\rm in}C_0+V_1\left[C_0+C_{01}+\frac{(C_{02}+C_{\rm eq})C_0}{C_0+C_{\rm eq}+C_{02}}\right]=N_1e+\frac{N_2eC_0}{C_0+C_{02}+C_{\rm eq}}. \quad (3.13)$$

On the other hand, the condition for tunneling through the J_{01} has to safisfy [29]

$$V_{\rm in}-V_1=\pm\frac{e}{2C_1^*}, \quad (3.14)$$

where, signs "+" and "−" correspond to the forward tunneling (charge $+e$ tunneling from left to right) and backward tunneling (charge $+e$ tunneling from right to left) through the J_{01}. C_1^* is the total capacitance between the first center island and its environment [29], which is expressed as

$$\begin{aligned} C_1^* &= C_0+C_{01}+C_0//(C_{02}+C_{\rm eq}) \\ &= C_0+C_{01}+\frac{C_0(C_{02}+C_{\rm eq})}{C_0+(C_{02}+C_{\rm eq})}. \end{aligned} \quad (3.15)$$

Combination of Eqs. (3.13) − (3.15), the input threshold voltage $V_{\rm inT}$ for single-electron tunneling through the J_{01} can be given by

$$V_{\rm inT}=\frac{C_0+C_{02}+C_{\rm eq}}{C_0C_{01}+(C_0+C_{01})(C_{02}+C_{\rm eq})}(\pm\frac{e}{2}+N_1e+\frac{N_2eC_0}{C_0+C_{02}+C_{\rm eq}}). \quad (3.16)$$

The high and low threshold voltages $V_{\rm H}$ and $V_{\rm L}$ of the 2ID-FJI are respectively derived by selecting plus and minus signs in Eq. (3.16),

$$V_{\rm H}=\frac{C_0+C_{02}+C_{\rm eq}}{C_0C_{01}+(C_0+C_{01})(C_{02}+C_{\rm eq})}\left(\frac{e}{2}+N_1e+\frac{N_2eC_0}{C_0+C_{02}+C_{\rm eq}}\right), \quad (3.17)$$

$$V_{\mathrm{L}} = \frac{C_0 + C_{02} + C_{\mathrm{eq}}}{C_0 C_{01} + (C_0 + C_{01})(C_{02} + C_{\mathrm{eq}})}\left(-\frac{e}{2} + N_1 e + \frac{N_2 e C_0}{C_0 + C_{02} + C_{\mathrm{eq}}} \right). \quad (3.18)$$

According to Eqs. (3.17) and (3.18), V_{H} and V_{L} of the 2ID-FJI depend on the capacitances C_{01} and C_{02}.

Parameters of the 2ID-FJI are determined as follows. Parameters of the FJI are the same as the previous literature: $C_1 = 2C_2$, $C_G = 8C_2$, $C_B = 7C_2$, $C^* = C_1 + C_2 + C_G + C_B$, $V_s = 1.5/2C^*$ [29]. On the basis of these capacitance relationships, we set a typical value of C_2, $C_2 = 1$ aF, and calculate the other capacitances. Then, in the numerical simulation below, values of parameters are assumed as: $C_1 = 2$ aF, $R_1 = 50$ kΩ, $C_2 = 1$ aF, $R_2 = 100$ kΩ, $C_G = 8$ aF, $C_B = 7$ aF, $V_s = 6.7$ mV, $C_{\mathrm{out}} = 1$ fF. For simplication, C_{01} is set to be equal C_{02}. Since V_{H} and V_{L} of the 2ID-FJI depend on C_{01} and C_{02} (Eqs. (3.17) and (3.18)), values of C_{01} and C_{02} must be adjusted to achieve the hysteresis whose width is as wide as possible. The appropriate parameters of the 2IDs were chosen as follows: $C_0 = 1$ aF, $R_0 = 100$ kΩ, and $C_{01} = C_{02} = 72$ aF.

The numbers of excess electrons on the first and second center islands, $N_1 = Q_1/e$ and $N_2 = Q_2/e$, of the 2IDs are determined by simulation as shown in Fig. 3.9. Monte-Carlo simulation was executed using SIMON program [26] with the conditions of 0 K and no cotunneling. In Fig. 3.7, voltage V_{ID2} on the second island of the 2IDs is the direct input voltage of the main device FJI. In addition, in Sect. 2.3.1, the FJI switches between high and low output levels when its input voltage is between 2.48 mV and 4.22 mV. Hence, the switching between high and low output levels of the 2ID-FJI occurs when V_{ID2} is in the range between 2.48 mV and 4.22 mV. In Figs. 3.9(a) and (b), for V_{in} increasing from 0 to the source voltage V_s (6.7 mV), the switching occurs from high to low output level when V_{ID2} rises to 2.48 mV. $V_{\mathrm{ID2}} = 2.48$ mV at $(V_{\mathrm{H}})_{\mathrm{sim}} = 5.53$ mV where there are tunneling events from the states $N_1 = 2$ (to 3) and $N_2 = 1$ (to 3). In Figs. 3.9(c) and (d), for V_{in} decreasing from V_s to 0, the switching occurs from low to high output level when V_{ID2} reduces to 4.22 mV. $V_{\mathrm{ID2}} = 4.22$ mV at $(V_{\mathrm{L}})_{\mathrm{sim}} = 1.15$ mV where there are tunneling

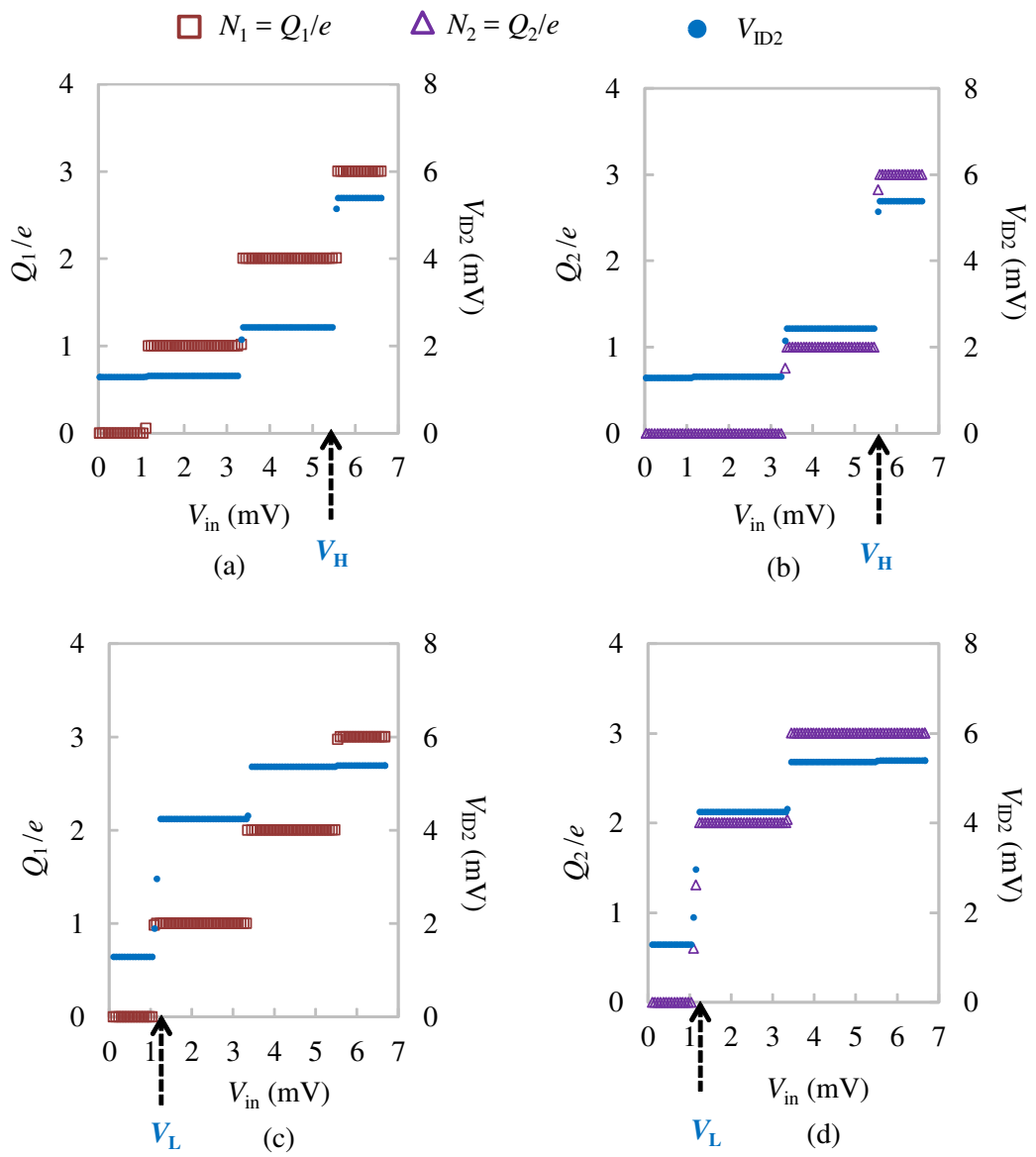


Figure 3.9: Number of excess electrons in the first and second center islands of the 2IDs, $N_1 = Q_1/e$ and $N_2 = Q_2/e$, are plotted as functions of input voltage V_{in}. Voltage on the second center island of the 2IDs, V_{ID2}, is also plotted as a function of V_{in}. (a) and (b) V_{in} increases. (c) and (d) V_{in} decreases.

events from the states $N_1 = 1$ (to 0) and $N_2 = 2$ (to 0).

The threshold voltages of the 2ID-FJI can be calculated from Eqs. (3.17) and (3.18) as follows. Substituting $N_1 = 2$ and $N_2 = 1$ to Eq. (3.17), the calculated high threshold voltage $(V_H)_{cal}$ is 5.51 mV. Substitution of $N_1 = 1$

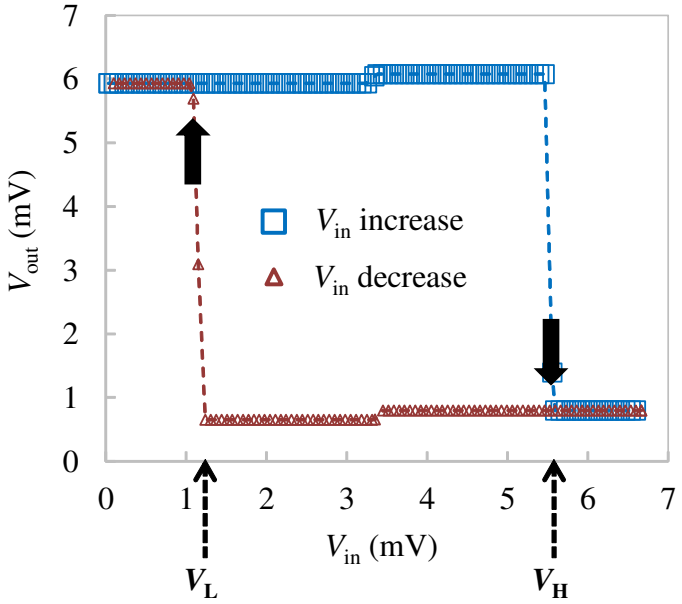


Figure 3.10: Input-output characteristics of the 2ID-FJI with $C_{01} = C_{02} = 72$ aF at $T = 0$ K. Dashed lines are inserted into the graph to show switching trends between high and low levels of V_{out}.

and $N_2 = 2$ to Eq. (3.18) obtains the calculated low threshold voltage $(V_{\mathrm{L}})_{\mathrm{cal}}$ of 1.15 mV. Thus the calculated and simulated threshold voltages of the 2ID-FJI are in reasonable agreement.

Input-output characteristics of the 2ID-FJI with $C_{01} = C_{02} = 72$ aF are described in Fig. 3.10. V_{out} for increasing and decreasing V_{in} are represented by rectangles and triangles, repectively. Hysteretic characteristics are confirmed with two threshold voltages V_{H} and V_{L}. The ratio of V_{L} to V_{H} is 0.208. The width ($W_{\mathrm{Hys}} = V_{\mathrm{H}} - V_{\mathrm{L}}$) and the normalized width ($W_{\mathrm{Hys}}/V_{\mathrm{H}}$) of the hysteretic region are 4.38 mV and 0.792, respectively. In addition, sharp switches between high and low output levels are also observed.

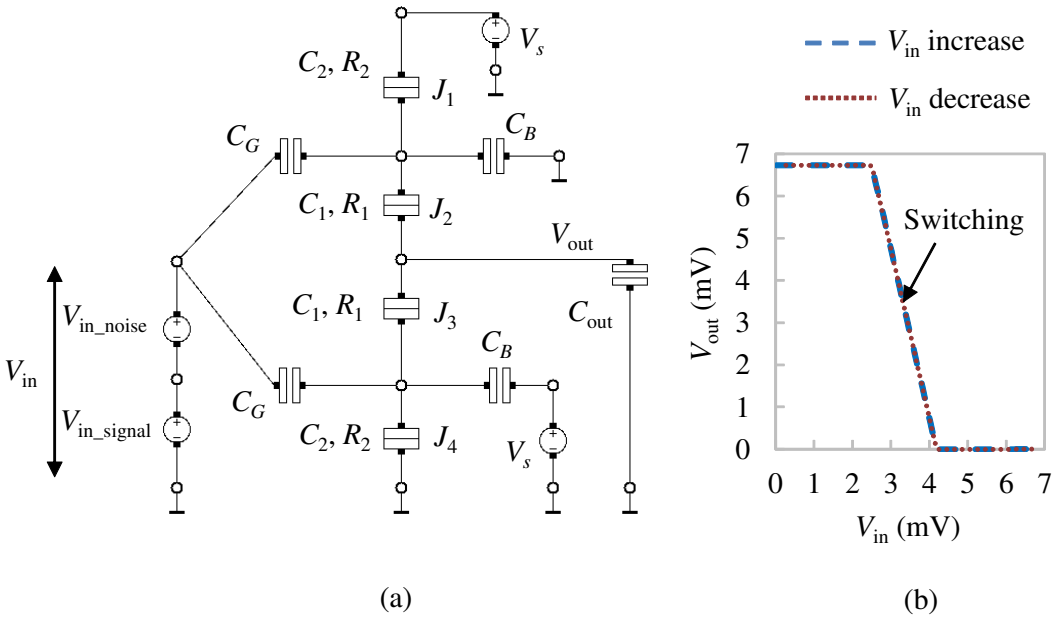


Figure 3.11: (a) Schematic diagram of single-electron four-junction inverter (FJI) is used for evaluation of stochastic resonance. (b) Input-output voltage characteristics of the FJI for the input signal increasing and decreasing between 0 and V_s (= 6.7 mV). No noise is included.

3.4 Enhancement of stochastic resonance using SE hysteretic inverter (2ID-FJI)

3.4.1 Stochastic resonance in single-electron four-junction inverter (SE FJI)

A schematic diagram of the FJI used for the evaluation of stochastic resonance is shown in Fig. 3.11(a). Output V_{out} is the voltage across the output capacitor C_{out}. Parameters of the FJI are the same as those in Sect. 3.3. Monte-Carlo simulation was executed in the conditions of 0 K and no cotunneling. Input-output characteristics of the FJI where no input noise is added are illustrated in Fig. 3.11(b). There is no hysteresis in its input-output characteristics.

One of the important ingredients of stochastic resonance is the threshold

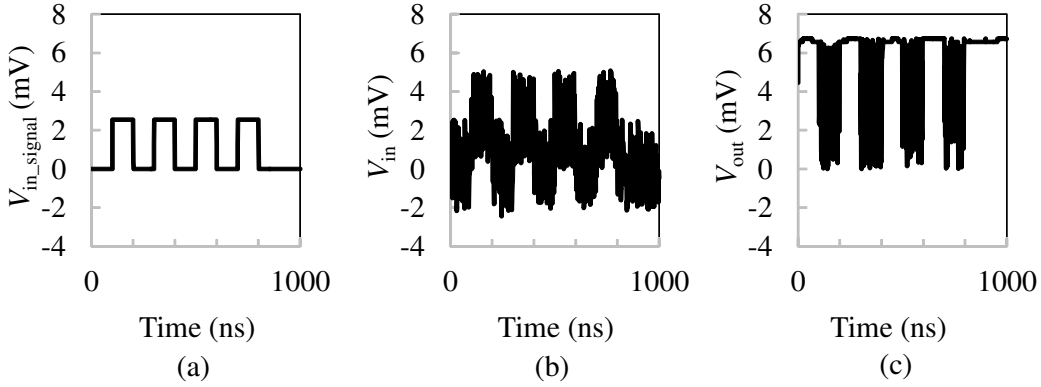


Figure 3.12: Example of simulated waveforms in the FJI. (a) Subthreshold input signal $V_{\text{in_signal}}$ has a nomalized magnitude $V_{\text{in_signal}}/\theta_{\text{S}}$ of 0.90. (b) Noisy input signal V_{in} contains $V_{\text{in_signal}}$ and input noise $V_{\text{in_noise}}$ where the input noise has a normalized magnitude $V_{\text{in_noise}}/\theta_{\text{S}}$ of 1.80. (c) Output signal V_{out}.

at which the output of the system responds to the input. A strict threshold is defined as the minimum level of the input signal which makes the device respond. We have found that the strict threshold of the FJI, θ_{S}, is 2.83 mV. A subthreshold input signal of the FJI is defined as a signal whose amplitude is smaller than the strict threshold ($V_{\text{in_signal}} < \theta_{\text{S}}$). For the FJI, normalized magnitudes of the input signal and noise are respectively defined as $V_{\text{in_signal}}/\theta_{\text{S}}$ and $V_{\text{in_noise}}/\theta_{\text{S}}$.

An example of simulated waveforms in the FJI, $V_{\text{in_signal}}$, V_{in} ($= V_{\text{in_signal}} + V_{\text{in_noise}}$), and the output V_{out}, are shown in Fig. 3.12. By adding the input noise to the subthreshold input signal (Fig. 3.12(a)), the noisy input signal has random fluctuations as described in Fig. 3.12(b). Figure 3.12(c) shows that, at the specific noise level, the output of the FJI responds to the input.

CC of the FJI is plotted as a function of $V_{\text{in_noise}}/\theta_{\text{S}}$ in Fig. 3.13. CC at different $V_{\text{in_signal}}/\theta_{\text{S}}$ of 0.60, 0.70, 0.80, and 0.90 are represented by solid circles, open rectangles, solid triangles, and slashes, respectively. When the input noise level increases, CC of the FJI behaves as a resonance curve with a dip. In Fig. 3.13, the dips are around -0.60.

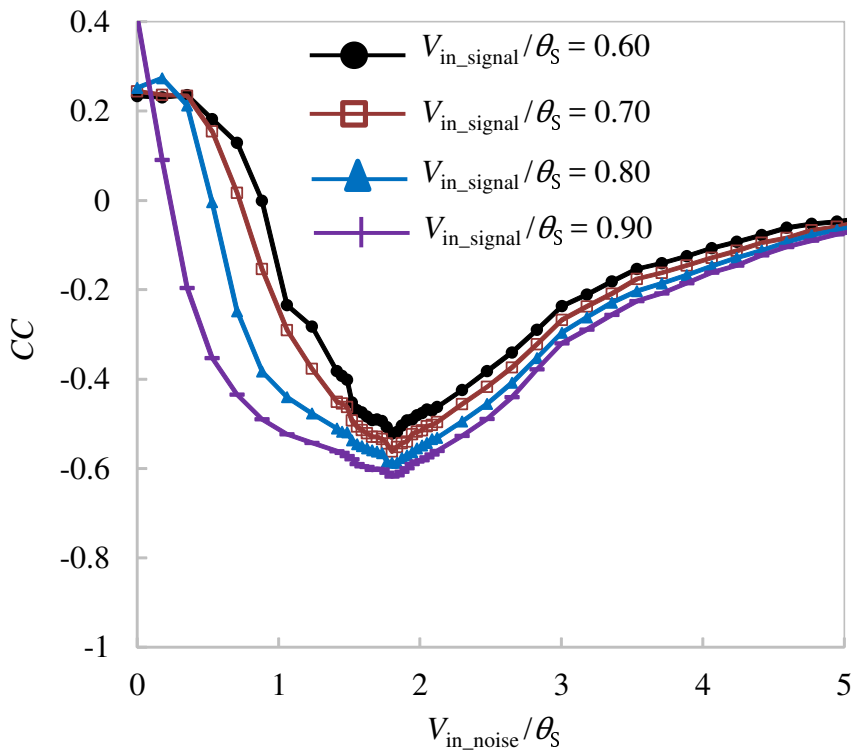


Figure 3.13: Correlation coefficients CC between input and output signals of the FJI are plotted as functions of normalized input noise V_{in_noise}/θ_S at different normalized input signals V_{in_signal}/θ_S of 0.60, 0.70, 0.80, and 0.90.

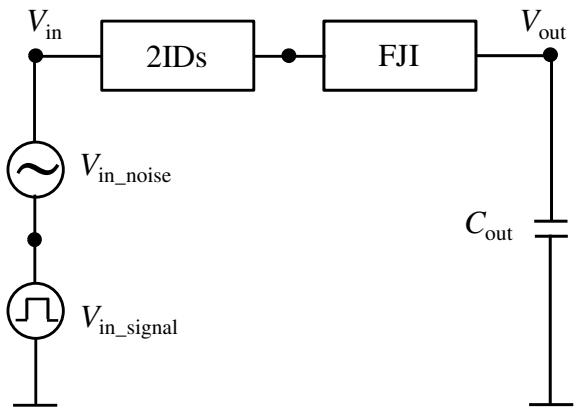


Figure 3.14: 2ID-FJI used for evaluation of stochastic resonance.

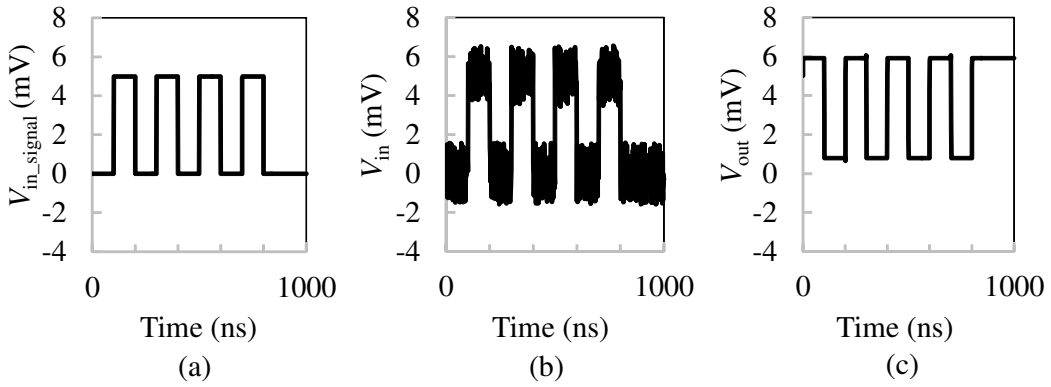


Figure 3.15: Example of simulated waveforms in the 2ID-FJI. (a) Subthreshold input signal $V_{\text{in_signal}}$ has a nomalized magnitude $V_{\text{in_signal}}/V_{\text{H}}$ of 0.90. (b) Noisy input signal V_{in} contains $V_{\text{in_signal}}$ and input noise $V_{\text{in_noise}}$ where the input noise has a normallized magnitude $V_{\text{in_noise}}/V_{\text{H}}$ of 0.58. (c) Output signal V_{out}.

3.4.2 Enhancement of stochastic resonance by using 2ID-FJI

The 2ID-FJI used for evaluation of stochastic resonance is shown in Fig. 3.14. The noisy input signal V_{in} including the input signal $V_{\text{in_signal}}$ and the input noise $V_{\text{in_noise}}$ is applied to the 2ID-FJI. Normalized magnitudes of the input signal and noise used in the 2ID-FJI are defined as similarly as those used in the ideal hysteretic inveter (Sect. 3.2), which are respectively $V_{\text{in_signal}}/V_{\text{H}}$ and $V_{\text{in_noise}}/V_{\text{H}}$.

Figure 3.15 shows an example of simulated waveforms in the 2ID-FJI. By adding the input noise to the subthreshold input signal (Fig. 3.15(a)), the noisy input signal has random fluctuations as described in Fig. 3.15(b). Figure 3.15(c) shows that, at the specific noise level, the output of the 2ID-FJI responds well to the input. Making a comparison between the output signals of the FJI (Fig. 3.12(c)) and the 2ID-FJI (Fig. 3.15(c)) indicates the improvement of the 2ID-FJI as follows. With the same normalized magnitude of the input signal ($V_{\text{in_signal}}/\theta_{\text{S}} = V_{\text{in_signal}}/V_{\text{H}} = 0.90$) and the noise levels chosen to obtain the dips of CC, while the output signal of the FJI fluctuates,

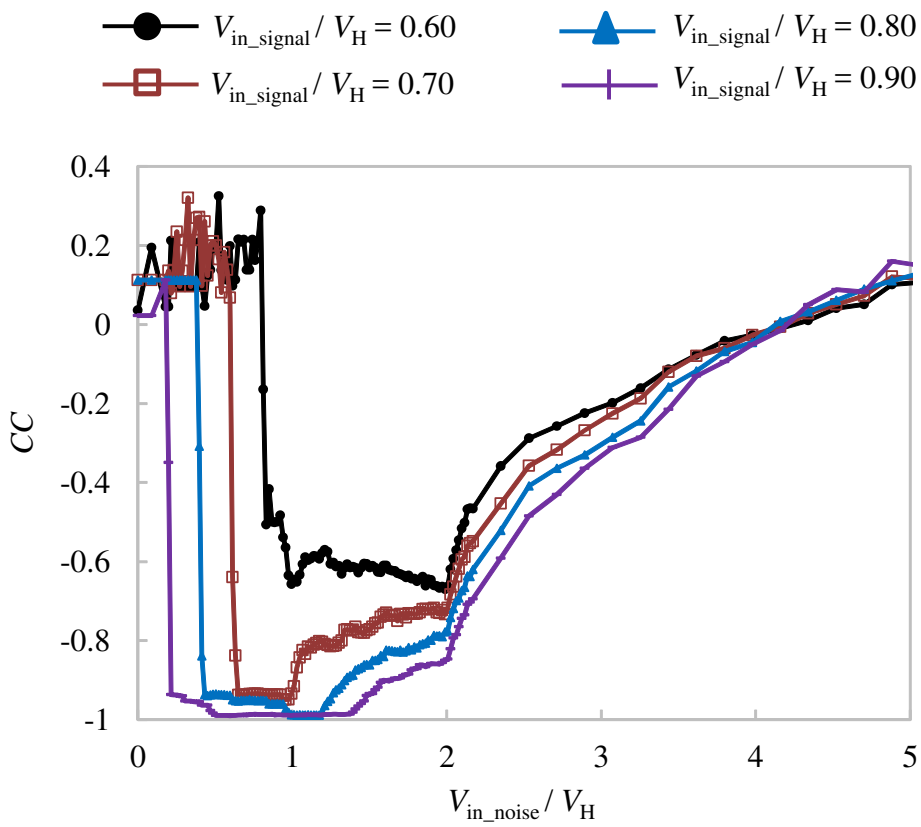


Figure 3.16: Correlation coefficients CC between input and output signals of the 2ID-FJI are plotted as functions of normalized input noise $V_{\mathrm{in_noise}}/V_{\mathrm{H}}$ at different normalized input signals $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$ of 0.60, 0.70, 0.80, and 0.90. The normalized width of the hysteresis of the 2ID-FJI, $W_{\mathrm{Hys}}/V_{\mathrm{H}}$, is 0.792.

that of the 2ID-FJI keeps stable. The response of the output of the 2ID-FJI can be explained on the basis of its hysteretic characteristics. Although there are fluctuations in the noisy input signal (Fig. 3.15(b)), magnitudes of these fluctuations are in the range between V_{L} and V_{H} of the hysteresis. Therefore, these fluctuations do not cause the change of the output state.

Stochastic resonance in the 2ID-FJI is also evaluated via CC. Figure 3.16 describes CC of the 2ID-FJI versus $V_{\mathrm{in_noise}}/V_{\mathrm{H}}$ at different $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$ of 0.60, 0.70, 0.80, and 0.90. The responses of CC look like resonance curves with dips at the smallest CC.

From the viewpoint of CC (Figs. 3.16 compared to Fig. 3.13), the 2ID-FJI

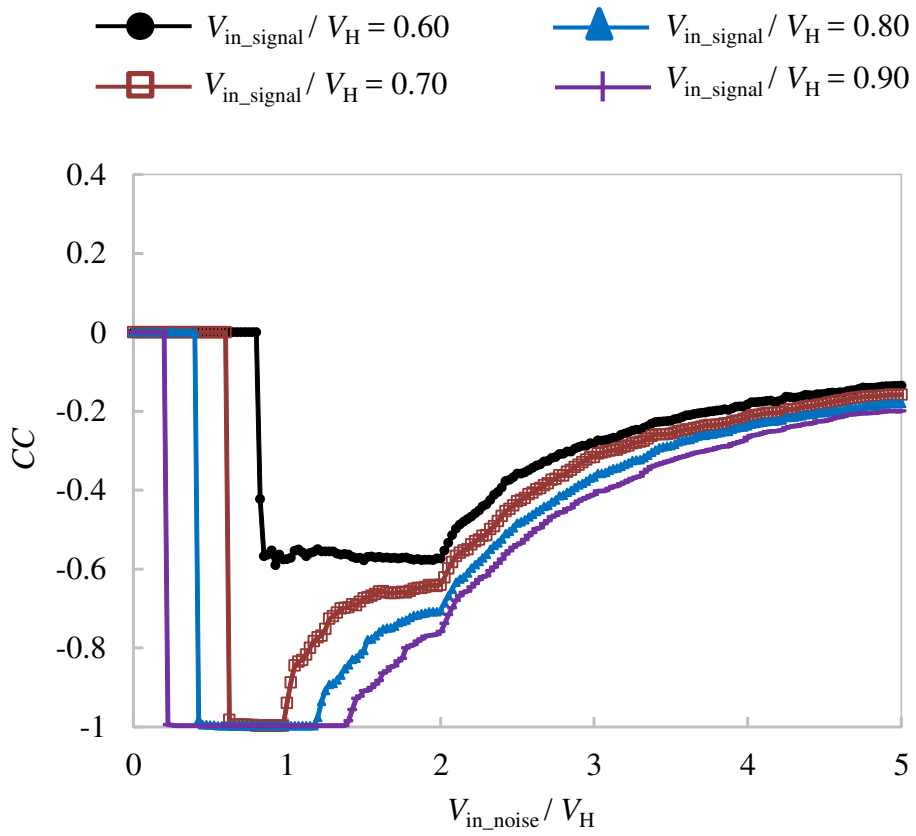


Figure 3.17: Correlation coefficients CC between input and output signals of the ideal hysteretic inverter are plotted as functions of normalized input noise $V_{\mathrm{in_noise}}/V_{\mathrm{H}}$ at different normalized input signals $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$ of 0.60, 0.70, 0.80, and 0.90. The normalized width of the hysteresis of the ideal hysteretic inverter, $W_{\mathrm{Hys}}/V_{\mathrm{H}}$, is 0.792.

has the dips of CC better than the FJI. Namely, at small (0.60) $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$, the dips of the 2ID-FJI ($CC \approx -0.67$) are slightly better than those of the FJI ($CC \approx -0.52$). At $V_{\mathrm{in_signal}}/V_{\mathrm{H}} \geq 0.70$, the dips of the 2ID-FJI are close to -1 whereas those of the FJI are less than -0.62. This advantage results from the effect of the hysteretic characteristics.

With the same $W_{\mathrm{Hys}}/V_{\mathrm{H}}$, stochastic resonance in the 2ID-FJI is as equivalent as that in the ideal hysteretic inverter from the viewpoint of CC (Fig. 3.16 compared to Fig. 3.17). Figure 3.17 illustrates CC of the ideal hysteretic inverter at different $V_{\mathrm{in_signal}}/V_{\mathrm{H}}$ of 0.60, 0.70, 0.80, and 0.90. The method for

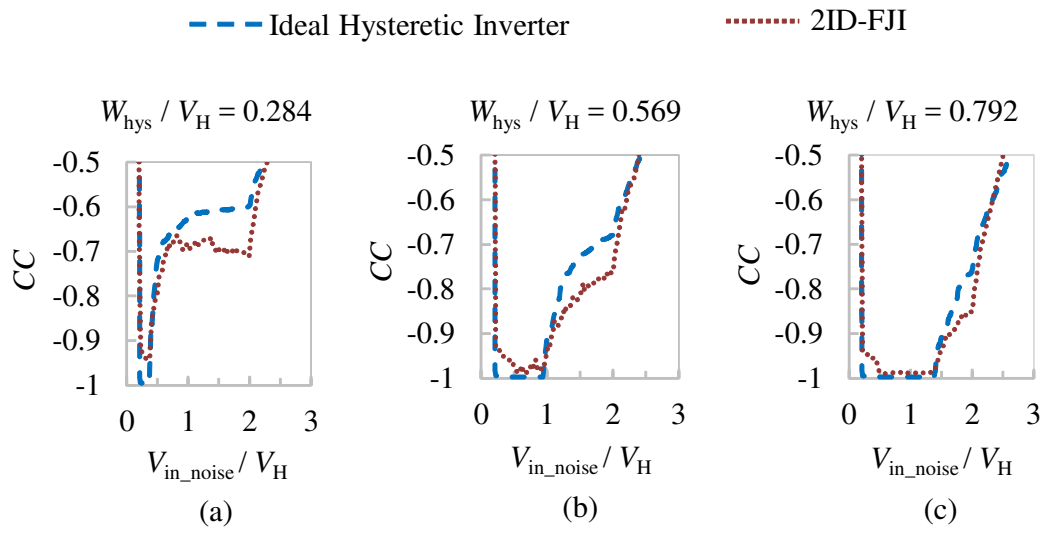


Figure 3.18: Correlation coefficients CC between input and output signals of the ideal hysteretic inverter (dashed curves) and the 2ID-FJI (dotted curves) versus normalized input noise $V_{\text{in_noise}}/V_{\text{H}}$ at the same normalized input signal $V_{\text{in_signal}}/V_{\text{H}} = 0.90$ and at different normalized widths of hysteresis $W_{\text{Hys}}/V_{\text{H}}$. (a) $W_{\text{Hys}}/V_{\text{H}} = 0.284$. (b) $W_{\text{Hys}}/V_{\text{H}} = 0.569$. (c) $W_{\text{Hys}}/V_{\text{H}} = 0.792$

.

calculating CC in Fig. 3.17 is quite similar to that in Sect. 3.2. The only difference is that in Sect. 3.2, the normalized width of the hysteresis $W_{\text{Hys}}/V_{\text{H}}$ is swept from 0.00 to 1.00, whereas in Fig. 3.17, $W_{\text{Hys}}/V_{\text{H}}$ is fixed to be equal to that of the 2ID-FJI ($W_{\text{Hys}}/V_{\text{H}} = 0.792$). At $V_{\text{in_signal}}/V_{\text{H}} = 0.60$, the 2ID-FJI and the ideal hysteretic inverter have the same dips of CC around -0.60. When $V_{\text{in_signal}}/V_{\text{H}} \geq 0.70$, their dips reach near -1.

With the same $V_{\text{in_signal}}/V_{\text{H}}$ (e.g 0.90) and different $W_{\text{Hys}}/V_{\text{H}}$, making a comparison between stochastic resonance in the 2ID-FJI and that in the ideal hystertic inverter also confirms that their CC behave similar to each other, as shown in Fig. 3.18. Namely, the dips of CC are close to -1. In addition, when $W_{\text{Hys}}/V_{\text{H}}$ increases, the region of the noise levels for the excellent CC ($CC < -0.90$) also increases.

Figure 3.19(a) shows a schematic drawing for determining the range of

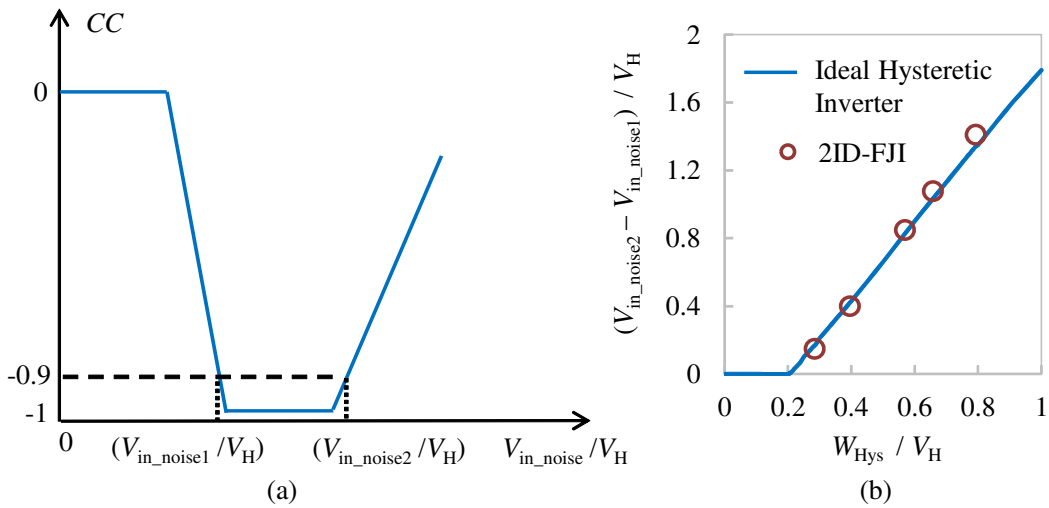


Figure 3.19: (a) Schematic drawing for determining the range of the input noise levels ($V_{\text{in_noise1}}/V_{\text{H}}, V_{\text{in_noise2}}/V_{\text{H}}$) having the excellent correlation coefficients ($CC \leq -0.90$). (b) $(V_{\text{in_noise2}} - V_{\text{in_noise1}})/V_{\text{H}}$ versus normalized width of hysteresis $W_{\text{Hys}}/V_{\text{H}}$ of the ideal hystertic inverter and the 2ID-FJI.

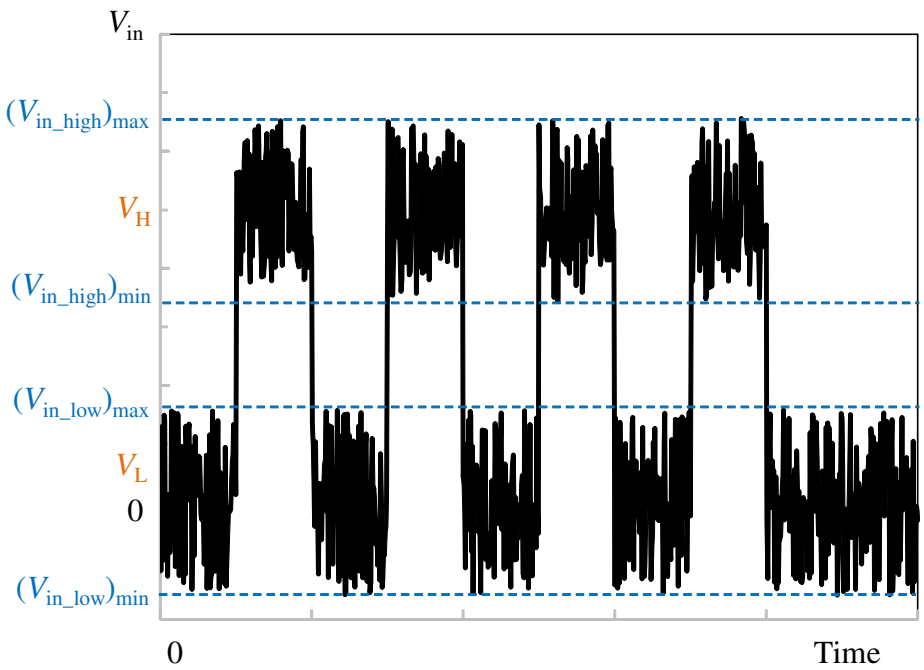


Figure 3.20: Schematic drawing for evaluating levels of the noisy input signal V_{in} which contains the input signal $V_{\text{in_signal}}$ and the input noise $V_{\text{in_noise}}$.

input noise levels (from $V_{\text{in_noise1}}/V_{\text{H}}$ to $V_{\text{in_noise2}}/V_{\text{H}}$) to obtain the excellent CC. The relationship between $(V_{\text{in_noise2}} - V_{\text{in_noise1}})/V_{\text{H}}$ and $W_{\text{Hys}}/V_{\text{H}}$ of the ideal hysteretic inverter and the 2ID-FJI are respectively illustrated by solid line and open circles in Fig. 3.19(b). It can be seen that this relationship in the 2ID-FJI is similar to that in the ideal hysteretic inverter, in which $(V_{\text{in_noise2}} - V_{\text{in_noise1}})/V_{\text{H}}$ is proportional to $W_{\text{Hys}}/V_{\text{H}}$. In addition, it is observed that $(V_{\text{in_noise2}} - V_{\text{in_noise1}})/V_{\text{H}} > 0$ when $W_{\text{Hys}}/V_{\text{H}}$ is larger than a specific value α (here, $\alpha = 0.20$).

The value of α is determined as follows. Fluctuations in the output signal of the 2ID-FJI can be eliminated if V_{in} satisfies two following conditions. Firstly, for the low level of V_{in}, its maximum value $(V_{\text{in_low}})_{\text{max}}$ $(= +(1/2)V_{\text{in_noise}})$ is smaller than V_{H} and its minimum value $(V_{\text{in_low}})_{\text{min}}$ $(= -(1/2)V_{\text{in_noise}})$ is smaller than V_{L}. Secondly, for the high level of V_{in}, its maximum value $(V_{\text{in_high}})_{\text{max}}$ $(= V_{\text{in_signal}} + (1/2)V_{\text{in_noise}})$ is larger than V_{H} and its minimum value $(V_{\text{in_high}})_{\text{min}}$ $(= V_{\text{in_signal}} - (1/2)V_{\text{in_noise}})$ is larger than V_{L}. Figure 3.20 shows an example of V_{in} which satisfies both conditions. The second condition results in that $2V_{\text{in_signal}} > V_{\text{H}} + V_{\text{L}}$ and then $W_{\text{Hys}}/V_{\text{H}} > 2(V_{\text{H}} - V_{\text{in_signal}})/V_{\text{H}}$. This requires that $\alpha = 2(V_{\text{H}} - V_{\text{in_signal}})/V_{\text{H}}$. When $V_{\text{in_signal}}/V_{\text{H}} = 0.90$, $\alpha = 0.20$ which is the same as in Fig. 3.19(b).

3.5 Conclusion

In conlusion, the SE hysteretic inverter (2ID-FJI) with the sharp switches can be designed by the combination of two IDs and the solo FJI. A model of the ideal hysteretic inverter was analyzed to determine the method for improvement of stochastic resonance. The analysis showed that CC of stochastic resonance can be improved (near -1) by designing a hysteresis whose width (W_{Hys}) is as large as possible. Therefore, the parameters of two IDs in the 2ID-FJI were chosen to achieve the large W_{Hys}. Numerical simulations demonstrated that stochastic resonance in the 2ID-FJI is as good as that in the ideal hysteretic inverter.

Chapter 4

Fabrication of single-electron devices by using gold nanoparticles

4.1 Introduction

Single-electron (SE) devices have attracted numerous researches on both theory and fabrication. In previous chapters, SE devices were analyzed theoritically. In this chapter, fabrication processes of SE devices are discussed. SE devices operate on the basis of Coulomb blockade (CB) phenomena which require the charging energy of one electron E_C to be much higher than the thermal energy k_BT: $E_C \gg k_BT$ (k_B is Boltzman constant, T is the absolute temperature) [25]. Hence, E_C is one of the important factors, which is related to the possibility of practical applications of SE devices. If the island size of SE devices is reduced, E_C and also T can increase [25]. Operation of SE devices at room temperature can be observed if the island size is decreased to a few nanometers [25]. To form such the island, many techniques such as silicon technologies [70], nano-oxidation process [71], carbon nanotube [16], aluminium nanodots [17], and nanoparticles (NPs) [72] have been used in fabrication processes. The method using NPs as islands has the two following advantages [73]. Firstly, NPs can be uniform in size with a standard deviation

of approximate 5%. Secondly, size of NP can be formed in an extremely small range from 1 nm. These advantages result in the ability of high-temperature operation of NP-based SE devices.

Electric properties of NPs depend on the size and shape of particles, distance between particles, and nature of the protection organic shell [74]. Among metal NPs, gold NPs (Au NPs) are the most stable metal NPs [74], which make them become good candidates for the islands.

To fabricate SE devices using Au NPs, there have been two typical configurations: with a probe tip and without a probe tip [72]. For the first configuration (with the probe tip), scanning tunneling microscopy (STM) have been used widely. The STM system uses a sharp conductive tip and Au NP chemisorbed via thiols on a metal substrate [72,75]. The tip and the substrate are brought into a distance small enough to let tunnel current flow. Another type using the probe tip is the conductive-probe atomic force microscope (CP-AFM) [72,76]. The CP-AFM system uses a sharp tip coated by metal and Au NP chemisorbed via thiols on a metal substrate. The distance between the tip and Au NP can be controlled by feedback electronics. Although, the STM and CP-AFM use different methods to approach their tips to Au NPs, the realized SE devices are essentialy the same. The second configuration (without the probe tip), which is composed of drain, source, and gate electrodes, has an advantage of the mechanical stability with fixed gemometry [77]. Hence, we used this configuration to fabricate three-terminal SE devices.

On the one hand, the three-terminal SE devices having C-SET characteristics were realized by using solutions of Au NPs [14, 32]. In the previous works [14, 32], they formed the narrow (sub-50-nm) gaps which required the high complexity in the forming the electrodes. On the other hand, the realization of R-SET has been limited because of the difficulty in forming the gate resistor. The gate resistor must satisfy both conditions of relative small size and resistance much greater than the quantum resitance ($R_Q \approx 26$ kΩ) [78] to minimize unwanted stray capacitance. Such gate resistors have been formed in several works [33–35, 79]. However, the previous works [33–35] did not use

Au NPs and had a very low operation temperature (sub-1-K).

In our experiment, we reduced the technical difficulty by designing wide ($\geq$ 200 nm) gaps and making connections between Au NPs randomly. Fabrication processes were done basically as follows. Drain, source, and gate electrodes were formed on a SiO_2/Si chip by using standard EBL and evaporation techniques. Then, arrays of small tunnel junctions were formed by dropping solutions of Au NPs on the chip. Characteristics of the fabricated SE devices are determined by observation of the CB phenomena in the measured data. Namely, devices exhibiting periodic Coulomb oscillations are categorized into the capacitively-coupled single-electron transistor (C-SET) type. In contrast, the devices showing the CB region without Coulomb oscillations are categorized into the resistively-coupled SET (R-SET) type.

Statistics of all devices formed by using Au NPs are shown in Table 4.1. In Table 4.1, "nonlinear" means that the device had nonlinear current-voltage characteristics but the CB phenomenon was not observed; "linear" means that the device had linear current-voltage characteristics; "no current" is defined for the case where all currents of the device were less than 0.5 nA and they did not change when the voltages were applied to the device. There were 109 fabricated devices, in which 6 devices were measured at 4.2 K and 109 devices measured at 77 K and room temperature. The percentages of devices exhibiting the CB phenomena at 4.2 K and 77 K are larger than 50%. In Table 4.2, it was observed at 77 K that the "Linear" cases occurred when the amount of Au NP solution was large, and the "No current" cases happened when the amount of Au NP solution was small. Then, the percentage of CB can be increased by using a sufficient amount of Au NP solution. For example, in our experiment, the chip having 6 devices exhibited the CB phenomena in total 6 devices when the total amount of 15-nm-diameter and 3-nm-diameter Au NP solutions in a range from 2 μL to 3 μL was dropped on the chip.

Among the devices exhibiting the CB phenomena, two cases happened when the gate voltages were applied to the devices. The first case was that the CB region changed under the effect of the gate voltage, resulting in the

Table 4.1: Statistics of devices formed by using Au NPs

Temperature (Temp.) (K)	Number of measured devices	Percentage of CB (%)	Percentage of nonlinear (%)	Percentage of linear (%)	Percentage of no current (%)
4.2	6	83.3	16.7	0	0
77	109	58.7	11.9	8.3	21.1
Room Temp.	109	1.8	2.8	95.4	0

Table 4.2: Statistics of amount of Au NP solutions used for devices which were measured at 77 K

Type of AuNPs	Amount of Au NP solutions, x (μL)		
	CB	Linear	No current
15-nm diameter (5-nm diameter)	$0.1 \leq x \leq 9$	$5 \leq x \leq 9$	$0.1 \leq x \leq 0.5$
3-nm diameter	$0 \leq x \leq 3$	$0 \leq x \leq 3$	$0 \leq x \leq 1.2$

type of devices (C-SET or R-SET) could be determined. The second case was that the CB region did not change under the effect of the gate voltage, then the type of the device was undetermined. The origin of the second case could result from that the distance between the gate and the gap was large (a few micrometers).

In this chapter, two typical fabricated devices including device I and device II are introduced. The device I had characteristics like C-SET whereas the device II had characteristics like R-SET at 77 K. For the device II, the CB gap was also observed at room temperature (287 K) and could be modulated by applying the gate voltage. In comparison with the previous C-SET devices [14, 32] which had the narrow ($<$ 50 nm) gaps, the device I had the wider gap (1000 nm). In addition, operation temperature of the device I was almost

equivalent to that in the previous work (80 K in [14]). On the other hand, the method of fabricating the device II was different from the previous works [34, 35] which did not use Au NPs. In addition, the operation temperature of the device II was higher than that in the previous works (sub-1-K in [34, 35]).

4.2 Fabrication techniques

4.2.1 Introduction of fabrication processes

4.2.1.1 Processes for forming three electrodes

Fabrication processes include the following steps: design of electrode layouts on a CAD, coating a resist on the chip, electron-beam (EB) drawing, development, shadow evaporation, and lift-off.

I used EB resists made of PMMA and/or Copolymer [80]. PMMA (polymethy methacrylate) is used as a high resolution positive resist. Copolymer is a combination of PMMA and PMAA. A solution of PMMA/Copolymer is dropped on the clean SiO_2/Si substrate, followed by the spinning at a certain speed, and then prebaked at specific temperature and duration. The thickness as well as the solubility of the resist are achieved by choosing appropriate parameters of the spin speed, prebaking temperature and prebaking duration. The relationships between the film thickness and the spin speed for Copolymer and PMMA resists are represented in Figs. 4.1 and 4.2, respectively [80]. The substrate coated by the resist is illustrated in Fig. 4.3. Due to the positive resist, it is converted from low to high solubility by electron beam [81]. A bi-layer resist combines a low layer and a high layer. The low and high layers have a large difference in sensitivity.

Electron beam lithography (EBL) is one of the most important techiques in nanofabrication [81]. EBL uses highly focused electron beam to write the designed pattern in the resist. After EB drawing, polymer in the resist is broken into smaller and more soluble fragments [81]. There are several factors degrading the process of EB drawing, in which the main effects result from the

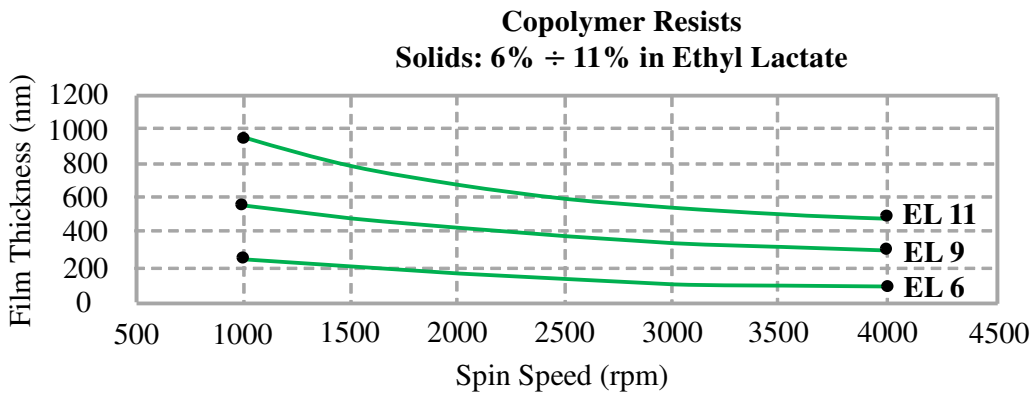


Figure 4.1: Film thickness versus spin speed for Copolymer resist at different Ethyl Lactate (EL) of 6%, 9%, and 11%. (After MicroChem datasheet [80].)

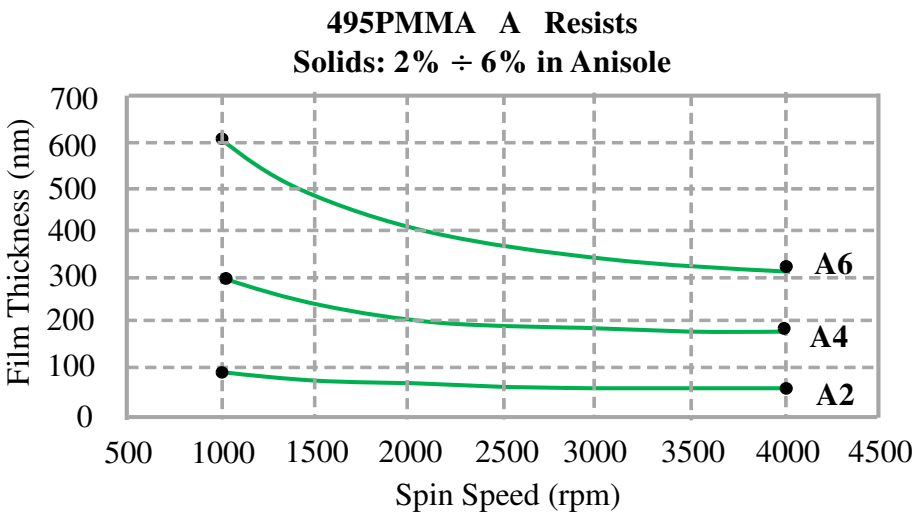


Figure 4.2: Film thickness is plotted as a function of spin speed for PMMA resist at different Anisole (A) of 2%, 4%, and 6%. (After MicroChem datasheet [80].)

forward and backward scattering phenomena (Fig. 4.4) [81]. The electrons entering the resist cause a series of low energy elastic collisions which deflect the electrons, resulting in the forward scattering. This phenonmenon broadens the beam and becomes significant with thick resist and low incident energy [81]. In addition, although most of the electrons penetrate into the substrate, some of them re-emerge into the resist layer resulting in the backward scattering.

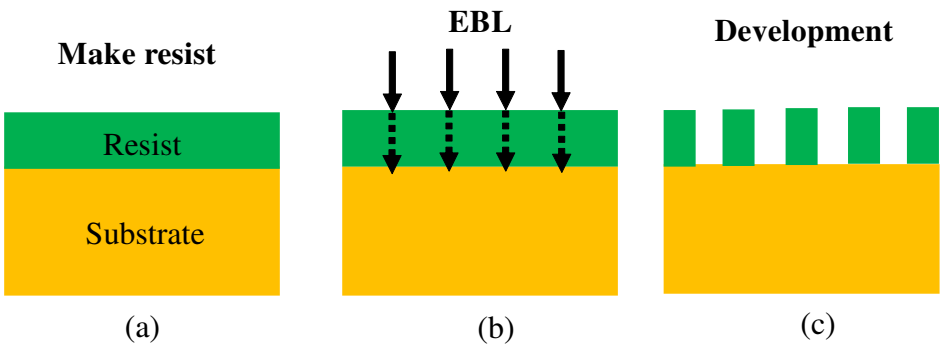


Figure 4.3: Outline of EBL process steps to form a pattern from a positive resist.

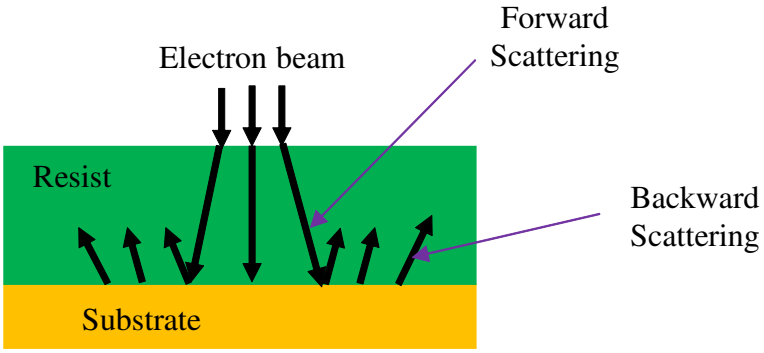


Figure 4.4: The forward and backward scattering phenomena in EBL.

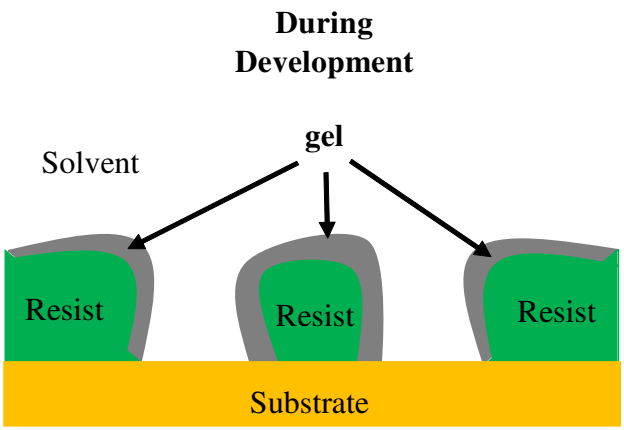


Figure 4.5: Interactions happen during the development process. (After M. A. Mohammad et al. [81].)

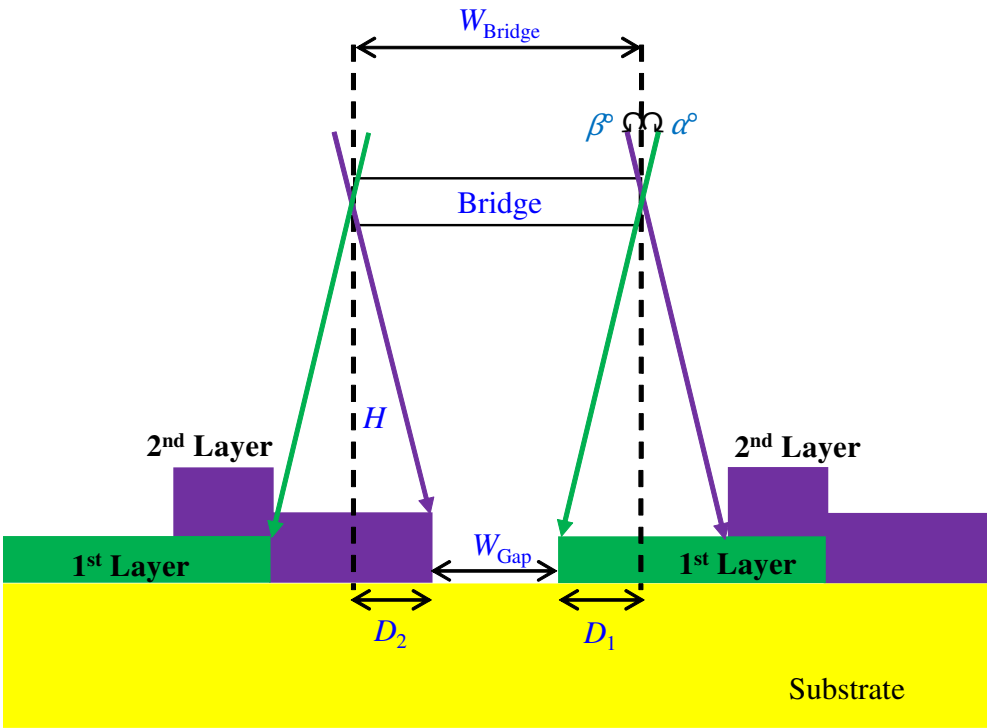


Figure 4.6: Model of shadow evaporation.

This leads to the proximity effect which causes the exposure of the area nearby the written patterns, causing the pattern distortion and overexposure [81].

After EB drawing, the pattern is immersed in a liquid developer to remove the irrediated fragments [81]. The dissolution depends on the temperature and duration of the development process. The hotter temperature or the longer duration is, the faster dissolution is. Development process happens as shown in Fig. 4.5 [81]. The solvent penetrates into the poly chain of the resist and surround the fragments forming the gels. After the surrounding is complete, the fragments detach from the chain and diffuse into the solvent. The long fragments take long time for dissolution. Exposure and development are related to each other. Namely, heavier exposure results in shorter development and vice versa. In development, it can appear the underdevelopment/overdevelopment which dissolution of the irradiated fragments is not enough or too much, causing undesired structure of the pattern.

Shadow evaporation technique is used to deposit metal in different angles

as shown in Fig. 4.6. This technique helps to fabricate the small gap between the drain and source electrodes. In the experiment discussed below, the first layer is firstly deposited from an angle of α degrees, then the second layer is deposited from another angle of β degrees. The bridge is the remained part of the high layer of the resist after development (because it has low sensitivity and no irradiation). If the width of the bridge is W_{Bridge} and the height from the bridge to the substrate (thickness of the low layer of the resist) is H, the width of the gap W_{Gap} between the drain and source electrodes can be calculated as

$$\begin{aligned} W_{\text{Gap}} &= W_{\text{Bridge}} - (D_1 + D_2) \\ &= W_{\text{Bridge}} - H\Big[\big|\tan(\alpha)\big| + \big|\tan(\beta)\big|\Big] \end{aligned} \tag{4.1}$$

Substitution of $H = 800$ nm, $\alpha = 14°$, and $\beta = -14°$ into Eq. (4.1) gives that W_{Gap} (nm) $= W_{\text{Bridge}} -$ 400.

Lift off process uses acetone. Because the resist is dissolved in acetone, both the remained resist and metal covering it are removed. The complete electrodes are obtained after this process.

4.2.1.2 Formation of NP chains between electrodes to realize arrays of small tunnel junctions

In the experiment described below, NP chains between electrodes were formed by using one or two kinds of solutions: a citric solution consisting of 0.007% of 15-nm-diameter (or 5-nm-diameter) Au NPs and a toluene solution containing 0.1% of 3-nm-diameter Au NPs chemisorbed via decanethiol. Both of them were bought from the company. Size distributions of 5-nm and 15-nm Au NPs are shown in Fig. 4.7. The 15-nm Au NPs include a group of Au NPs with the Gaussian size distribution, in which the size range is from 10 to 30 nm and the mean is 15 nm. Figure 4.8 shows size distribution of 3-nm Au NPs without decanethiol. For the type of 3-nm Au NPs, the size range is from 2 to 5nm and the number of 3-nm Au NPs is more than 40%.

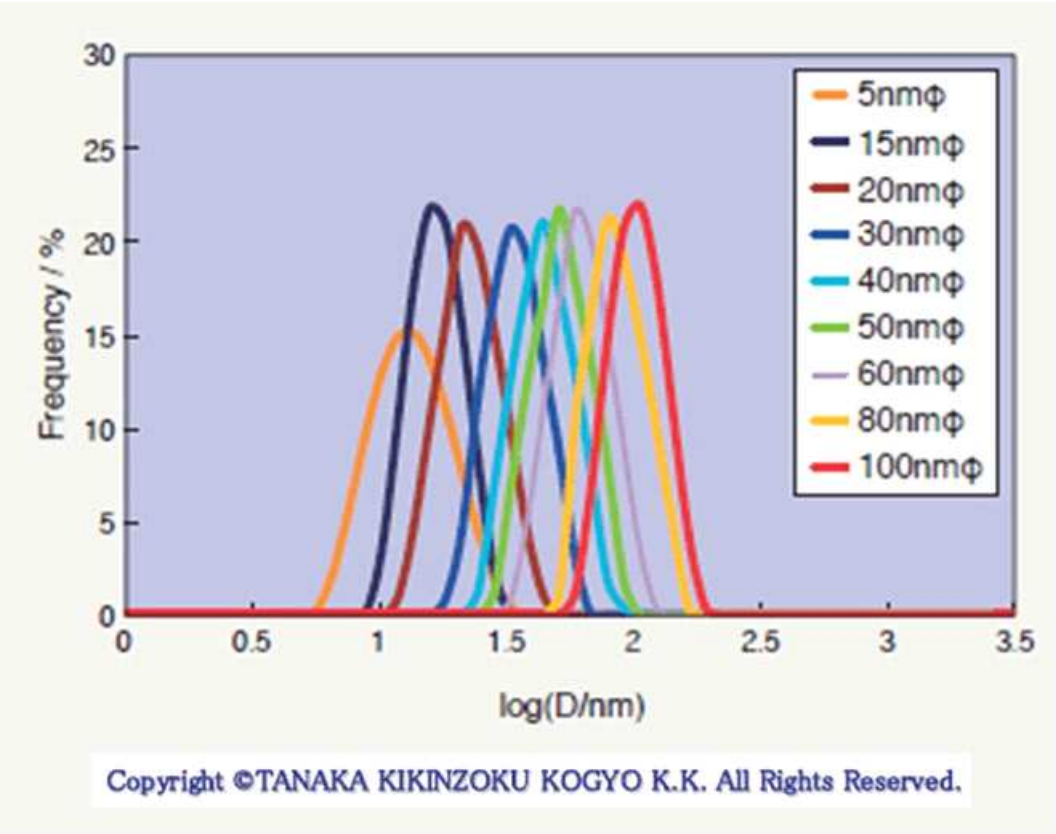


Figure 4.7: Size distributions of Au NPs. This figure is provided by Tanaka Kikinzoku Kogyo company [83].

Au NPs coated by decanethiol are formed on the basis of principle of self-assembled monolayer (SAM). SAMs are molecular assemblies formed spontaneously as the surface of solid (substrate) absorbs molecules from solution or the gas phase [82]. The most popular class of SAM is based on thiol (-SH) groups involving alkanethiols ($HS(CH_2)_nCH_3$) and alkanedithiol ($HS(CH_2)_nSH$) on a Au substrate. Alkanethiol SAM on the Au substrate is schematically illustrated in Fig. 4.9 [76]. SAM consists of three parts including a head group, a spacer/backbone, and an end group [82]. The head group is the chemisorbed contact between sulfur (S) and Au (here, Au replaces H in (H-S-) group). The backbone is the methylene ($-CH_2-$) group. The end group is the methyl (CH_3-) group and constitutes the outer part of SAM. If the number of carbon in alkanethiol is 10 ($n = 9$), it will be SAM of decanethiol. A

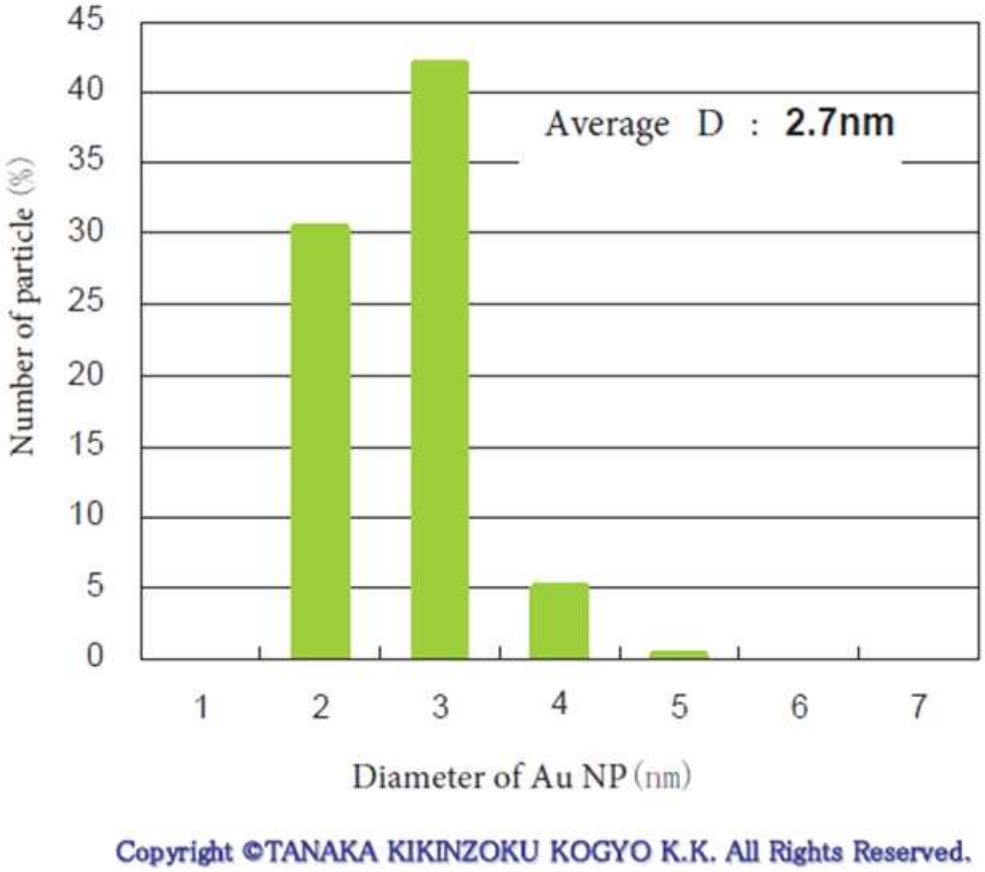


Figure 4.8: Size distribution of 3-nm-diameter Au NPs. The figure is provided by Tanaka Kikinzoku Kogyo company.

combination of this SAM with the other metal such as Au forms a molecular tunnel junction (Au-alkanethiol-Au) as shown in Fig. 4.10 [76]. In Fig. 4.10, the connection between S and Au is the chemisorbed contact whereas the connection between (CH_3-) group and Au is the physisorbed contact. Between the chemisorbed and physisorbed contacts, it is the tunnel barrier.

According to Ref. [76], two typical properties of SAM are reported as follows. Firstly, the contact resistance of the chemisorbed contact is smaller than that of the physisorbed contact. Secondly, the current has an exponential decrease with an increase of the barrier width (length of the molecule).

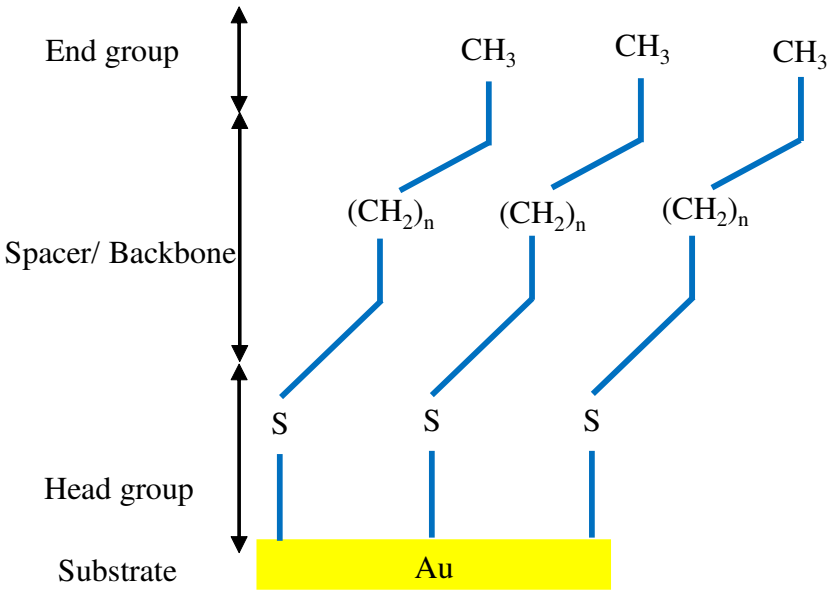


Figure 4.9: Schematic drawing of alkanethiol SAM on Au substrate.

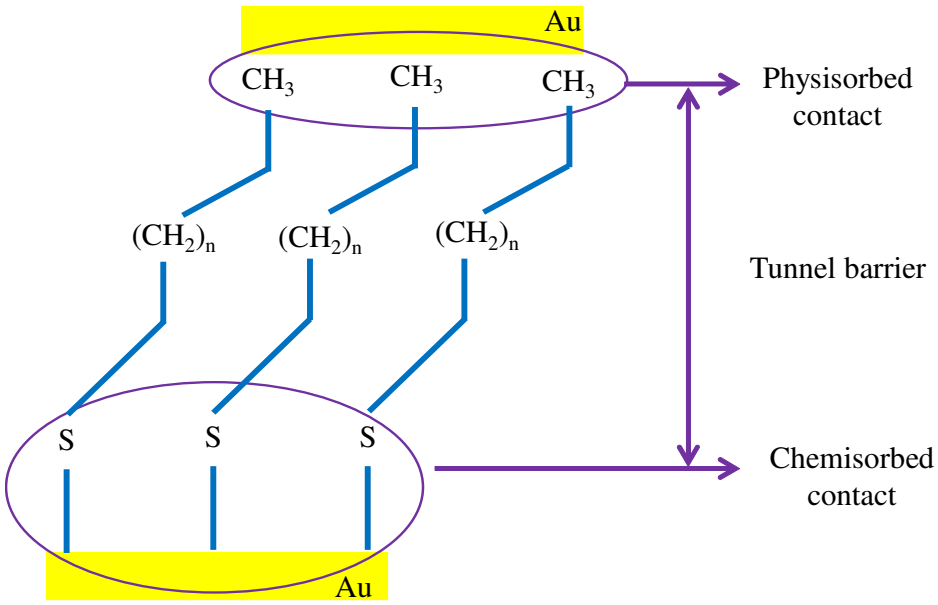


Figure 4.10: Schematic drawing of a molecular tunnel junction Au-alkanethiol-Au.

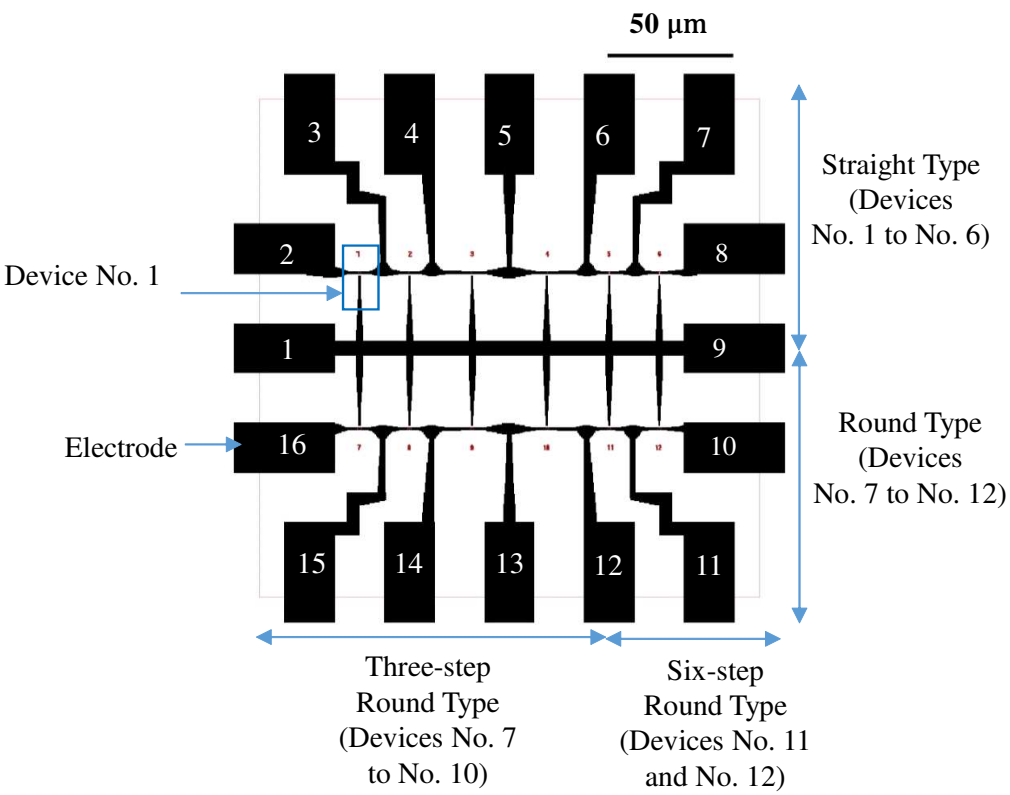


Figure 4.11: CAD layout.

4.2.2 Example of fabrication conditions

Fabrication steps to make devices having three electrodes are described below via a specific example of the fabricated chip (chip 150706C). The devices were formed on the Si chip covered by SiO_2.

4.2.2.1 CAD design

A CAD layout is shown in Fig. 4.11. 16 electrodes were designed to have 12 devices. Each device was composed of a drain electrode, a source electrode, and a gate electrode. The geometries of the drain and source electrodes were divided into a straight type, a three-step round type, and a six-step round type. The upper part includes 6 devices of the straight type (from No. 1 to No. 6). The lower part includes 4 devices of the three-step round type (from No. 7 to No. 10) and 2 devices of the six-step round type (No. 11, No. 12).

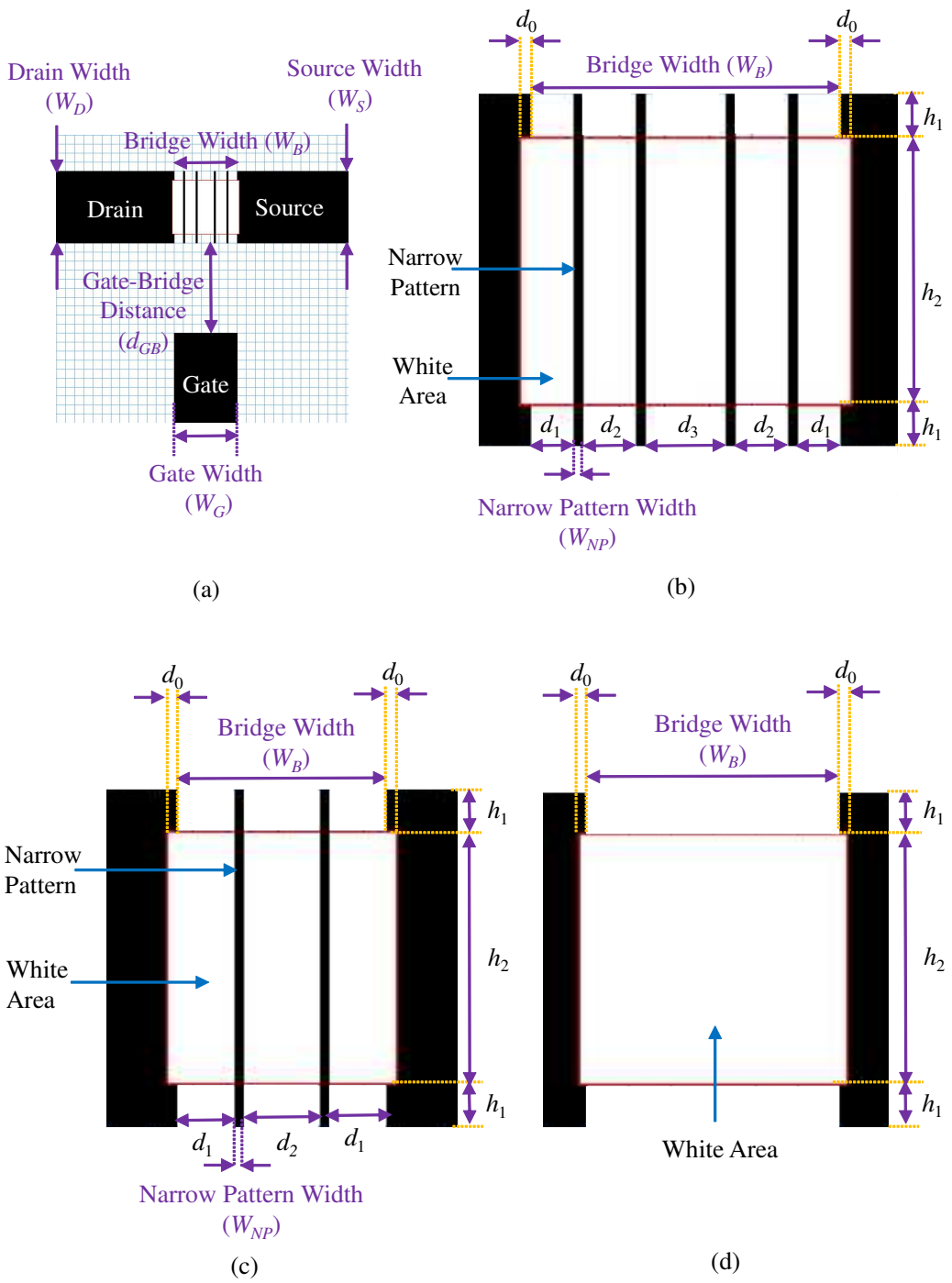


Figure 4.12: Layouts of straight type.

Designs of the straight, three-step round, and six-step round electrodes are respectively illustrated in Figs. 4.12 – 4.14. Values of all parameters in Figs. 4.12 – 4.14 are listed in Tables 4.3 – 4.5, respectively. The area between

Table 4.3: Parameter values in Fig. 4.12

Devices	Drain Width	Source Width	Gate-Bridge Distance	Narrow Pattern Width	White area		
					Horizontal Position	Vertical Positions	
	W_D (nm)	W_S (nm)	d_{GB} (nm)	W_{NP} (nm)	d_0 (nm)	h_1 (nm)	h_2 (nm)
No. 1 – 6	800	800	1000	20	20	100	600

Devices	Bridge Width	Narrow Pattern			
		Number	Horizontal Postions		
	W_B (nm)	N	d_1 (nm)	d_2 (nm)	d_3 (nm)
No. 1	700	4	100	120	180
No. 2	600	2	200	160	x
No. 3	540	2	160	180	x
No. 4	500	2	140	180	x
No. 5	600	0	x	x	x
No. 6	500	0	x	x	x

the drain and source electrodes is called a bridge. Inside the bridge, there are narrow patterns which help to increase the solubility of the low layer of the resist during development process. The white area was designed to decrease the proximity effect from EB drawing. All the devices had the same width ($W_D = W_S = 800$ nm) of the drain and source electrodes, the same distance from the gate to the bridge ($d_{GB} = 1000$ nm), and the same width of the narrow patterns ($W_{NP} = 20$ nm). The widths of the gate electrodes were designed to be equal to the widths of the bridge. The widths of the bridge were changed from 700 nm to 500 nm, resulting in the expected equivalent gaps from 300 nm to 100 nm after shadow evaporation.

For the straight type, the number of narrow patterns N was decreased

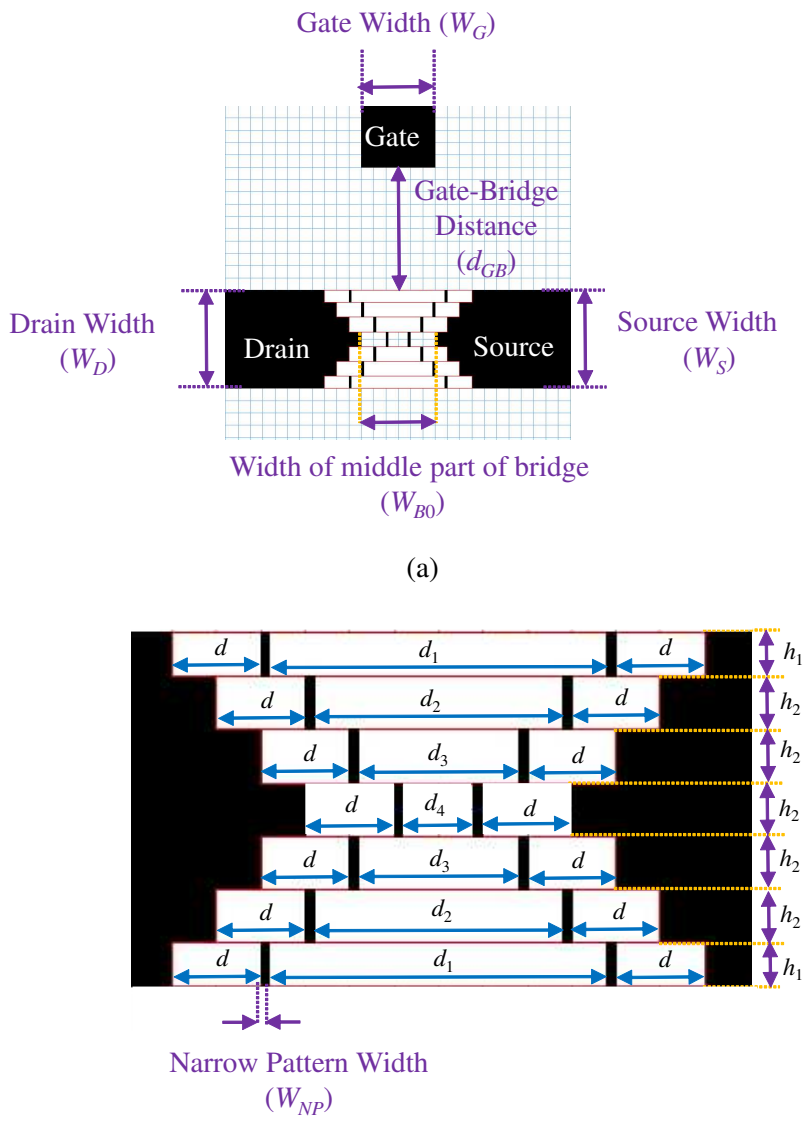


Figure 4.13: Layouts of three-step round type.

as the width of the bridge was reduced as shown in Table 4.3. Besides, the narrow bridge (600 nm and 500 nm) were desiged in two cases of having narrow patterns and without narrow patterns.

For the round type, all devices had the same $N = 2$. Shapes of the three-step and six-step round types are shown in Figs. 4.13 and 4.14, respectively. From the center of the bridge, the three-step round type has three upstairs and three downstairs, whereas the six-step round type has six upstairs and six

Table 4.4: Parameter values in Fig. 4.13

Devices	Drain Width	Source Width	Gate-Bridge Distance	Narrow Pattern Width	Vertical sizes of Bridge	
	W_D (nm)	W_S (nm)	d_{GB} (nm)	W_{NP} (nm)	h_1 (nm)	h_2 (nm)
No. $7-10$	800	800	1000	20	100	120

Devices	Width of middle part of Bridge	Narrow Pattern					
		Number	Horizontal positions				
	W_{B0} (nm)	N	d (nm)	d_1 (nm)	d_2 (nm)	d_3 (nm)	d_4 (nm)
No. 7	700	2	200	860	660	460	260
No. 8	600	2	200	760	560	360	160
No. 9	540	2	160	780	580	380	180
No. 10	500	2	160	740	540	340	140

downstairs. In each device, positions of the narrow patterns and the white areas are distributed symmetrically with repsect to the center of the bridge.

4.2.2.2 Fabrication steps

First of all, a SiO_2/Si chip was coated by a bi-layer resist. The resist consisted of a low layer and a high layer with a large difference in sensitivity. To have high sensitivity, the low layer was made of Copolymer in 11% Ethyl Lactate (EL11), spinned at 1500 rpm (rounds per minute), and prebaked at 170 °C in 2 minutes. Consequently, the thickness of the low layer was 800 nm (Fig. 4.1). To have low sensitivity, the high layer was formed by PMMA in 2% Anisole (A2), spinned at 4000 rpm, and prebaked at 170 °C in 3.5 minutes. As a result, the thickness of the high layer was 60 nm (Fig. 4.2).

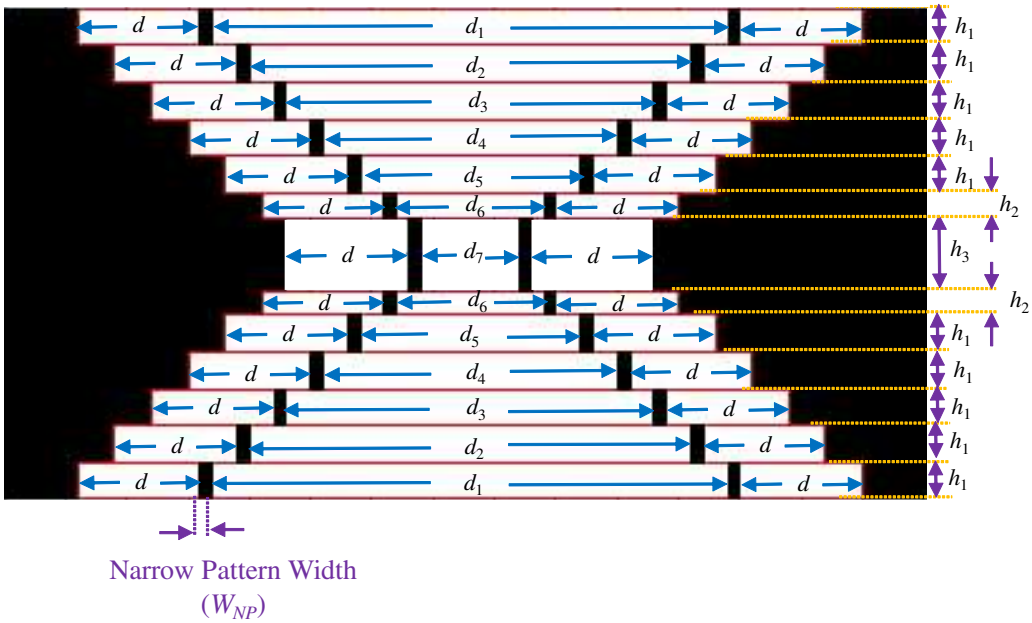


Figure 4.14: Layout of six-step round type.

Table 4.5: Parameter values in Fig. 4.14

Devices	Drain Width	Source Width	Gate-Bridge Distance	Narrow Pattern Width	Vertical sizes of Bridge		
	W_D (nm)	W_S (nm)	d_{GB} (nm)	W_{NP} (nm)	h_1 (nm)	h_2 (nm)	h_3 (nm)
No. 11, No. 12	800	800	1000	20	60	40	120

Devices	Width of middle part of Bridge	Narrow Pattern								
		Number	Horizontal positions							
	W_B (nm)	N	d (nm)	d_1 (nm)	d_2 (nm)	d_3 (nm)	d_4 (nm)	d_5 (nm)	d_6 (nm)	d_7 (nm)
No. 11	600	2	200	840	720	600	480	360	240	160
No. 12	500	2	140	860	740	620	500	380	260	180

Second, the chip coated by resist was written with the above CAD layouts

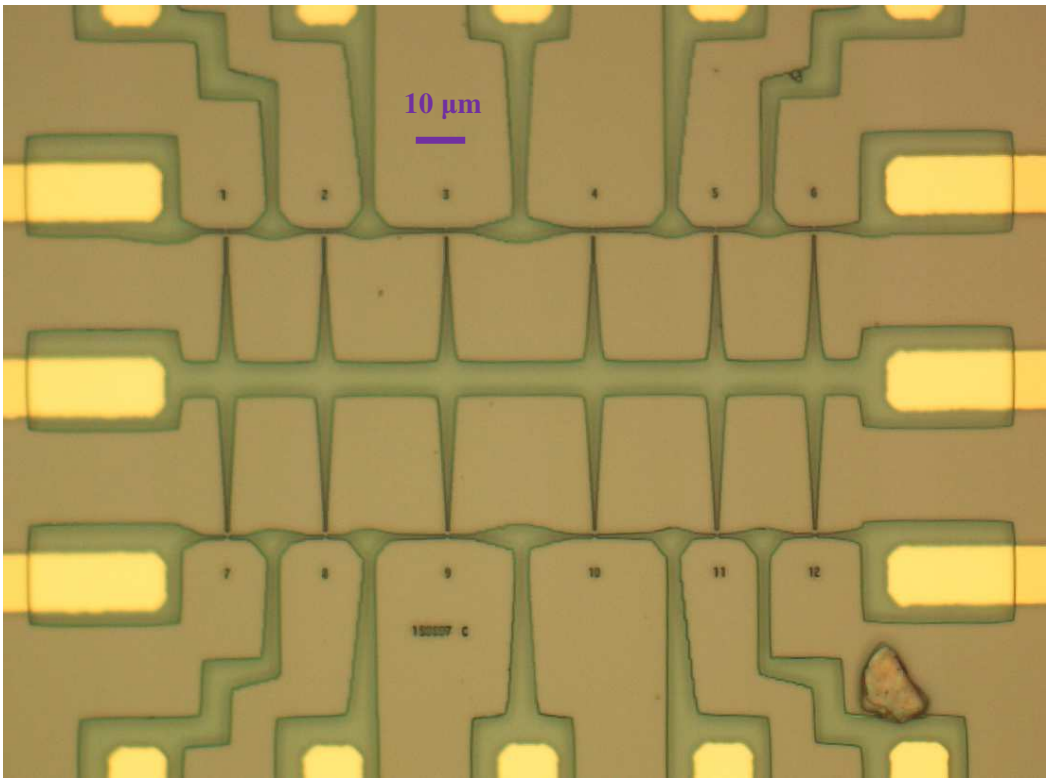
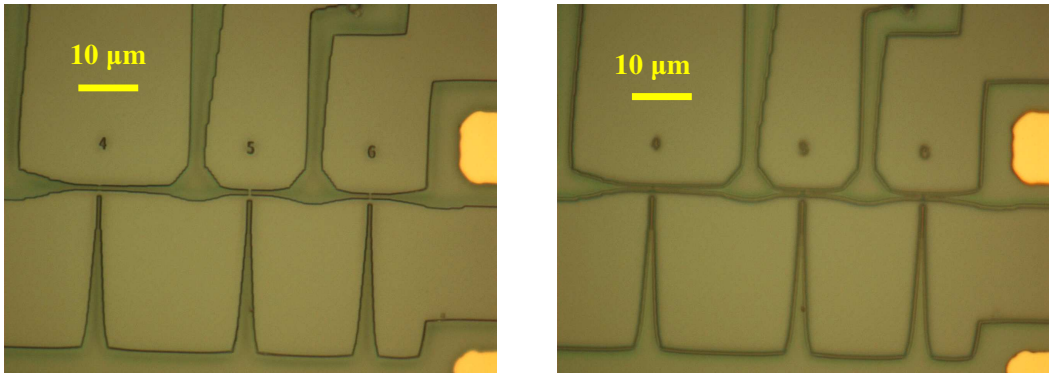


Figure 4.15: Optical micrograph of 16 electrodes after development.

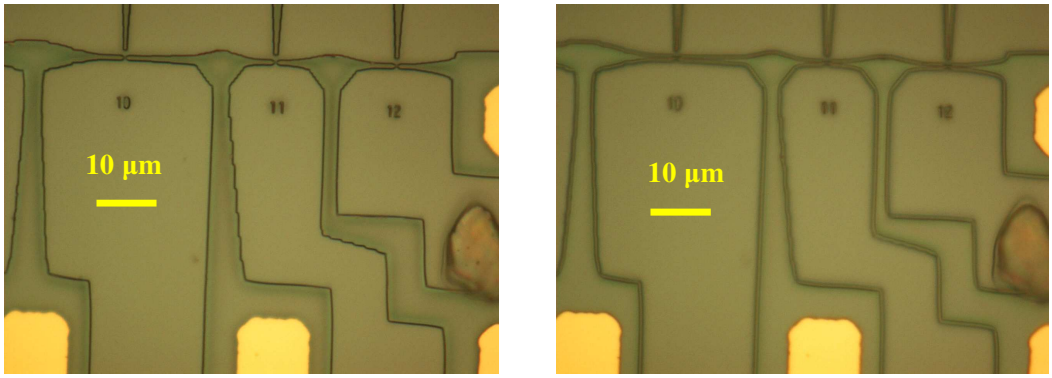


(a) (b)

Figure 4.16: Optical micrographs of straight type (Devices No. 4, No. 5, and No. 6) after development. (a) Upper layer. (b) Lower layer.

by using the standard EBL under the condition of 120-pA beam current and 5-μs/pixel dose time.

Third, Isoproponal alcohol (IPA) mixed with pure water (H_2O) with a ratio



(a) (b)

Figure 4.17: Optical micrographs of three-step round type (Devices No. 10) and six-step round type (Devices No. 11 and No. 12) after development. (a) Upper layer. (b) Lower layer.

of 10 : 1 was used as development solvent. An ultrasonic bath was used to make the solvent homogeneously. The development processes: the chip was firstly immersed in the developer glass in 175 s, followed by being rinsed in the first H_2O glass in 30 s, and rinsed in the second H_2O glass in 10 s. After the development processes, the optical micrographs of the total 16 electrodes, the straight-type devices, and the round-type devices are respectively shown in Figs. 4.15 − 4.17.

Fourth, 16 electrodes were formed in vacuum less than 1×10^{-5} Torr by using shadow evaporation of NiCr with a deposition rate of 0.1 nm/s. The first layer of 20-nm thickness was evaporated from the angle of 166°. The second layer of 45-nm thickness was evaporated from the angle of −166°.

Final, lift off process was done by immersing the chip in the acetone solution for 1 hour. Then, the chip was dried by Nitrogen gas.

The scanning electron microscopy (SEM) images of the straight type, three-step-round type, and six-step-round type devices are respectively illustrated in Figs. 4.18 − 4.20. The width of the gap W_{gap} is defined as the distance between the middle point of the drain electrode to the midlle point of the source

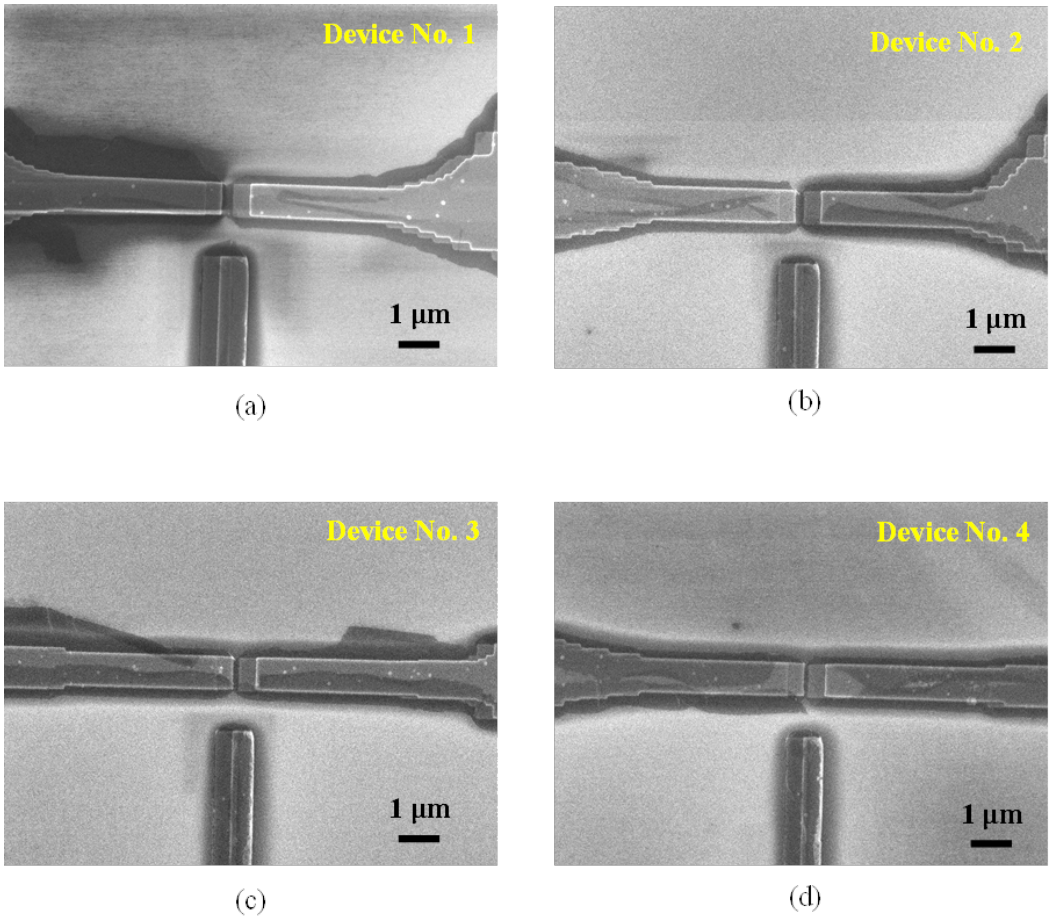


Figure 4.18: Scanning electron microscopy (SEM) images of the straight type. (a) Device No. 1. (b) Device No. 2. (c) Device No. 3. (d) Device No. 4

electrode as shown in Fig. 4.21. The measurement gap width is measured on SEM images. The design gap width is calculated on the basis of the model of shadow evaporation (Fig. 4.6). The design (triangle points) and meaurement (circle points) gap widths are compared in Fig. 4.22. It can be seen that the measurement results are close to the design results. This indicates that the design and measurement results are in good agreement.

For straight type (Devices No. 1 to No. 6 in Fig. 4.22), the difference between the measurement gap width and the design gap width can be driven from the number of narrow patterns as follows. The device No. 1 had 4 narrow patterns, which could cause over-dose of EB. As a result, a part of

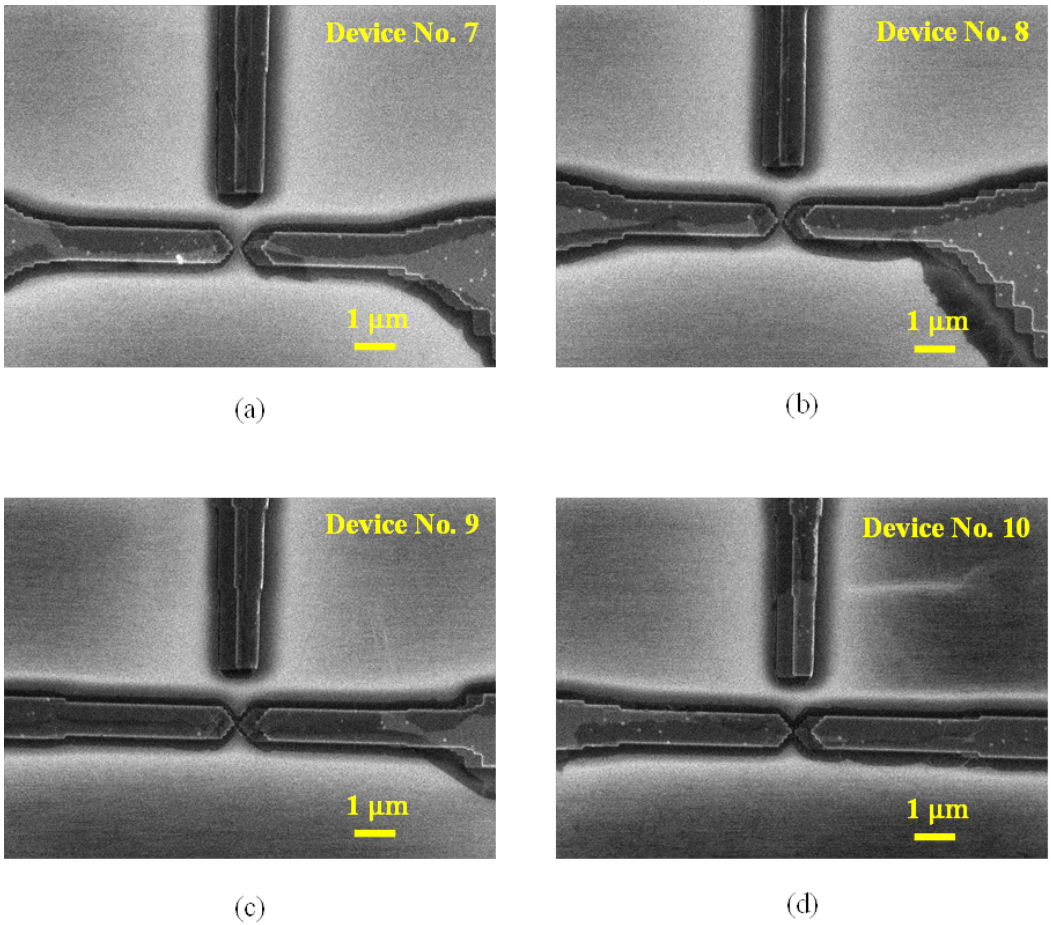
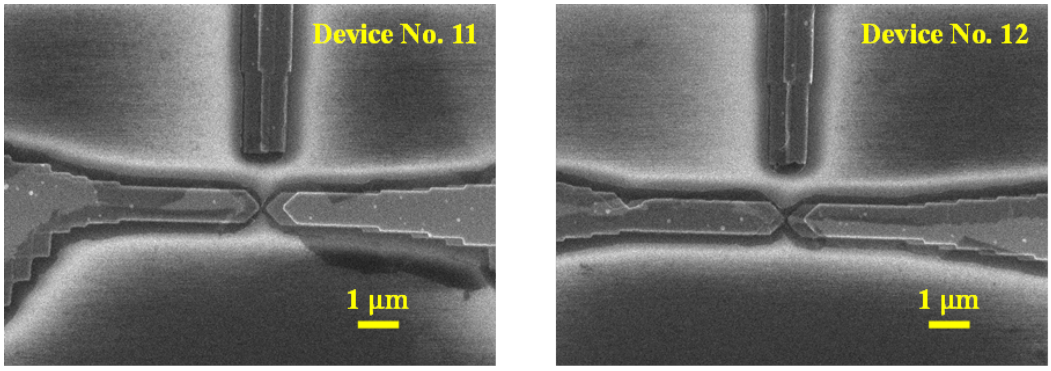


Figure 4.19: Scanning electron microscopy (SEM) images of the three-step round type. (a) Device No. 7. (b) Device No. 8. (c) Device No. 9. (d) Device No. 10.

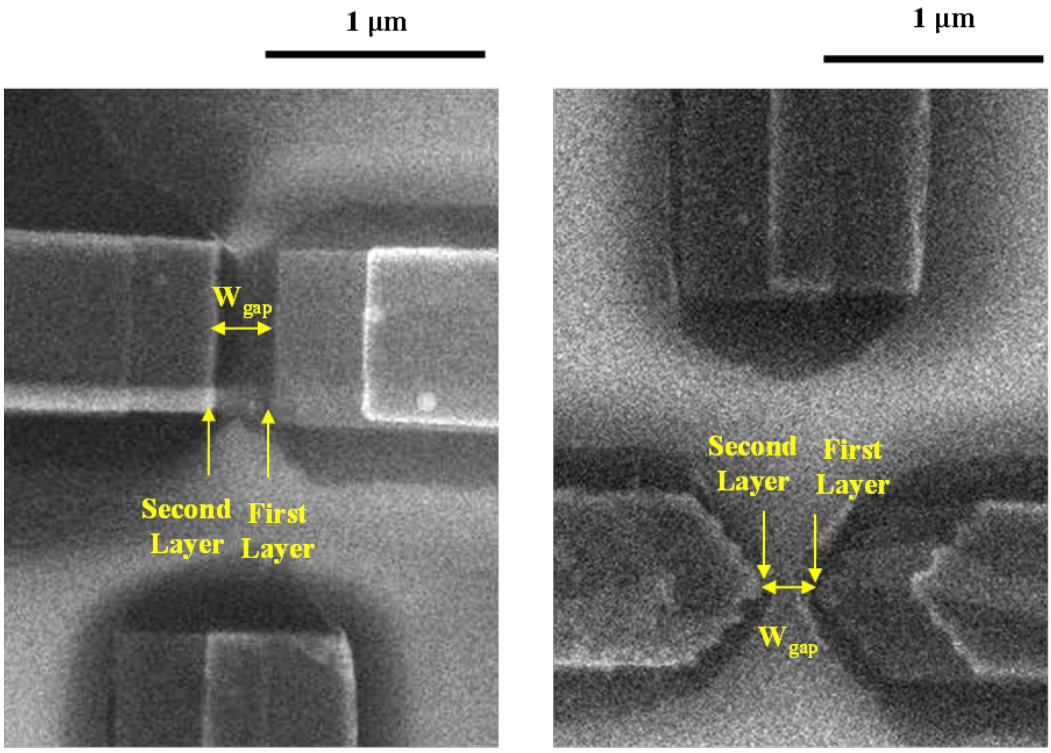
high layer of resist in the bridge area was removed by development. This is called overdevelopment, resulting in a smaller measurement gap than the design gap. In contrast, the device No. 5 had a relatively wide bridge (600 nm) and no narrow patterns. Therefore, a part of low layer of resist under the bridge still existed after development. This was judged as under-development or insufficient undercut. Consequently, the measurement gap was larger than the design gap.

For the round type (Devices No. 7 to No. 12 in Fig. 4.22), the measurement gap widths were smaller than the design gap widths. Here, the origin of



(a) (b)

Figure 4.20: Scanning electron microscopy (SEM) images of the six-step round type. (a) Device No. 11. (b) Device No. 12



(a) (b)

Figure 4.21: Definition of gap widths for straight and round types. (a) Straight type. (b) Round type.

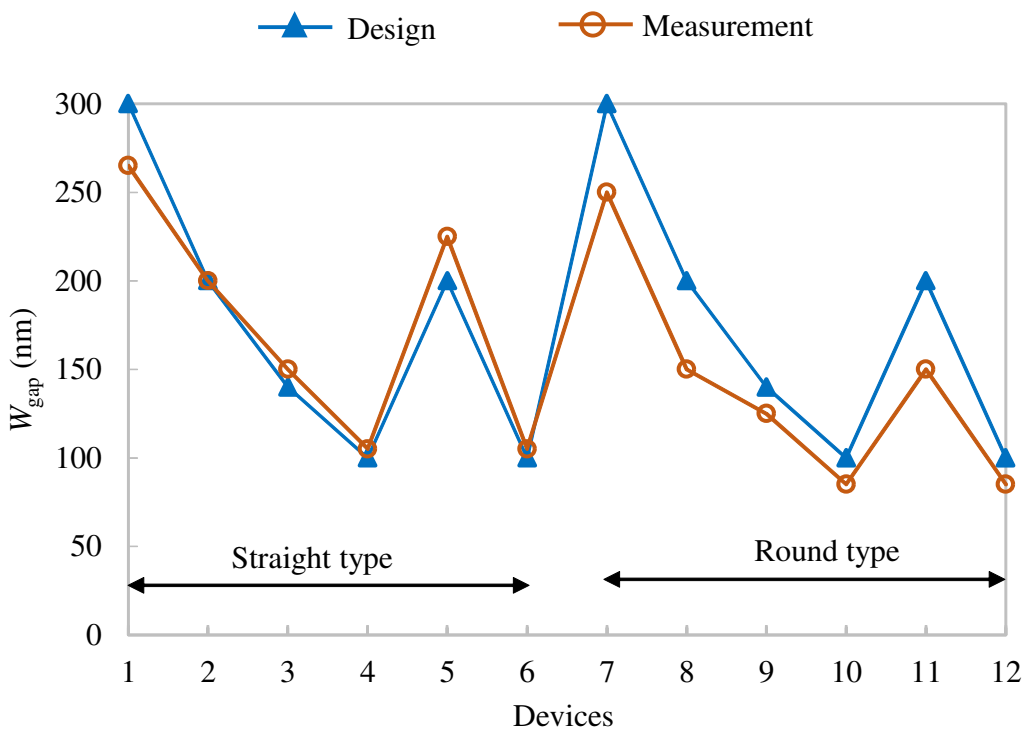


Figure 4.22: Design and measurement gap widths of the devices composed of three electrodes. Straight type includes the devices from No. 1 to No. 6. Round type includes the devices from No. 7 to No. 12.

the overdevelopment phenomena can arise from the increase of the proximity effects when the drain and source patterns were composed of many steps.

4.3 Device I

4.3.1 Fabrication Method

Fabrication processes of the device I consisted of two following steps.

Firstly, drain, source, and gate electrodes were simultaneously fabricated by using EBL, shadow evaporation of 20-nm-thick and 45-nm-thick Au, and lift off process. An optical micrograph of the device after lift off is shown in Fig. 4.23(a). Widths of the drain, source, and gate electrodes are larger than 800 nm. The gap width W_{gap} is 1000 nm. Distance from the gate electrode to

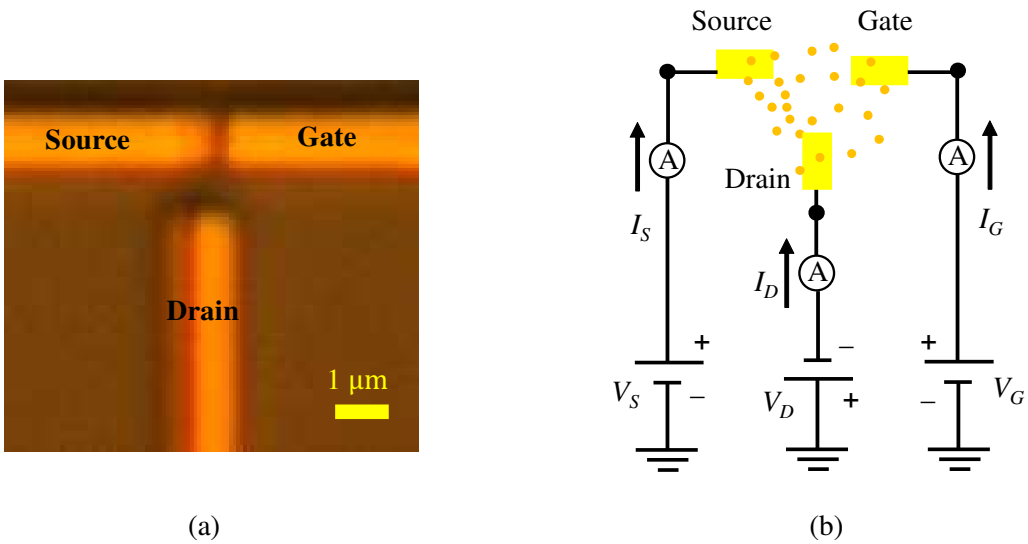


Figure 4.23: (a) Optical micrograph of the device I after lift off (chip 151202A No. 2). (b) Measurement circuit using a seminconductor parameter analyzer (SPA). Drain, source, and gate electrodes are illustrated by yellow rectangles. Au NPs are distributed randomly between the electrodes.

the source electrode is approximatly 250 nm.

Secondly, arrays of small tunnel junctions were formed by dropping a solution of Au NPs. Namely, 7 μL of an aqueous solution of citric acid containing 0.007 wt% of 15-nm-diameter Au NPs was dropped on the device. After dropping, the solution of Au NPs was dried by keeping the chip at the room temperature (289 K).

The fabricated device was cooled by dipping into liquid nitrogen and measured by using a semiconductor parameter analyzer (SPA). A model of set-up measurement is illustrated in Fig. 4.23(b). Current values through all three voltage-biased terminals were measured.

4.3.2 Results and Discussion

Figure 4.24 shows measured currents versus drain-source voltage V_{DS} at 77 K. The currents at different gate voltages V_G of 0.000 V, 0.015 V, and 0.030

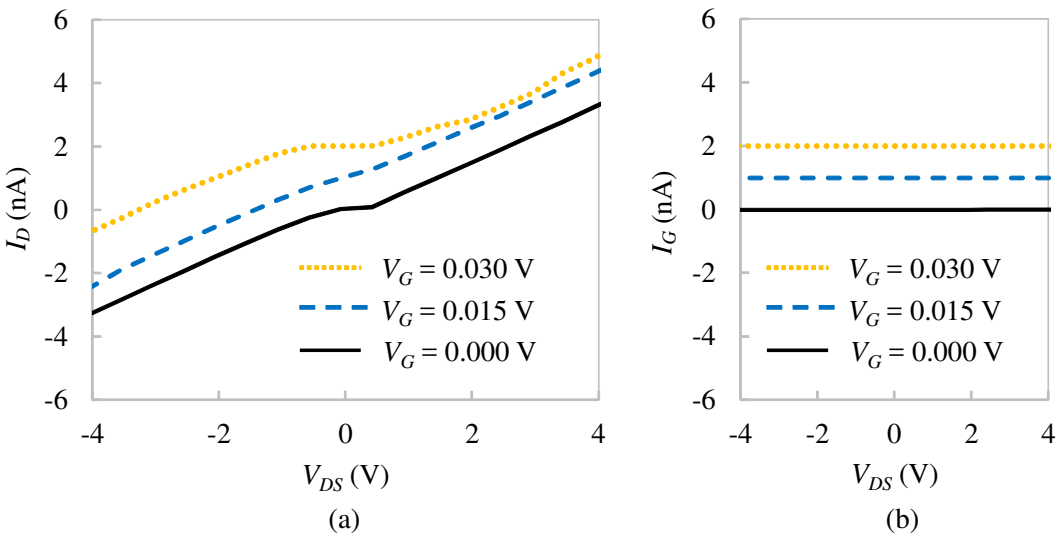


Figure 4.24: Measured currents of the device I at 77 K as gate voltage V_G varies from 0.000 V to 0.030 V in 0.015 V steps. For clarity, from $V_G = 0.000$ V to 0.030 V (from bottom to top), the curves are shifted from 0 nA to 2 nA with an offset 1 nA for each 0.015 V step. (a) Drain currents I_D versus drain-source voltage V_{DS}. (b) Gate currents I_G are plotted as functions of V_{DS}.

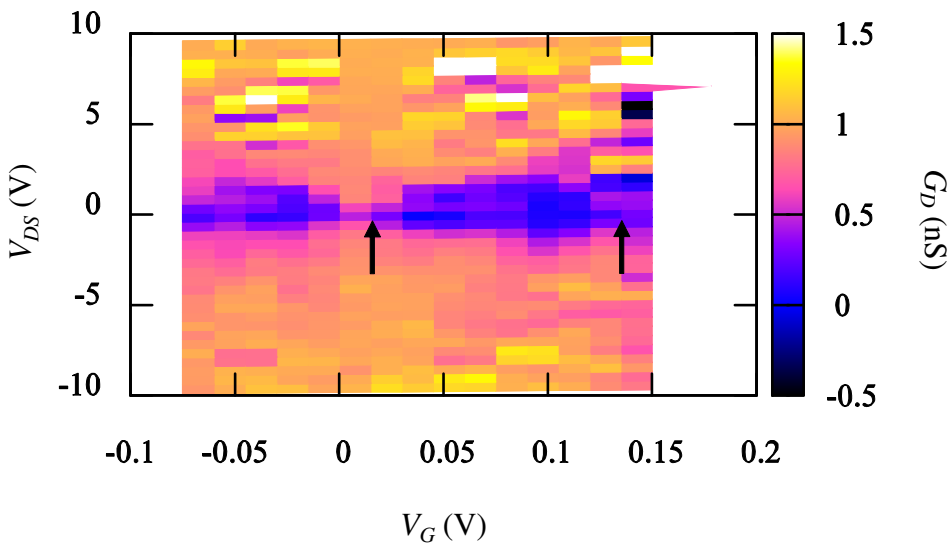


Figure 4.25: Drain conductances of the device I, $G_D = dI_D/dV_{DS}$, are plotted as functions of drain-source voltage V_{DS} and gate voltage V_G at 77 K.

V are represented by solid, dahsed, and dotted curves, respectively. A region is defined as Coulomb blockade (CB) if absolute drain current $|I_D|$ is smaller than 0.05 nA. At $V_G = 0.000$ V, the CB region is observed between $V_{DS} = -0.2$ and 0.15 V (Fig. 4.24(a)). The CB region disappears when V_G increases to 0.015 V, and appears again when V_G rises further to 0.030 V. This indicates the Coulomb oscillation. Figure 4.24(b) shows that all gate currents I_G are almost zero ($|I_G| < 15$ pA). This means that there is no resistive connection from the gate electrode to the gap between the drain and source electrodes.

Drain conductance, $G_D = dI_D/dV_{DS}$, plotted as functions of V_{DS} and V_G is illustrated in Fig. 4.25. Blue areas represent the regions with small G_D ($G_D <$ 0.5 nS). Periodic Coulomb oscillations are observed with a period ΔV_G of 0.12 V. Such the characteristics are categorized into a C-SET type.

4.4 Device II

4.4.1 Fabrication Method

The fabrication processes of the device II consisted of four steps as follows. Firstly, on the SiO_2/Si chip, a narrow gate electrode was formed by using a single PMMA resist, standard EBL, thermal evapration, and lift off process. Secondly, on the chip containing the gate electrode, drain and source electrodes were made by using PMMA/copolymer bi-layer resist, EBL, shadow evaporation of 20-nm-thick Au and 45-nm-thick Au, and lift off process. CAD layouts for EBL and optical micrographs after lift off in the first and the second steps are respectively shown in Figs. 4.26 and 4.27. Thirdly, 5 μL of a citric acid solution containing 0.007 wt% of 15-nm-diameter Au NPs was dropped on the chip. Finally, 3 μL of a toluene solution consisting of 0.1 wt% of 3-nm-diameter Au NPs was dropped on the chip. After dropping, the solutions of Au NPs were dried by keeping the chip at the room temperature (287 K).

The measurement circuit using SPA was established as shown in Fig. 4.28. Voltages were applied to the drain and source terminals have the same magnitude and opposite polarity. The device was dipped into liquid nitrogen to

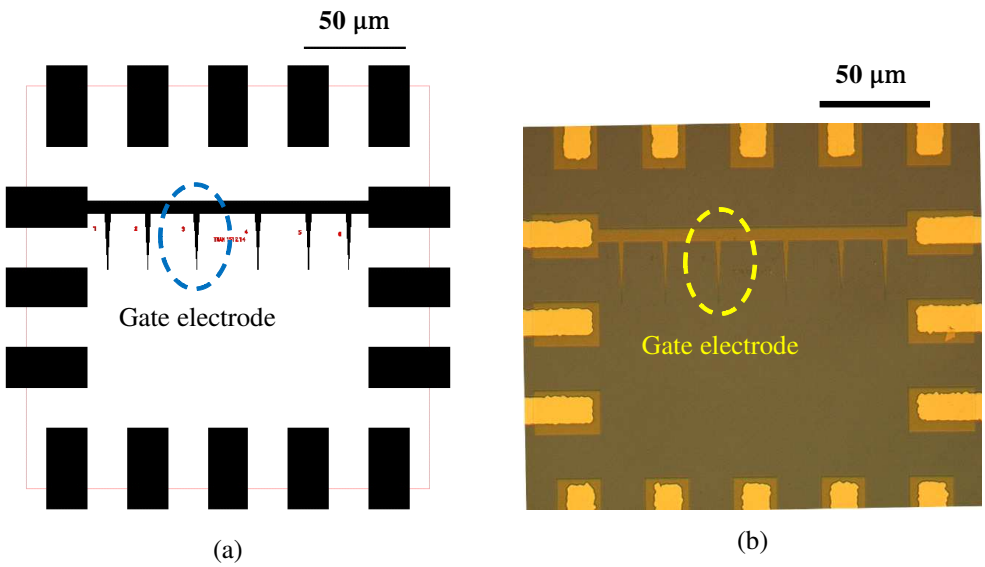


Figure 4.26: Gate electrode of the device II. (a) CAD layout for EBL. (b) Optical micrograph after lift off.

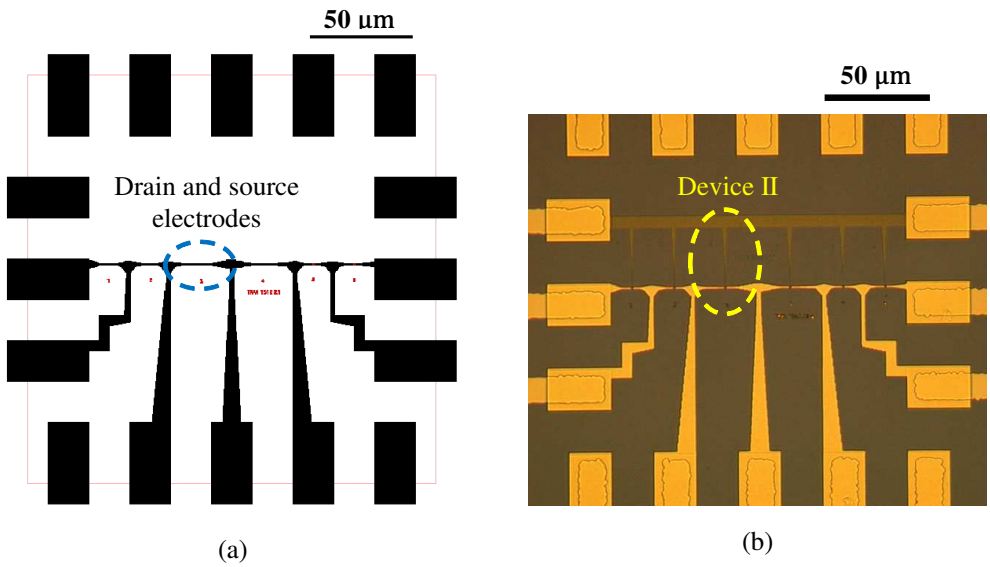


Figure 4.27: (a) CAD layout of drain and source electrodes of the device II. (b) Optical micrograph of the device II after lift off.

measure its characteristics at 77 K.

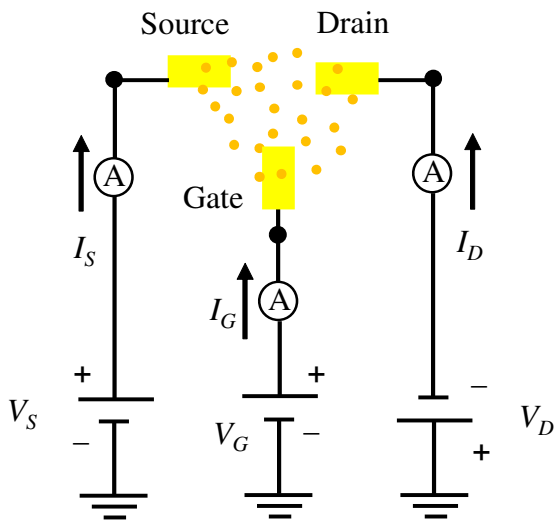


Figure 4.28: Measurement circuit of the device uses semiconductor parameter analyzer (SPA). Drain, source, and gate electrodes are illustrated by yellow rectangles. Au NPs are distributed randomly between the electrodes.

4.4.2 Results and Discussion at 77 K

4.4.2.1 Characteristics at 77 K

Figure 4.29 shows a SEM image of the device II. The gate electrode made of 10-nm-thick Au has a narrow width of 70 nm. The drain and source electrodes have the same width of 800 nm. Between the drain and source electrodes, there is the 200-nm-wide gap. The gate electrode penetrates 190 nm into the gap. It is observed that an array of Au NPs consisting of parallel branches was constituted between the drain and source electrodes (Fig. 4.29(c)). Additionally, a part of the array connects to the gate electrode.

Currents versus drain-source voltage V_{DS} of the device II measured at 77 K are shown in Fig. 4.30. The currents at different gate voltages V_G of −25 V, 0 V, and +25 V are respectively represented by dotted, solid, and dashed curves. Figure 4.30(a) shows drain currents I_D. Again, a CB region is defined as the region where the absolute drain current is smaller than 0.05 nA ($|I_D| < 0.05$ nA). At $V_G = 0$, there is a CB region between $V_{DS} = -5.4$ V and +4.2 V. The

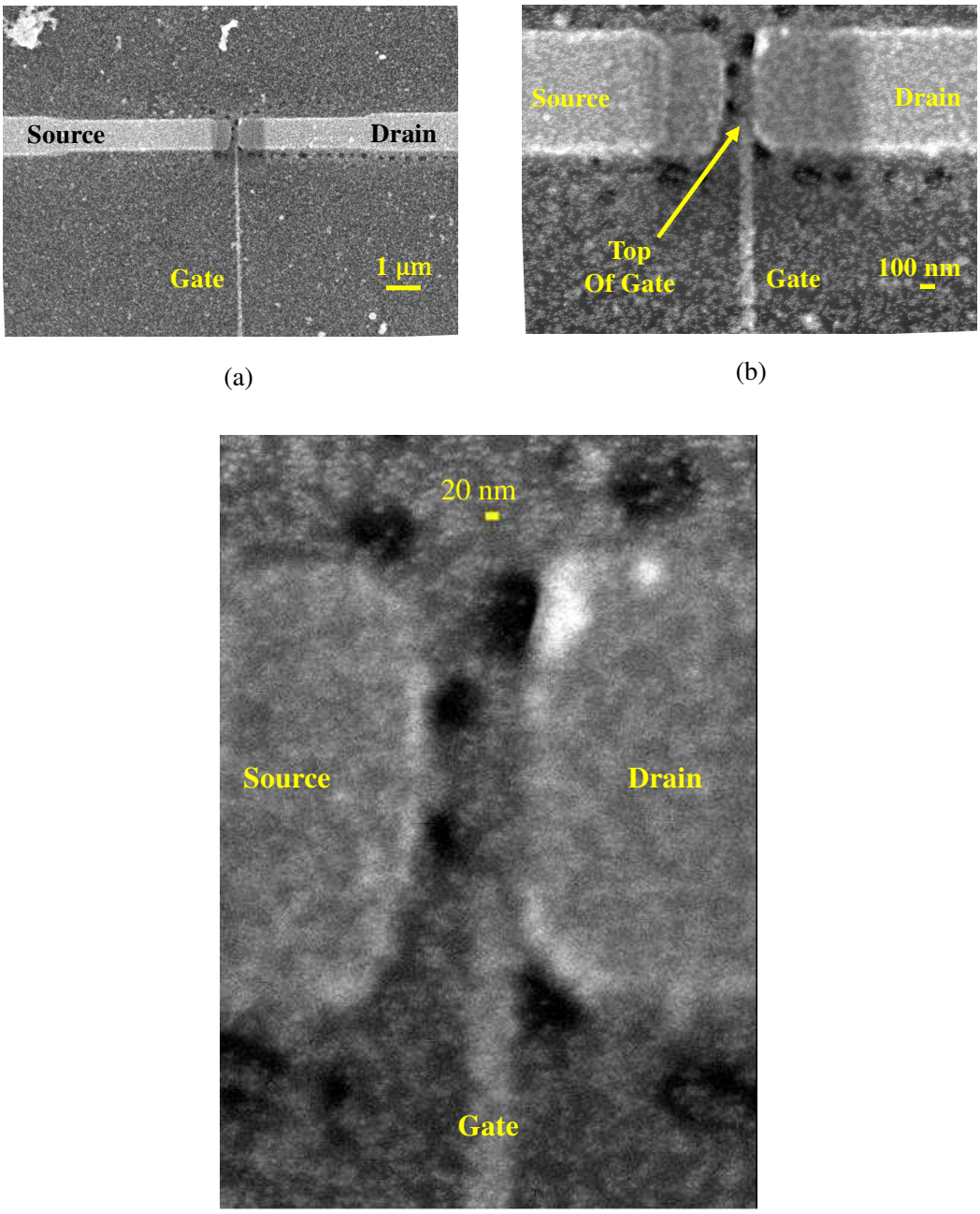


Figure 4.29: Scanning electron microscopy (SEM) images of the device II (chip 151214_21B No. 3) after measurment at different scales. Top of gate electrode is shown by a yellow arrow. Small white dots are Au NPs.

absolutely smaller value V_{DS} of 4.2 V is chosen as an absolute threshold voltage $(V_{DS})_{\mathrm{th}}$ of the device II at 77 K. Besides, gate currents I_G are illustrated in

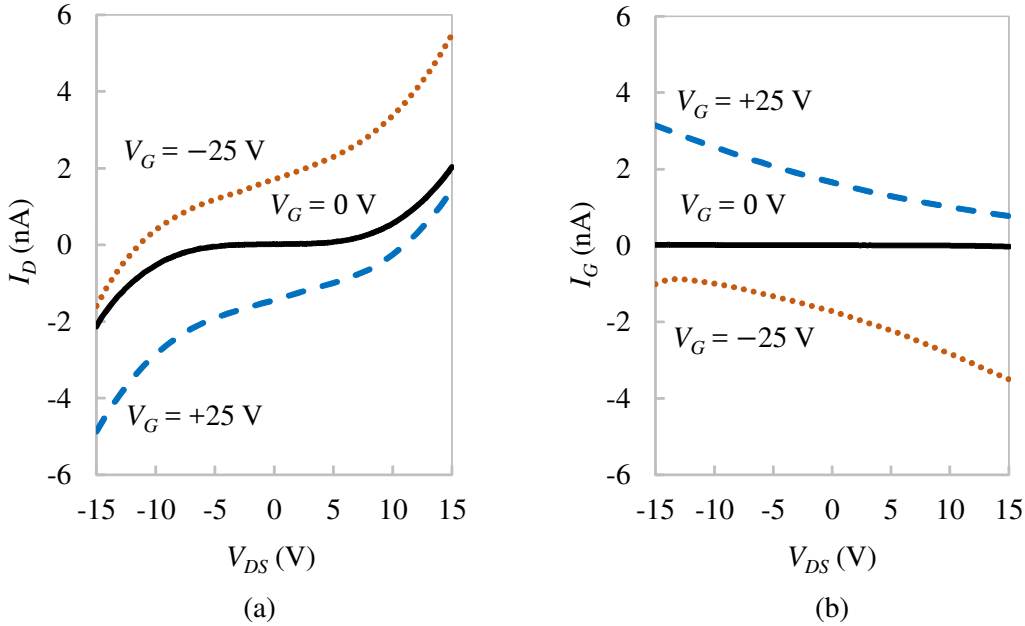


Figure 4.30: Measured currents of the device II at 77 K and at different gate voltages of −25 V, 0 V, and +25 V. (a) Drain currents I_D versus drain-source voltage V_{DS}. (b) Gate currents I_G are plotted as functions of V_{DS}.

Fig. 4.30(b). Although the absolute gate current $|I_G|$ is smaller than 0.03 nA at $V_G = 0$, it becomes large (a few nA) at $V_G = \pm 25$ V. This indicates that when non-zero V_G was applied to the device II, I_G flew through the device. Therefore, the characteristics of the device II are categorized into those of R-SET type. In addition, the relationship between I_D and I_G is not linear, in which the absolute ratios $|I_D/I_G|$ can be larger than unity at several values of V_{DS} and V_G. For instance, $|I_D/I_G| > 1.0$ when $V_G = -25$ V and V_{DS} is in the range from 2.0 V to 15 V.

The relationship between I_D versus V_G and V_{DS} in details is illustrated in Fig. 4.31(a). White and black areas show I_D over +1.0 nA and under −1.0 nA. The CB region ($|I_D| < 0.05$ nA) is depicted by a pink area surrounded by light blue ($I_D = -0.05$ nA) and blue ($I_D = +0.05$ nA) contour curves. This CB region mainly appears in the ranges of V_G from −6 V to +6 V and V_{DS} from −4V to +4 V. Drain conductance, $G_D = dI_D/dV_{DS}$, is plotted on the

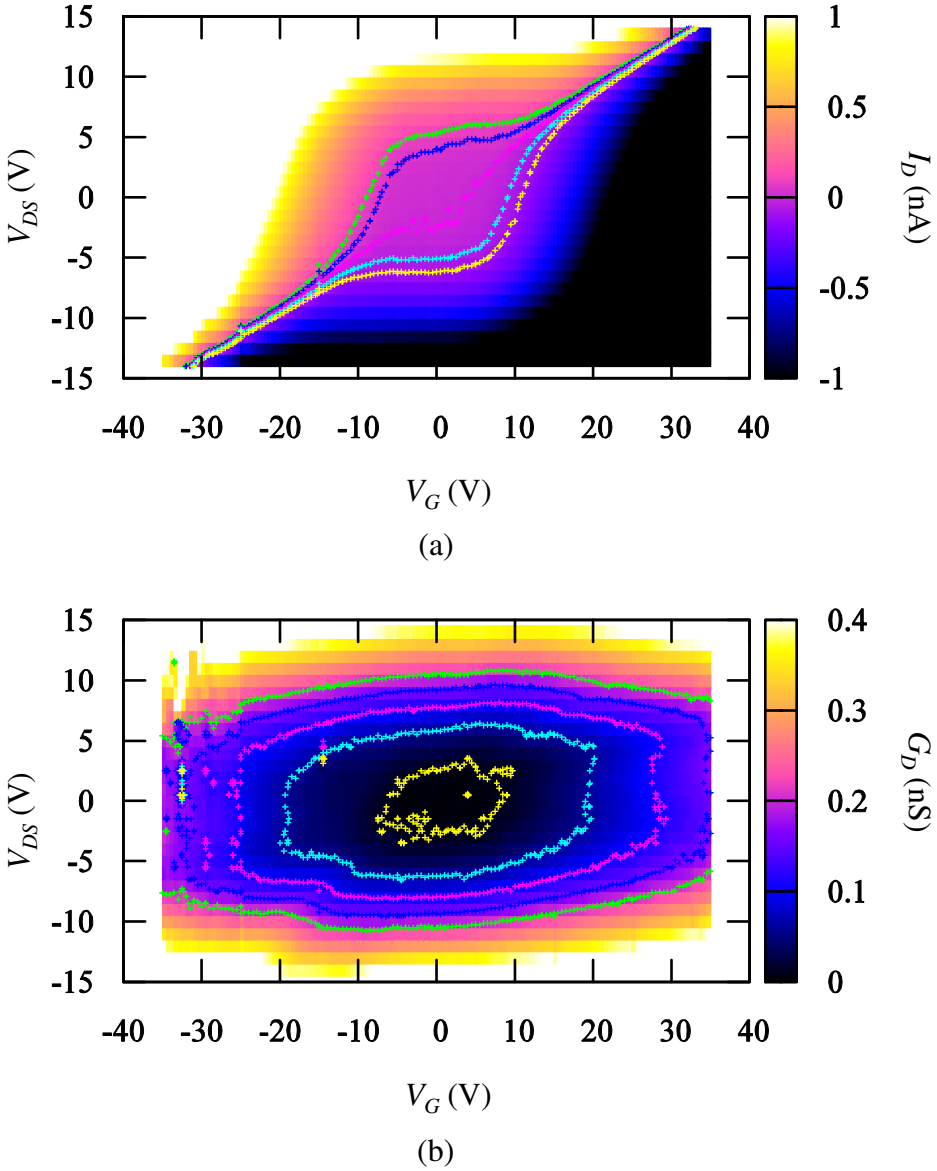


Figure 4.31: Measured drain current and conductance of the device II at 77 K. Defined colors of contour curves are different from those in the color bars. (a) Measured drain currents I_D versus gate voltage V_G and drain-source voltage V_{DS}. I_D from -0.1 nA to $+0.1$ nA are illustrated by contour curves (from bottom to top) in 0.05 nA steps. (b) Drain conductances, $G_D = dI_D/dV_{DS}$, are plotted as functions of V_G and V_{DS}. G_D from 0.01 nS to 0.21 nS are shown by contour curves in 0.05 nS steps.

$V_{DS} - V_G$ plane in Fig. 4.31(b). G_D less than 0.01 nS is represented by a black area surrounded by a yellow ellipse. At $V_{DS} = 0$ V, $G_D > 0.1$ nS (a pink ellipse) when $V_G \geq 25$ V. Thus, the experimental results did not exhibit the Coulomb oscillations.

4.4.2.2 Discussion

Effective charging energy of the device II, $(E_C)_{\mathrm{exp}}$, is estimated from the characteristics of the device at 77 K as follows. According to the calculation for a symmetrically biased R-SET model in Ref [28], the total capacitance C_Σ becomes $e/(V_{DS})_{\mathrm{th}}$. In Sect. 4.4.2.1, the absolute threshold voltage $(V_{DS})_{\mathrm{th}}$ of the device II at 77 K is observed as 4.2 V. Therefore, $(E_C)_{\mathrm{exp}}$ is calculated as

$$\begin{aligned}(E_C)_{\mathrm{exp}} &= \frac{e^2}{2C_\Sigma} \\ &= \frac{e(V_{DS})_{\mathrm{th}}}{2} \\ &= 2.1 \quad eV \end{aligned} \tag{4.2}$$

The Au NP array consisting of the parallel branches between the drain and source electrodes in Fig. 4.29(b) is simply modelled into parallel branches of tunnel junctions. Each branch consists of tunnel junctions in series. In addition, 3-nm Au NPs chemisorbed via decanethiol are assumed to work as islands whereas 15-nm Au NPs are assumed to be conductive bridges. Since the 200-nm-wide gap of the device is over 60 times longer than the diameter of one 3-nm Au NP, there should be tens of 3-nm Au NPs on each branch.

Effective charging energy of one island (3-nm Au NP) is calculated from the geometry of the device II, E_{C1}, as follows. The self-capacitance C_{self} of one island is simply calculated as [84],

$$C_{\mathrm{self}} = 4\pi\varepsilon_0\varepsilon_{\mathrm{d1}}r, \tag{4.3}$$

where

ε_0 is the vacuum permittivity (8.854 $\times 10^{-12}$ F/m);

$\varepsilon_{\mathrm{d1}}$ is the dielectric constant of SiO_2;

r is the radius of the island (1.5 nm).

Then, C_{self} is estimated as 0.667 aF. The mutual (tunnel) capacitance C_{m} between two 3-nm Au NPs is simply calculated as below [84],

$$C_{\mathrm{m}} = 2\pi\varepsilon_0\varepsilon_{\mathrm{d2}}\sqrt{d^2 - r^2}\sum_{i=1}^{\infty}\frac{1}{\sinh(i\mathrm{arcosh}(d/r))} \tag{4.4}$$

in which $\varepsilon_{\mathrm{d2}}$ is the dielectric constant of decanethiol (2.6) [14]; d is a half of the distance between two NP centers: $2d = 2r + w$. Here, w is the space between two Au NPs, working as a tunnel barrier. For simplification, w is assumed to be 1 nm. Consequently, d is 2 nm. Hence, with the sum in Eq. (4.4) from $i =$ 1 to 100, C_{m} is estimated as 0.363 aF. It is assumed that each island has two neighboring islands, the total capacitance of one island C_1 is given in the form of $C_{\mathrm{self}} + 2C_{\mathrm{m}}$ which is calculated as 1.393 aF. Then, the charging engery of one island E_{C1} is given by

$$\begin{aligned} E_{C1} &= \frac{e^2}{2C_1} \\ &= 0.057 \quad eV. \end{aligned} \tag{4.5}$$

From the viewpoint of energies, the ratio $(E_C)_{\mathrm{exp}}/E_{C1}$ corresponding the effective number of islands on a branch, which is 37. Otherwise, from the viewpoint of geometry, if the branch is composed of only 3-nm Au NPs with 1-nm spacing, there should be at least 50 NPs in the 200-nm-wide gap between the drain and source electrodes. The minimum number of NPs (50) larger than the ratio $(E_C)_{\mathrm{exp}}/E_{C1}$ (37) indicates that not only 3-nm Au NPs, but also 15-nm Au NPs participate in bridging the 200-nm gap. In a circuit composed of parallel branches, the branch has the smallest charging energy should be the branch whose $(E_C)_{\mathrm{exp}}$ calculated from the $I_D - V_{DS}$ characteristics. The other branches should have larger charging energy.

A simple simulation model was built on the basis of the structure of the device II in Fig. 4.29 and its electrical characteristics. Firstly, the model consisted of three terminals because of the three-terminal structure of the device II. Secondly, the Au NP array was simplified to eight parallel branches

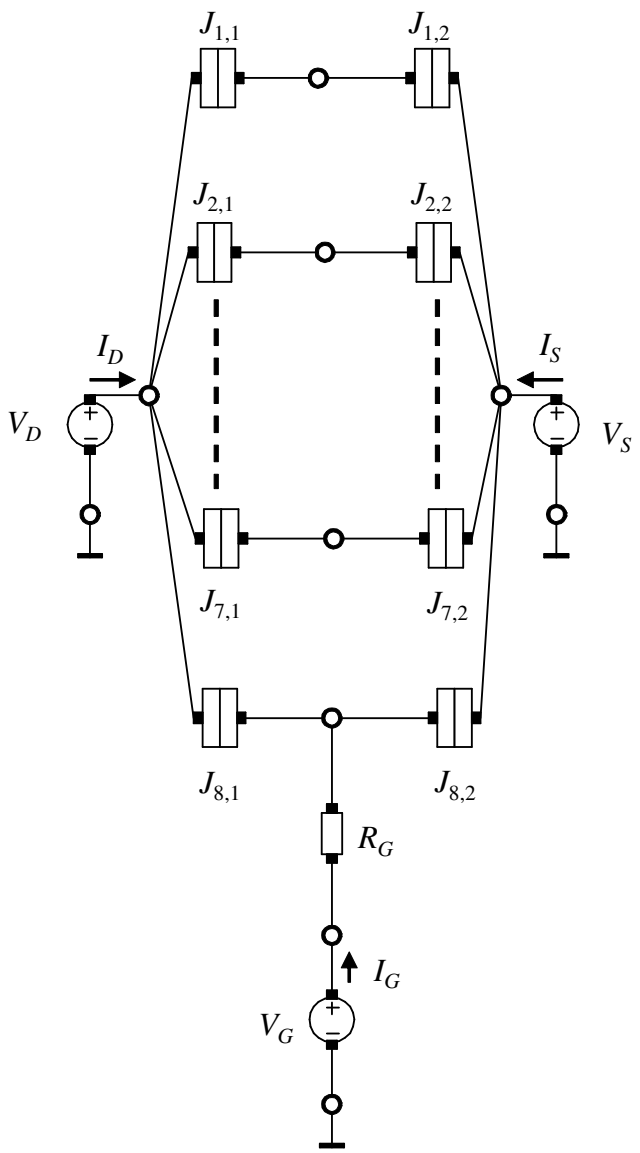


Figure 4.32: Schematic diagram of the simulation model.

of tunnel junctions. Finally, since the gate electrode was connected to a part of the NP array in Fig. 4.29, it was assumed to be resistively connected to one of the branches. Simulation was executed by using Monte-Carlo method [26] in the conditions of 77 K and no cotunneling.

Schematic diagram of the simulation model is described in Fig. 4.32. On each branch, there are two tunnel junctions in series. Positions of the junctions are like a matrix of elements $J_{i,j}$ with i = 1, 2, ..., 8 and j = 1, 2. Here, i is

Table 4.6: Paramters in the Simulation Model

Junctions	**Parameters**							
$J_{i,j}$	$J_{1,1}$	$J_{1,2}$	$J_{2,1}$	$J_{2,2}$	$J_{3,1}$	$J_{3,2}$	$J_{4,1}$	$J_{4,2}$
$C_{i,j}$ (aF)	0.020	0.018	0.018	0.016	0.016	0.014	0.014	0.012
$R_{i,j}$ (GΩ)	20.0	30.0	30.0	40.0	40.0	50.0	50.0	60.0

Junctions	**Parameters**							
$J_{i,j}$	$J_{5,1}$	$J_{5,2}$	$J_{6,1}$	$J_{6,2}$	$J_{7,1}$	$J_{7,2}$	$J_{8,1}$	$J_{8,2}$
$C_{i,j}$ (aF)	0.012	0.010	0.010	0.008	0.008	0.007	0.007	0.006
$R_{i,j}$ (GΩ)	60.0	70.0	5.0	7.0	7.0	8.0	8.0	9.0

Gate Resistor	**Parameter**
R_G (GΩ)	1.0

the position of the branch from top to bottom; j is the position of the junction from left to right on each branch. The junction $J_{i,j}$ has capacitance $C_{i,j}$ and resistance $R_{i,j}$. The gate resistor R_G connects the gate terminal and the eighth branch ($J_{8,1}, J_{8,2}$). The drain and source voltages have the same magnitude and opposite polarity. Directions of the drain, source, and gates currents are shown by arrows.

Since the model is built on the basis of the simple assumptions, values of parameters are only reprsentative selections in order for the numerical characteristics to fit to the experimental characteristics. The parameters listed in Table 4.6 are determined as follows. Firstly, in the parallel-branch model, the threshold voltage of the CB region $(V_{DS})_{\mathrm{th}}$ is determined by the branch having the lowest charging energy, so the largest total capacitance on one branch

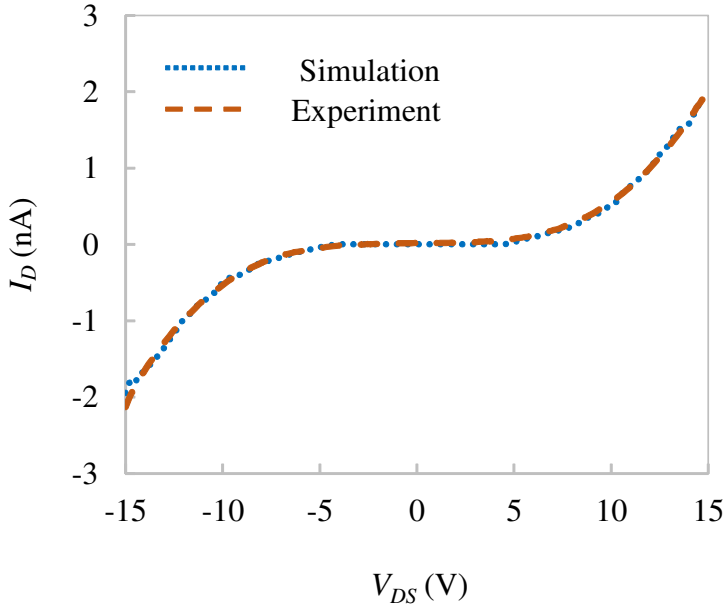


Figure 4.33: Simulated and measured drain currents I_D versus drain-source voltage V_{DS} at gate voltage V_G of 0 V and 77 K.

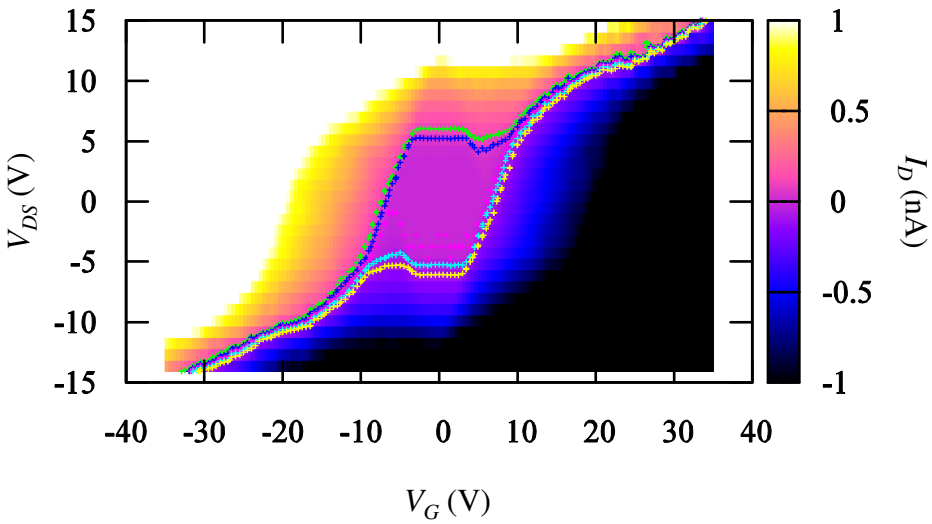


Figure 4.34: Simulated drain currents I_D are plotted as functions of gate voltage V_G and drain-source voltage V_{DS} at 77 K. I_D from -0.1 nA to $+0.1$ nA are illustrated by contour curves (from bottom to top) in 0.05 nA steps. Definition of contour colors are different from those in the color bar.

$(C_\Sigma)_{\max}$ is estimated as $(C_\Sigma)_{\max} = e/(V_{DS})_{\text{th}} \approx 0.038$ aF (the formular is driven from the symmetrically biased R-SET model). The first branch ($J_{1,1}$, $J_{1,2}$) is assumed to have $(C_\Sigma)_{\max}$. Secondly, tunnel resistances of the junctions are selected so that the simulated slope of I_D versus V_{DS} fits the measured slope in Fig. 4.30(a). Thirdly, effect of the gate voltage is considered as follows. The Coulomb diamond in the R-SET model disappears at $|V_G|_{\text{limit}} = e/(2C^*)$ [35]. On the other hand, in the experiment data in Fig. 4.31(a), the CB region mainly appears in the range of $|V_G|$ less than 6 V, that is, $|V_G|_{\text{limit}} = 6$ V. Hence, the total capacitance on the resistively-coupled branch C^* is 0.013 aF. This branch is assumed to be the eighth branch ($J_{8,1}, J_{8,2}$). Finally, the gate resistance R_G is adjusted to reproduce the slope of I_D on the $V_{DS} - V_G$ plane in Fig. 4.31(a).

Simulated and measured I_D versus V_{DS} are represented by dotted and dashed curves in Fig. 4.33. It is demonstrated that the simulation result is in good agreement with the experiment data. Figure 4.34 illustrates I_D on the $V_{DS} - V_G$ plane. The CB region (pink area) surrounded by light blue ($I_D = -0.05$ nA) and blue ($I_D = +0.05$ nA) contour curves mainly appears in the region of $|V_G| \leq 6$ V and $|V_{DS}| \leq 4$ V. This result reasonably agrees with that in Fig. 4.31(a). Strictly speaking, the simulation model is valid in limited conditions because the real device comprised a lot of Au NPs should have much more tunnel junctions and gate resistors. Nonetheless, this model can reproduce quite well the experiment results from the viewpoint of current-voltage characteristics.

4.4.3 Results and Discussion at Room Temperature

The device II was also measured at room temperature (287 K). The device was exposed in the air and measured by using the SPA. A measurement circuit is set as the same as in Fig. 4.28.

Current-voltage characteristics measured at 287 K are shown in Fig. 4.35. Drain currents I_D are plotted as functions of drain-source voltage V_{DS} at different gate voltages V_G of -35 V, 0 V, and $+35$ V. At $V_G = 0$ V, I_D is reprensented

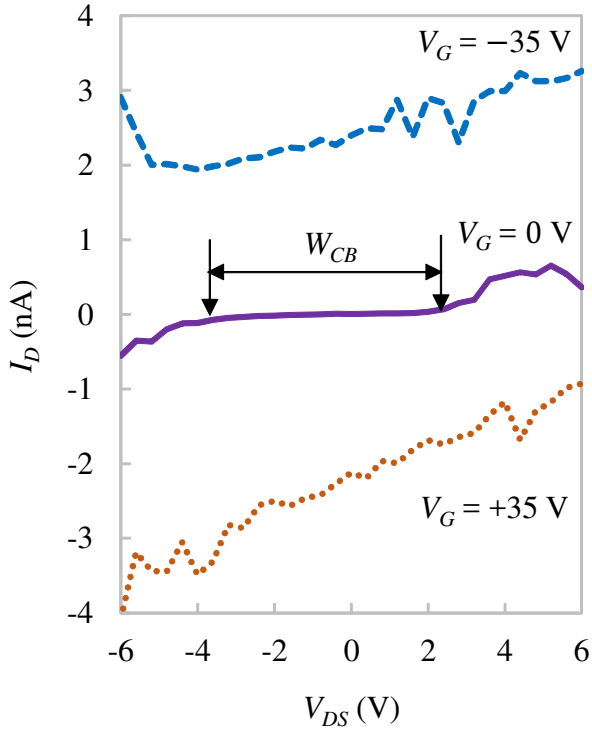


Figure 4.35: Measured drain currents I_D plotted as functions of drain-source voltage V_{DS} at room temperature (287 K) and different gate voltages V_G of −35 V, 0 V, and +35 V.

by a solid line. The CB region is defined as the region where $|I_D| < 0.1$ nA. Here, the threshold for the CB region at room temperature (0.1 nA) is assumed to be larger than that at 77 K (0.05 nA) because of larger effects of thermal fluctuations at room temperature. Then, the CB region is observed between V_{DS} of −3.6 V and +2.4 V, which is narrower than that at 77 K (between V_{DS} of −5.4 V and +4.2 V) due to thermal fluctuations [25]. A CB width W_{CB} is defined as the width of the CB region shown by arrows in Fig. 4.35. At V_G ± 35 V, the CB regions disappear, which indicates the effect of V_G on the CB state.

The effect of V_G on drain conductance, $G_D = dI_D/dV_{DS}$, is illustrated in Fig. 4.36. Blue area shows the small G_D which is less than 0.1 nS. By sweeping V_{DS} from −6 to +6V, the horizontal dimension of the blue area is modulated

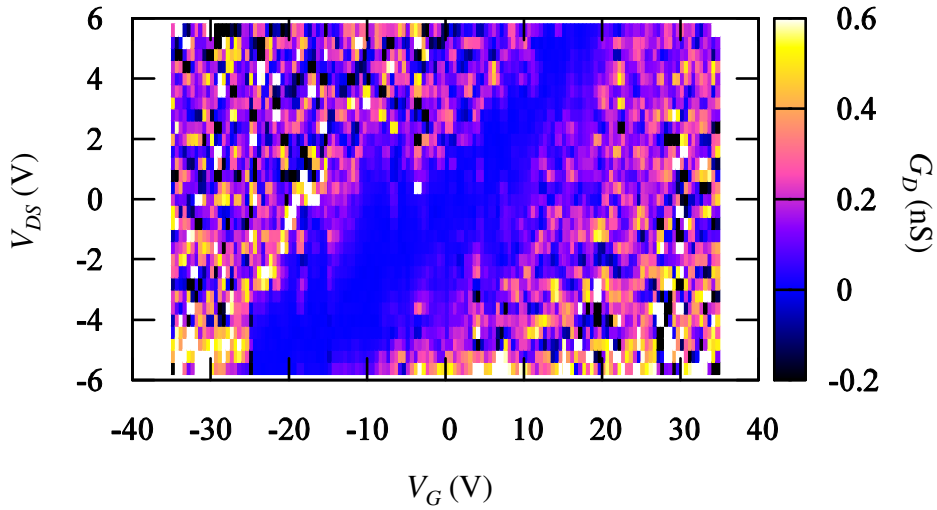


Figure 4.36: Drain conductances, $G_D = dI_D/dV_{DS}$, are plotted as functions of gate voltage V_G and drain-source voltage V_{DS} at room temperature (287 K).

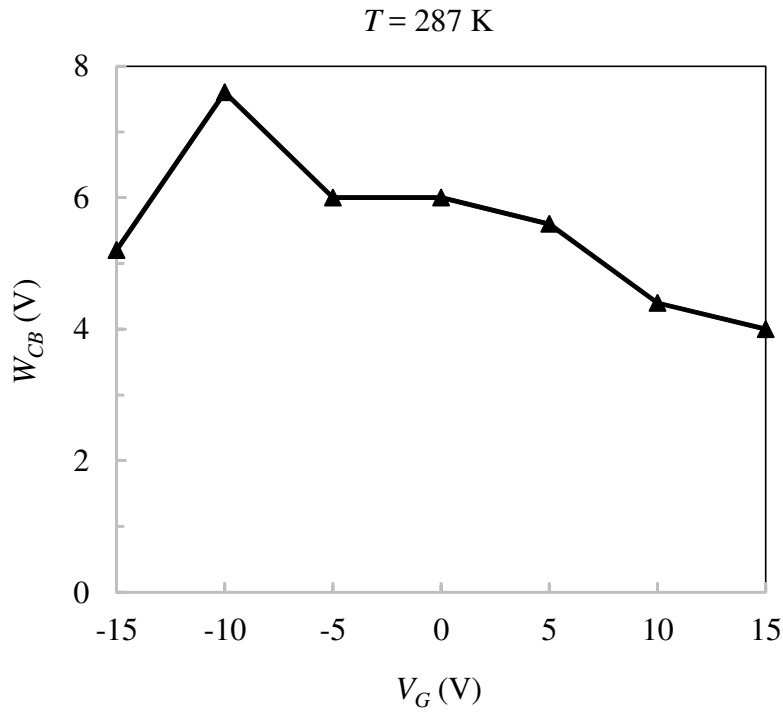


Figure 4.37: Coulomb blockade width W_{CB} is plotted as a function of gate voltage V_G at room temperature (287 K).

by changing V_G. This modulation can be seen more clearly in Fig. 4.37 where the width of CB gap, W_{CB}, is changed by applying V_G. Therefore, at room temperature, the CB region is observed at $V_G = 0$ and modulated by changing V_G.

4.5 Conclusion

In this chapter, the fabrication processes were described in details. The drain, source, and gate electrodes were formed on the SiO_2/Si chip by using standard EBL and evaporation techniques. The designed and fabricated geometries of the electrodes were confirmed in good agreement by analyzing an example of the fabricated chip. Arrays of tunnel junctions between the electrodes were formed by dropping the solutions of Au NPs. After measurements, types of the devices were determined by observing the CB phenomena. The fabrication processes and charactersitics of two typical devices including the device I and device II were introduced. The device I and the device II had the different gaps between the drain and source electrodes, different relative positions of the gate electrodes compared to the gaps, and the different amounts of Au NPs, resulting in different electrical characteristics. At 77 K, the device I was categorized into C-SET type whereas the device II was categorized into R-SET type. Moreover, for the device II, the CB was observed and modulated by applying the gate voltage at room temperature (287 K). Thus, our method is able to be useful for the future of the fabrication of SE devices.

Chapter 5

Conclusions

The thesis achieved two main goals including the improvement of the nonlinear characteristics of SE logic devices and the fabrication of SE devices having characteristics like SET.

The first objective was gained by using numerical method. SE logic devices such as SE four-junction inverter (SE FJI) and SE NAND gates have the disadvantage of the gradual switches between high and low output levels, resusting in unclear decision about output states in the transition region. To improve the gradual switching, input discretizer (ID) was added between the input terminal and the main device (SE logic device). Parameters of the ID was calculated on the basis of the condition of CB phenomena to obtain the sharp switching the designed threhold voltage. Monte-Carlo simulation was used to confirm the improvement of the characteristics of the SE logic device. The addition of the ID to the FJI (ID-FJI) made the switching of the ID-FJI sharp. The transition region of the ID-FJI was reduced to 0.011 times that of the solo FJI. The combination of the ID and the NAND gate (ID-NAND) made the switches of the ID-NAND sharp and its unclear regions were reduced to 0.33 times those of the solo NAND gate. Furthermore, two serially-cascaded IDs added between the input terminal and the SE FJI created the SE hysteretic inveter, 2ID-FJI. Parameters of the 2IDs were also calculated on the basis of the CB phenomena and confirmed by Monte-Carlo simulation to exhibit the hysteretic characteristics. The 2ID-FJI was used to

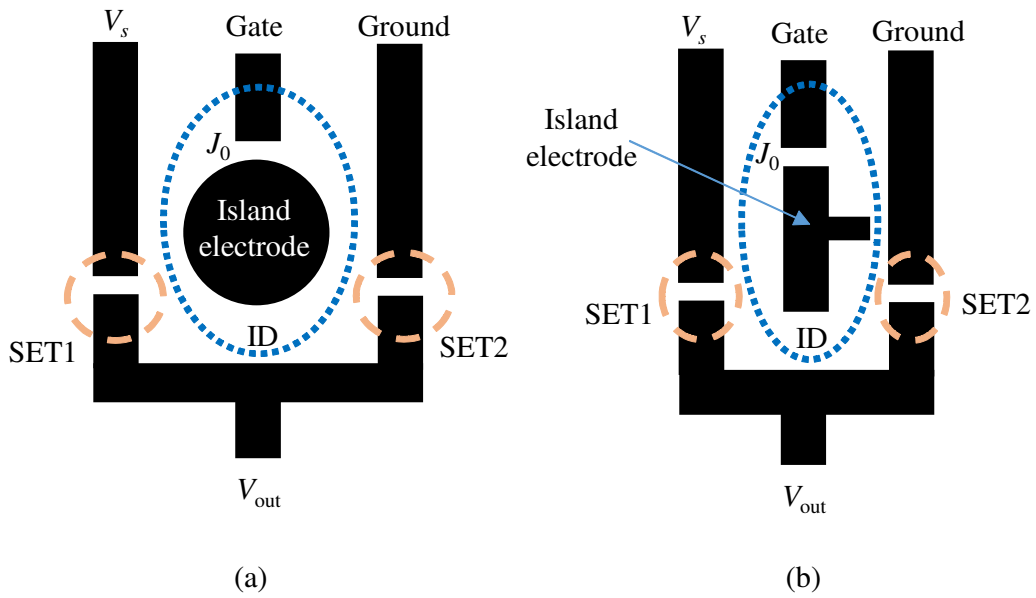


Figure 5.1: Simplified layout of a model composed of an input discretizer (ID) and an SE device. The SE device consists of SET1 and SET2. (a) Large island electrode. (b) Small island electrode.

improve stochastic resonance. The simulation results indicated that stochastic resonance in the 2ID-FJI was better than that in the solo FJI and equivalent to that in the ideal hysteretic inverter from the viewpoint of the correlation coefficient between the input and output signals.

The second objective was achieved from the experiment process. Fabrication of SE devices consisted of two main steps. In the first step, drain, source, and gate electrodes were fabricated by using standard EBL and evaporation techniques. In the second step, arrays of small tunnel junctions between the electrodes were formed by dropping solutions of Au NPs. To reduce the techinical difficulty during the fabrication, the gap size between the source and drain electrodes was designed to be at least 200 nm and the connections between Au NPs occured randomly. The fabricated devices were measured to confirm their characteristics. There were two typical configurations of the fabricated devices including device I and device II. In comparison with the previous works [14,32] which had narrow (sub-50-nm) gaps and operation temperature until 80 K, the

device I had the wider (1000 nm) gap and characteristics like C-SET at almost equivalent temperature (77 K). The deive II exhibited the characteristics like R-SET at 77 K. At room temperature, the CB gap was observed and modulated by applying the gate voltage to the device II. Hence, the deivce II used the different method and exhibited characteristics like R-SET at higher temperature than the previous litterature [34, 35] (sub-1-K). The method of fabrication might be useful for the realization of SE devices in the future.

Although the ID was designed for the improvement of the nonlinear characteristics of SE logic devices by numerical method, it is difficult to fabricate the total structure of the ID by using Au NPs. This can be explained as follows. The advantages of the ID mainly depend on the grounded capacitance whose value must be formed relatively exact. This grounded capacitance is difficult to form by using Au NPs because of the random distribution of Au NPs after dropping. Therefore, a combination of the ID and the main device might be done as shown in Fig. 5.1. The ID consists of the tunnel junction J_0 and the island electrode. The main device is composed of SET1 and SET2. Parameters in Fig. 5.1 include a voltage source V_s and an output voltage V_{out}. The electrodes can be fabricated by using EBL and shadow evaporation [85]. After that, solutions of Au NPs will be dropped to form the tunnel junctions of the ID and the main SE device. The size of the circuit includes the size of the ID and the size of the main device. In the simulation, the grounded capacitance C_{01} of the ID is much larger than the tunnel capacitance, then size of the C_{01} is main contributor. If we assume that the shape of the island electrode is a sphere far from the ground (Fig. 5.1(a)), for the SiO_2 substrate and C_{01} = 72 aF, the diameter of the sphere is evaluated approximately 0.52 μm. In addition, if we fabricate the 100-nm-wide electrodes, the area of the circuit (the ID and the main device) can be 1.0 μm $\times$ 1.0 μm. The size of the circuit can be reduced by designing the model as shown in Fig. 5.1(b). In Fig. 5.1(b), the size of the island electrode is reduced by making the island electrode close to the ground.

The achivements of the thesis are prospective for future applications. Firstly,

the correct operation of the SE logic devices requires that the output levels lie in the certain ranges defined as the high and low levels. The output of the SE logic device (the FJI and NAND gates) is continuous in the transition region, causing the error decisions about the output states in this region. This error can be reduced if the logic circuits are composed of the ID-FJI and/or the ID-NAND because they have the narrower transition regions (the sharp switches). Furthermore, the possibility of connecting the ID-FJIs in series and in parallel allows us to implement various logic circuits, for example the interver string and the flip-flop, and increase the number of fan-ins and fan-outs in the circuit. Secondly, in the thesis, the SE hysteretic inverter which enhanced stochastic resonance to be equivalent to the ideal hysteretic inverter can be used to improve the detectability of the weak signals in sensory systems. Finally, in the thesis, the device exhibiting characteristics like R-SET was fabricated. The R-SET device is a potential candidate for eliminating the random background charge which is one of the serious obstacles in digital applications. Moreover, the observation of CB phenomenon at room temperature are prospective for practical applications.

Appendix A

Negative Differential Resistance Characteristics

A.0.1 Fabrication Method

In our experiment, we also observed another interesting characteristcs: negative differential resistance (NDR). Below, we introduced device III as an example of the device exhibiting the NDR phenomena.

Fabrication processes of the device III included three steps as follows. Firstly, on the SiO_2/Si chip, drain, source, and gate electrodes were formed by using a single copolymer (PMMA and PMAA 11 %) resist, standard EBL, thermal evaporation of 30-nm-thick Au, and lift off process. Secondly, 0.1 μL of a toluene solution containing 0.1 wt% of 3-nm Au NPs coated by decanethiol was dropped on the chip. Finally, 0.1 μL of a citric acid solution containing 0.007 wt% of 5-nm Au NPs was also dropped on the chip. Here, 3-nm Au NPs were expected to work as islands whose charging energies should be large enough for room temperature operation. In addition, 5-nm Au NPs were used to make conductive bridges, which contributed to reduce resistance between the drain and source electrodes.

The device III was measured by using SPA. The measurement circuit established is the same as Fig. 4.28. Voltages applied to the drain and source were the same in magnitude and opposite in polarity. The device was exposed

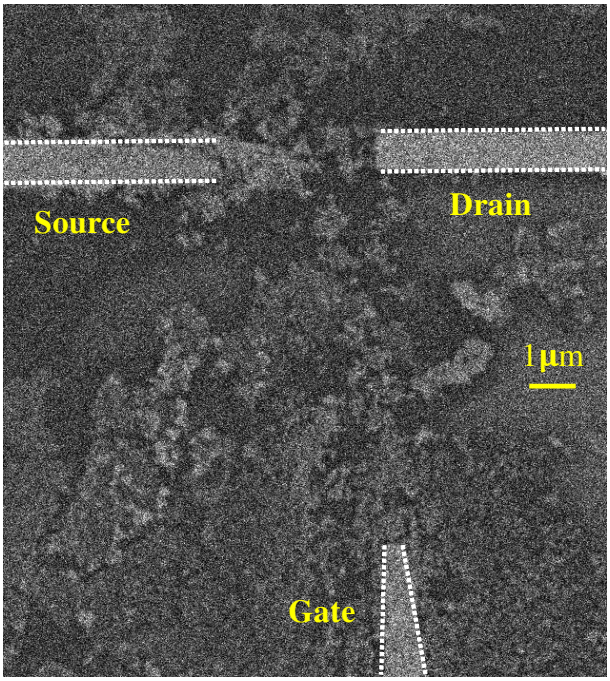


Figure A.1: Scanning electron microscopy (SEM) image of the device III (chip 160419A No. 4) after measurement.

to the air to measure its characteristics at room temperature (298 K).

Figure A.1 shows a SEM image of the device III after measurements. For clarity, edges of the drain, source, and gate electrodes are shown by white dashed lines. Between the drain and source electrodes, there is a 3.1-μm-wide gap. The gate electrode is 7.3 μm far from the drain electrode. An array of Au NPs was constituted between the electrodes.

A.0.2 Results and Discussion

Currents of the device III measured at room temperature (298 K) are shown in Fig. A.2. Drain current I_D, source current I_S, and gate current I_G at gate voltage $V_G = 0.5$ V are respectively represented by dotted, dashed, and solid curves in Fig. A.2(a). I_D and I_S have the same magnitude but opposite polarity. I_G is less than 0.6 nA. It can be seen that a clear NDR phenonmenon is observed in the region of V_{DS} from 1.9 V to 2.5 V, which is shown by the

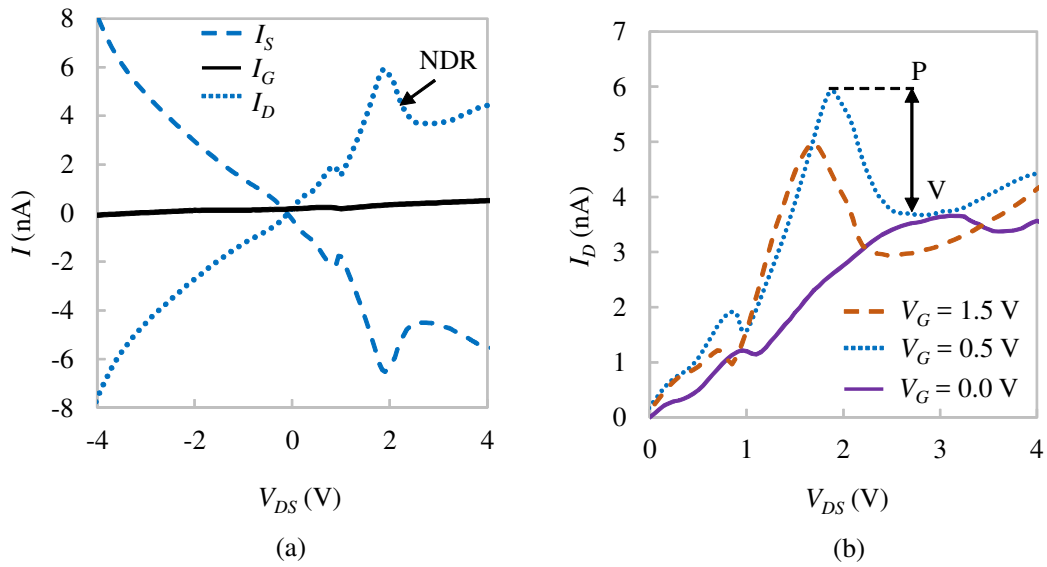


Figure A.2: Measured currents versus drain-source voltage V_{DS} of the device III at room temperature (298 K). Currents are shifted by using the current offsets at $V_G = V_{DS} = 0.0$ V. (a) Drain current I_D, source current I_S, and gate current I_G at $V_G = 0.5$ V. Negative differential resistance (NDR) is shown by an arrow. (b) I_D at different V_G of 0.0 V, 0.5 V, and 1.5 V. P and V stand for peak and valley points of NDR, respectively.

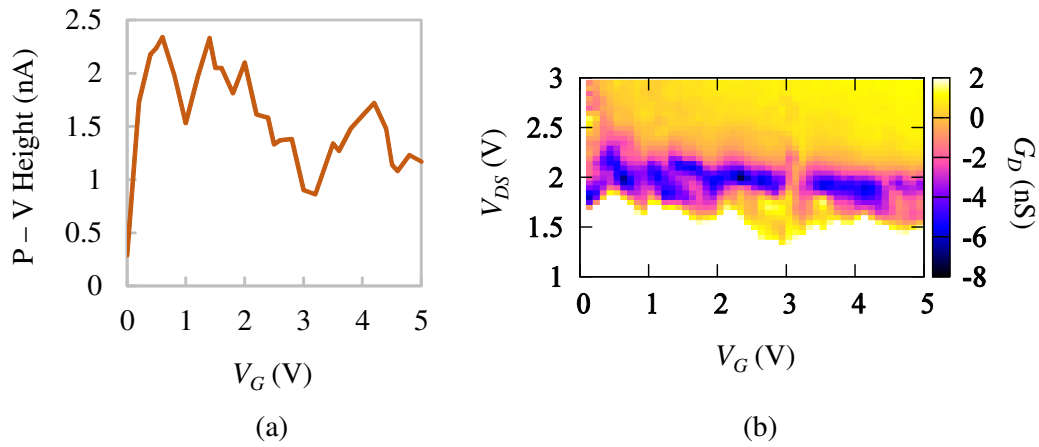


Figure A.3: Characteristics of the device III are observed at 298 K. (a) P-V height is plotted as a function of gate voltage V_G. (b) Drain conductances, $G_D = dI_D/dV_{DS}$, are plotted as functions of V_G and drain-source voltage V_{DS}.

arrow.

Effects of V_G on the NDR behavior are described in Fig. A.2(b). All the absolute I_G are confirmed to be under 0.8 nA. I_D at different V_G of 0.0 V, 0.5 V, and 1.5 V are illustrated by solid, dotted, and dashed curves, respectively. All of three curves exhibit NDR phenomena, in which the most remarkable NDR appears in the region of 1 V $< V_{DS} <$ 3 V. We use a "P-V height", which is the height of the peak (P) from the valley (V) indicated by the double arrow in Fig. A.2(b), for characteristics of the NDR. The P-V height increases when V_G increases from 0.0 V to 0.5 V. It is reduced when V_G rises further from 0.5 V to 1.5 V.

The relationship between the P-V height and V_G are demonstrated in more details in Fig. A.3(a), where the oscillation of the P-V height is observed. The P-V height reaches a maximum (2.3 nA) at $V_G = 0.6$ V, whereas it reaches a minimum (0.29 nA) at $V_G = 0.0$ V. Figure A.3(b) shows the drain conductance G_D plotted on the $V_{DS} - V_G$ plane, where G_D is defined as dI_D/dV_{DS}. A white area describes the region without NDR ($G_D > 0$). Blue areas correspond to the noticeable NDR regions where $G_D < -4$ nS. Since the NDR phenonmena could be controlled by applying V_G, NDR is tunalbe.

Although it is difficult to observe the individual Au NP in Fig. A.1, it can be observed that the Au NP array contains multi-directional paths with different densities. The Au NP array suggests that there are many branches of tunnel junctions whose parameters are different. These properties could be a reason to generate the NDR phenomena in SE devices [86].

Appendix B

List of publications

Journal papers

1. Tran T. T. Huong and Y. Mizugaki, "A single-electron hysteretic inverter designed for enhancement of stochastic resonance," IEICE Electronics Express (ELEX), vol.12, no.17, pp.20150527-1-12, September, 2015.

2. Tran T. T. Huong, H. Shimada, and Y. Mizugaki, "Improvement of Single-Electron Digital Logic Gates by Utilizing Input Discretizers," IEICE Transactions on Electronics, vol.E99-C, No.2, pp.285-292, Febuary, 2016.

International conferences

1. Tran T. T. Huong and Y. Mizugaki, "Design of single-electron hysteretic inverter," International Symposium on Nanoscale Transport and Technology (ISNTT2015), Atsugi, Kanagawa, Japan, November 17-20, 2015.

2. Huong T. T. Tran, K. Matsumoto, M. Moriya, H. Shimada, Y. Kimura, A. Hirano-Iwata, and Y. Mizugaki, "Fabrication of high temperature

capacitively- and resistively-coupled single electron transistors using gold nanoparticles," 16th International Conference on Nanotechnology (IEEE NANO 2016), Sendai International Center, Sendai, Japan, August 22-25, 2016. Proceedings of the 16th International Conference on Nanotechnology, pp. 131-134.

Domestic conferences

1. H. Tran, H. Shimada, and Y. Mizugaki, Numerical Demonstration of Single-Electron Inverter with Input Discretizer, JSAP 75th Autumn Meeting, 19a-A7-5, 2014.

2. H. Tran, H. Shimada, and Y. Mizugaki, Stochastic Resonance in Single-Electron Inverter Improved by Attachment of Input Discretizer, JSAP 62nd Spring Meeting, 14a-A20-5, 2015.

Award

1. UEC President's Award for Excellent Research Achievement, March 25th, 2016.

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