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Power Gain Mechanism and Methods for Power Gain Improvement of Quantum and Conventional Transistors

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和文要旨

本論文では、量子効果トランジスタを始めとし全ての電子デバイスで重要となる電力利得に関して詳細に検討し、その改善方法を提案している。先ず、初めての試みとして、量子効果トランジスタの中での代表格である単電子トランジスタ（ＳＥＴ）を信号源有能電力とインピーダンス整合負荷電力の比から定義される電力利得の視点でモデリングし、構造パラメータとの関連を明らかにしている。さらに、電力利得と並んでＳＥＴの動作速度に大きな影響を与える電力利得の周波数特性についても解析している。この結果、ＳＥＴの電力利得は、ＳＥＴのソース接合厚を 1.25nm 薄くするなどデバイス構造を最適化すると 40dB 程度改善されることを示している。また周波数特性はＴＨｚ領域まで伸びていることを解析的に示している。これらからＳＥＴが高速デバイスとしての可能性を有していることが示されている。さらに、電力利得向上の知見を従来型デバイスである InGaP/GaAs ヘテロ接合バイポーラトランジスタ（ＨＢＴ）ならびに AlGaN/GaN 高電子移動度トランジスタ（ＨＥＭＴ）にも適用し、これらの電力利得を複数トランジスタの回路的結合の視点で改善する方法を検討している。特に電力利得とひずみ特性などの大信号特性との両立に対して優れていると考えられる３トランジスタのスタック構造から構成される独立バイアス型 3 段カスコード回路と従来型３段カスコード回路との利害得失をＨＢＴとＨＥＭＴに関して検討している。独立バイアス型ＨＢＴカスコード回路では 1.9 GHz において 5 dB 以上の電力利得改善が従来型に対して実験的に改善されている。これらの検討により試作されたＨＢＴ増幅器では電力利得 32.6 dBc, 出力 12 dBm 時に付加電力効率 23.5 %，3 次相互変調ひずみ比-35dBc が得られ、GaN HEMT 増幅器では電力利得 24.0 dB，出力 28.8dBm 時に付加電力効率 46.5 %，3 次相互変調ひずみ比-32.3 dBc が得られている。

この構成により各段バイアス設定により、これまでトレードオフと考えられていたマイクロ波回路動作の重要な指標である電力利得，電力効率，ひずみ特性を独立に制御できることを示している。

Abstract

This thesis aims to study power gain, methods for its improvement and various power gain related microwave performances including stability, isolation, efficiency and linearity for various devices and independently biased circuit configurations. For the purpose of studying power gain, one of the most important characteristics of active devices, a quantum device named the single-electron transistor (SET), and an independently biased heterojunction bipolar transistor (HBT) cascode configuration were chosen to investigate using the methods of current transfer control and resistance transfer control, respectively. By using the current transfer control method for power gain improvement, power gain and output power of the SET were found to be significantly improved by 39.45 dB and 39.45 dBm, respectively if its source resistance was reduced by 99.3 MΩ which is equivalent to the reduction by 1.25 nm of the source junction thickness. In addition to the power gain, frequency characteristic which relates to the operation speed of the SET was also investigated. The frequency characteristic of the proposed SET model reveals the fact that it can operate well at THz regime, thus it can be regarded as an ultra-high speed device for possible high data rate wireless communication application in the future. Besides SET, power gain enhancement for a novel circuit construction which is so-called the independently biased cascode InGaP/GaAs HBT was also studied by taking the advantage of resistance transfer control method of the cascode configuration. Its power gain can be enhanced thanks to the use of the independently biased feature to control its output resistance through adjusting the second stage collector bias current. Its power gain was experimentally confirmed to be higher than that of a conventional configuration by more than 5 dB at an operation frequency of 1.9 GHz. For the purpose of studying power gain related microwave performances, two independently biased configurations, namely 3-stack InGaP/GaAs heterojunction bipolar transistor (HBT) and 3-stack AlGaN/GaN high mobility electron transistor (HEMT) were chosen to

investigate. In this research topic, not only power gain but various important microwave performances of the two configurations were studied under the investigation of various bias conditions by taking the advantage of the two added bias terminals. It was concluded that the fabricated amplifier which was based on the independently biased InGaP/GaAs HBT 3-stack monolithic microwave integrated circuit (MMIC) chip can deliver an optimum performance at an operation frequency of 1.6 GHz for superior power gain and low distortion as: PAE = 23.5 %, P_{out} = 12 dBm; Gain = 32.6 dB at IMD3 = -35 dBc. In addition, the small-signal and large-signal performances of the proposed configuration also exhibited better than that of a conventional configuration if its bias condition is controlled appropriately. For the independently biased AlGaN/GaN HEMT 3-stack configuration, by setting appropriate bias condition for each transistor using independently biased feature, the simulated results at an operation frequency of 2.1 GHz demonstrated a high output power, high efficiency and high gain performance as: PAE = 46.45 %, P_{out} = 28.82 dBm; Gain = 23.96 dB at IMD3 = -32.34 dBc. These results has confirmed the superior advantages of the proposed configurations.

Contents

Abstract v

List of Figures x

List of Tables xx

1 Introduction 1

1.1 Introduction to power gain and its related applications . . . 1

1.1.1 The need for power in conventional applications . . . 2

1.1.2 The need for power in quantum applications . . . 4

1.2 Power gain mechanism . . . 5

1.3 Power gain definitions for two-port networks . . . 7

1.3.1 Power gain definitions . . . 7

1.3.2 Figures of merits of device related to power gain definitions . . . 10

1.4 Practical applications related to figure of merits of the device . . . 12

1.5 Methods for power gain improvement . . . 13

1.5.1 Power gain improvement for BJT/HBT . . . 13

1.5.2 Power gain improvement for FET and high electron mobility transistor (HEMT) . . . 20

1.6 Brief introduction to two important quantum devices . . . 24

1.7 Outline of the thesis . . . 29

2 Method for power gain enhancement of single-electron transistor (SET) 30

2.1 Introduction . . . 30

2.2 Operation of single-electron transistor (SET) . . . 33

2.2.1 Background of SET 33
2.2.2 Important parameters of the SET 36
2.2.3 Conductance and transconductance characteristics of SET according to MIB model 39
2.3 Method for power gain enhancement of single-electron transistor (SET) . . 48
2.3.1 Small-signal equivalent circuit 49
2.3.2 Power gain improvement for SET 51
2.3.3 Frequency response of the SET 52
2.3.4 Influence of the source junction thickness on power gain improvement . 55
2.4 Summary 58

3 Power gain performance enhancement of independently biased InGaP/GaAs heterojunction bipolar transistor (HBT) cascode chip 60

3.1 Introduction 60
3.2 DC power analysis 62
3.3 Power gain investigation 65
3.4 Bias conditions investigation 71
3.4.1 First bias case 71
3.4.2 Second bias case 73
3.5 Experimental setup 74
3.6 Measured results 75
3.6.1 First bias case results 76
3.6.1.1 DC power supply 76
3.6.1.2 Small-signal power gain 78
3.6.2 Second bias case results 78
3.6.2.1 DC power supply 78
3.6.2.2 Small-signal power gain 82
3.7 Summary 82

4 Microwave performances investigation of independently biased 3-stack InGaP/GaAs HBT and GaN HEMT configurations 84

4.1 Introduction 84

4.2 Microwave performance investigation of independently biased 3-stack InGaP/GaAs HBT configuration . . . 85
4.2.1 Small-signal analysis . . . 85
4.2.1.1 Investigation of the first transistor's base bias current (I_{b1}) . . . 88
4.2.1.2 Investigation of the second transistor's base bias current (I_{b2}) . . 88
4.2.1.3 Investigation of the third transistor's base bias current (I_{b3}) . . 89
4.2.1.4 Investigation of the first mid-point bias voltage (V_{cc1}) 90
4.2.1.5 Investigation of the second mid-point bias voltage (V_{cc2}) 91
4.2.1.6 Investigation of the third collector bias voltage (V_{cc3}) 92
4.2.1.7 Comparison of performances between the independently biased 3-tack HBT structure and the conventional, independently biased HBT cascode structures . . . 95
4.2.1.8 Performance comparison between the independently biased 3-tack HBT structure and the conventional 3-stack HBT structure . 98
4.2.2 Large-signal analysis . . . 99
4.2.2.1 Simulation investigation . . . 100
4.2.2.2 Measured results . . . 108
4.2.3 Conclusion . . . 113
4.3 Microwave performance investigation of independently biased 3-stack GaN HEMT configuration . . . 114
4.3.1 Introduction . . . 114
4.3.2 Investigation of large-signal characteristics . . . 114
4.3.2.1 Effect of the gate bias voltage . . . 115
4.3.2.2 Effect of the drain bias voltage . . . 119
4.3.3 Conclusion . . . 122
4.4 Summary . . . 123

5 Conclusions and future work **125**

Acknowledgements **128**

Bibliography **130**

List of Figures

1.1 The importance of power in conventional applications: a) RADAR systems; b) mobile communication network; c) satellite communications; d) microwave area. 3

1.2 Illustration of sole voltage and current amplifier: a) voltage amplifier; b) current amplifier. In either case, there is not enough output power ($V_{\mathrm{out}} I_{\mathrm{out}}$) to follow the variation of the load R_{L}. 3

1.3 Illustration of the basic power gain mechanism for a gain element. 6

1.4 Types of power gain definitions for the gain element worked as a two-port network. Here: a) transducer gain; b) available gain; c) operating gain; d) maximum available gain (MAG). 8

1.5 Typical curves for short-circuit current gain and power gains of a common-emitter (CE) 2 μm x 20 μm x 2 InGaP/GaAs heterojunction bipolar transistor (HBT) (WIN Semiconductor Corp. model) under bias condition: $V_{\mathrm{ce}} = 4.0$ V, $I_{\mathrm{b}} = 0.12$ mA. It is noted here that $|S_{21}|^2$ curve can reach to MAG curve at the point of matched condition. Here $f_{\mathrm{c}} = 9.2$ GHz, $f_{\mathrm{T}} = 29.7$ GHz, $f_{\max} = 36.4$ GHz. 9

1.6 Typical step response of a transistor and its related possible applications: a) the output signal having slow response time and slow rise time; b) the output signal having fast response time and slow rise time; c) the output signal having slow response time and fast rise time; d) the output signal having fast response time and fast rise time. Here fast response time and fast rise time means high f_{T} and high $f_{\max}$ respectively and vice verse. . . . 11

1.7 Simplified small-signal equivalent circuit for BJT where both the input and output sides are simultaneous conjugate matched. 14

1.8 Typical energy band diagram of an HBT: a) before energy band formation and b) after energy band formation. 16
1.9 Simplified small-signal equivalent circuit with both input and output conjugate matched of the BJT cascode configuration. 18
1.10 Simplified small-signal equivalent circuit for FET where both the input and output sides are simultaneous conjugate matched. 21
1.11 Typical energy band diagram of an AlGaN/GaN HEMT. 22
1.12 Simplified small-signal equivalent circuit with both input and output conjugate matched of the FET cascode configuration. 23
1.13 Illustration of the SET structure. 25
1.14 Illustration of operation of SET. 26
1.15 Typical energy band structure of a resonant tunneling device. 26
1.16 Typical IV characteristic of an RTD which exhibits the negative differential resistance (NDR). 27
1.17 Small-signal equivalent circuit of RTT. Here R_{S} is series resistance, R_{d}, L_{d} and C_{d} are internal resistance, inductance and capacitance, respectively. . 28

2.1 The evolution of transistor from the beginning to the appearance of emerging devices. 31
2.2 The equivalent basic diagram of SET. 34
2.3 The SPICE macro model proposed by Yu. Here $R_{\mathrm{G}} = 100\,\mathrm{G\Omega}$; $R_1(V_{\mathrm{GS}}) = CR_1 + CR_2 cos(\pi CF_1 V_{\mathrm{GS}})$; $R_2 = R_3 = CV_{\mathrm{p}}/(CI_2 - 2CV_{\mathrm{p}}/R_1(V_{\mathrm{GS}}))$. . . . 35
2.4 The typical $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic of SET plotted by using Eq. (2.9). The parameters' values are $R_{\mathrm{TD}} = 1\,\mathrm{M\Omega}$, $R_{\mathrm{TS}} = 19\,\mathrm{M\Omega}$, $C_{\mathrm{G}} = 1\,\mathrm{aF}$, $C_{\mathrm{TS}} = 1.9\,\mathrm{aF}$, $C_{\mathrm{TD}} = 0.1\,\mathrm{aF}$, $T = 18.6\,\mathrm{K}$. 37
2.5 The typical $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ characteristic of SET plotted by using Eq. (2.9). The parameters' values are the same as $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic. 37
2.6 Drain conductance characteristic of the SET. The Coulomb blockade effect still exists and repeats periodically. The SET's parameters still remain same as when calculating $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic. 39
2.7 Transconductance characteristic of the SET. The Coulomb blockade effect still exists and repeats periodically. 40

2.8 Transconductance characteristic of the SET. The Coulomb blockade effect still exists and repeats periodically. 40

2.9 Transconductance characteristic of the SET. The Coulomb blockade effect still exists and repeats periodically. 41

2.10 Dependence of g_{d} on tunnel resistances (R_{TD} and R_{TS}). It can be seen that g_{d} increases with the decreasing R_{TD} and R_{TS}. Here $V_{\mathrm{GS}} = 0.02\,\mathrm{V}$. . . 46

2.11 Dependence of g_{d} on tunnel capacitances (C_{TD} and C_{TS}) and the gate capacitance (C_{G}). Although g_{d} increases with the decreasing C_{TD}, the effect of C_{TS} and C_{G} on g_{d} is not so clear. Here $V_{\mathrm{GS}} = 0.02\,V$. 46

2.12 Dependence of g_{m} on tunnel resistances (R_{TD} and R_{TS}). It can be seen that g_{m} increases with the decreasing R_{TD} and R_{TS} as the same g_{d}. Here $V_{\mathrm{DS}} = 0.02\,V$ 47

2.13 Dependence of g_{m} on tunnel capacitances (C_{TD} and C_{TS}) and the gate capacitance (C_{G}). The effect of C_{G}, C_{TS} and C_{G} on g_{m} is also not so clear. Here $V_{\mathrm{GS}} = 0.02\,V$. 47

2.14 The construction of equivalent circuit for MOSFET devices based on their active region of the $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic. Here: a) MOSFET device, b) The $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic, and c) The simplified equivalent circuit. . 48

2.15 New $I_{\mathrm{D}} - V_{\mathrm{DS}}$ characteristic of the SET. The calculated characteristic by Inokawa model coincides well with SIMON simulator. The SET parameters values are $R_{\mathrm{TD}} = 0.1$ MΩ, $R_{\mathrm{TS}} = 10$ MΩ, $C_{\mathrm{G}} = 0.5$ aF, $C_{\mathrm{TD}} = 10^{-3}$ aF, $C_{\mathrm{TS}} = 2 \times 10^{-4}$ aF. 49

2.16 Small-signal equivalent circuit of the SET for power gain investigation as a MOSFET-like common-source configuration. V_{S} and Z_{S} denote the source voltage and impedance respectively while Z_{L} represents the load impedance. Here the gate resistance of the SET is not considered. 50

2.17 a) and b): Frequency characteristic with respect to the variation of the source and drain resistances (R_{TS} and R_{TD}); c), d), and e): frequency characteristic with respect to the variation of the drain, source and gate capacitances (C_{TD}, C_{TS}, and C_{G}) respectively. The SET parameters: a) $R_{\mathrm{TD}} = 0.1\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$, $C_{\mathrm{G}} = 0.5\,\mathrm{aF}$; b) $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$, $C_{\mathrm{G}} = 0.5\,\mathrm{aF}$; c) $R_{\mathrm{TD}} = 0.1\,\mathrm{M\Omega}$, $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$, $C_{\mathrm{G}} = 0.5\,\mathrm{aF}$; d) $R_{\mathrm{TD}} = 0.1\,M\Omega$, $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_G = 0.5\,\mathrm{aF}$; e) $R_{\mathrm{TD}} = 0.1\,\mathrm{M\Omega}$, $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$. 54

2.18 Source junction thickness of the SET: a) Draw of the structure and b) The equivalent circuit of the junction. 55

2.19 The dependence of SET output power and power gain on the source resistance. The SET parameters: $R_{\mathrm{TD}} = 0.1\ \mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\ \mathrm{aF}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\ \mathrm{aF}$, $C_{\mathrm{G}} = 0.5\ \mathrm{aF}$. 56

2.20 The dependence of SET power gain on the source junction thickness. . . . 56

3.1 Simplified hybrid π model small-signal equivalent circuit of the cascode configuration. 61

3.2 a) Conventional cascode configuration (Conventional CC) and b) Independently biased cascode configuration (Independently Biased CC). Here I_{b1c} and I_{b2c} represent the base bias currents of the CE and CB of the Conventional CC; I_{b1n} and I_{b2n} denote the base bias currents of the CE and CB of the Independently Biased CC, respectively. Furthermore, V_{c1c} and V_{c2c} are the collector bias voltages of the CE and CB transistors of the Conventional CC, respectively; V_{c1n} and V_{c2n} are the collector bias voltages of the CE and CB transistors of the Independently Biased CC, respectively. I_{c1c}, I_{c2c} and I_{c1n}, I_{c2n} represent the DC collector currents for the CE and CB transistors of the Conventional CC and Independently Biased CC respectively whereas V_{c1c}, V_{c2c} and V_{c1n}, V_{c2n} represent their DC collector voltages. 63

3.3 Simplified small-signal equivalent circuit for the Conventional CC and Independently Biased CC as a two-port network of a cascode connection of CE and CB transistors. Here g_{m}, g_0, and g_π represent the conductances at a specific bias point; C_μ and C_π denote the base-collector and base-emitter capacitances, respectively; i_{b1} and i_{c2} are the AC currents of the CE and CB transistors, respectively whereas v_1 and v_2 represent the AC base-emitter voltages of the CE and CB transistors, and v_3 is the AC CB transistor collector voltage. 65

3.4 Conventional CC and Independently Biased CC as a two-port network which is formed by the combination in cascade of two two-port networks, the CE and CB transistors. S-parameters of the Conventional CC and Independently Biased CC are derived by converting their F-parameters. . . 66

3.5 The dependence of MAG difference between the Conventional CC and Independently Biased CC employing the graphical method. The relationship between the difference in MAG or $\mathrm{MAG}_n - \mathrm{MAG}_c$ and difference in I_{c2} or $I_{\mathrm{c2n}} - I_{\mathrm{c2c}}$) is expressed through the angles α_1, α_2, α_3, and α_4. Here, I_{c2} denotes both I_{c2n} and I_{c2c}. 69

3.6 A typical load-line of the Conventional CC. Tr2 or the CB transistor is treated as a load terminal of the Tr1 or the CE transistor. Q_{1c} and Q_{2c} represent two possible or stable bias points which is contrary to the unstable bias region lying between these two points. It is noted that the total collector voltage V_{cc} remains the same at both Q_{1c} and Q_{2c} or $V_{\mathrm{cc}} = V_{\mathrm{c1c}} + V_{\mathrm{c2c}}$. Moreover, in the case of the Conventional CC, $I_{\mathrm{c1c}} = I_{\mathrm{c2c}}$. 72

3.7 A typical load-line of the Independently Biased CC. Here $\mathrm{Q}_{1n} - \mathrm{Q}_{4n}$ are sample possible bias points of the Independently Biased CC. In the Independently Biased CC V_{cc} are the same with that of the Conventional CC or $V_{\mathrm{cc}} = V_{\mathrm{c1c}} + V_{\mathrm{c2c}} = V_{\mathrm{c1n}} + V_{\mathrm{c2n}}$. 72

3.8 Illustration of the first bias case in which it can be seen that for the Conventional CC, at its two bias points, one of the two transistors has to be biased in the saturation region. On the other hand, in the case of the Independently Biased CC, its two transistors can be biased in the active region. With this bias condition, Independently Biased CC shows higher I_{c2} compared to that of the Conventional CC. 73

3.9 Illustration of the second bias case. In this case, bias condition of the Independently Biased CC is set the same as that of the Conventional CC, this makes the I_{c2n} to fall between I_{c2cmin} and I_{c2cmax} 74

3.10 Experimental setup for DC power supply and power gain investigation between the Independently Biased CC and Conventional CC. 75

3.11 Results for the investigation of the relationship between I_{c2} and DC power supply P_{DC} of the Independently Biased CC and Conventional CC for the first bias case. Here, *New* means the Independently Biased CC and *Conv* is the Conventional CC whereas *Sim* is simulation and *Exp* is experiment. 77

3.12 The dependence of the difference in DC power supply or $P_{DCn} - P_{DCc}$ on the difference in I_{c2} or $I_{c2n} - I_{c2c}$ for the first bias case. 77

3.13 Results for the investigation of the relationship between I_{c2} and small-signal power gain (MSG) of the Independently Biased CC and Conventional CC for the first bias case. 79

3.14 Results for the investigation of the dependence of the difference in power gain or $\mathrm{MSG_n} - \mathrm{MSG_c}$ on the difference in I_{c2} or $I_{c2n} - I_{c2c}$ for the first bias case. 79

3.15 Results for the investigation of the relationship between I_{c2} and DC power supply P_{DC} of the Independently Biased CC and Conventional CC for the second bias case. Here I_{c2} represent both I_{c2n} and I_{c2c}. 80

3.16 The dependence of the difference in DC power supply or $P_{DCn} - P_{DCc}$ on the difference in I_{c2} or $I_{c2n} - I_{c2c}$ for the second bias case. Both the difference in I_{c2} and difference in P_{DC} curves cross the zero-line, or the balanced point of DC power and power between the Independently Biased CC and Conventional CC. 80

3.17 Results for the investigation of the relationship between I_{c2} and small-signal power gain (MAG) of the Independently Biased CC and Conventional CC for the second bias case. 81

3.18 Results for the investigation of the dependence of the difference in power gain or $MSG_n - MSG_c$ on the difference in I_{c2} or $I_{c2n} - I_{c2c}$ for the second bias case. 81

4.1 Independently biased 3-stack configurations which are the connection of one common-emitter (CE) or common-source (CS) transistor and two common-base (CB) or common-gate (CG) transistors: a) conventional 3-stack HBT configuration; b) independently biased 3-stack HBT configuration consisting two mid-bias points; c) conventional 3-stack HEMT configuration; b) independently biased 3-stack HEMT configuration consisting two mid-bias points. 86

4.2 Experimental setup for measuring the S-parameters of the independently biased 3-stack HBT MMIC chip. Three transistors have the same emitter size of $2 \times 20\,\mu\text{m}^2 \times 2$ fingers 87

4.3 Realistic experimental setup for on-wafer S-parameters measurement of the MMIC chip. 88

4.4 Effect of I_{b1} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic. 89

4.5 Effect of I_{b2} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic. 90

4.6 Effect of I_{b3} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic. 91

4.7 Effect of V_{cc1} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic. 92

4.8 Effect of V_{cc2} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic. 93

4.9 Effect of V_{cc3} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic. 94

4.10 The conventional, proposed cascode and 3-stack configurations: a) conventional cascode configuration; b) proposed cascode configuration or independently biased cascode configuration; c) 3-stack configuration. 95

4.11 Performances comparison between three types of configurations at I_b = 0.1mA: independently biased 3-tack HBT, the conventional and proposed cascodes; the bias conditions are also shown. Here: a) stability characteristic; b) power gain characteristic; c) isolation characteristic. 96

4.12 Performances comparison between three types of configurations at I_b = 0.2 mA: independently biased 3-tack HBT, the conventional and proposed cascodes; the bias conditions are also shown. Here: a) stability characteristic; b) power gain characteristic; c) isolation characteristic. 97

4.13 Performances comparison between independently biased 3-stack HBT configuration and the conventional one at I_b = 0.1mA; the bias conditions are also given. Here: a) power gain characteristic; b) isolation characteristic. . 99

4.14 Performances comparison between independently biased 3-stack HBT configuration and the conventional one at I_b = 0.2mA; the bias conditions are also given. Here: a) power gain characteristic; b) isolation characteristic. . 100

4.15 The 3-stack HBT MMIC chip based amplifier circuit. 101

4.16 The ADS schematic of the 3-stack HBT MMIC chip based amplifier for simulation. 102

4.17 One-tone gain and PAE characteristics of the amplifier under the influence of the base bias current I_b at f = 1.6 GHz: a) I_{b1} variation; b) I_{b2} variation; c) I_{b3} variation. 103

4.18 One-tone gain and PAE characteristics of the amplifier under the influence of the collector bias voltages at f = 1.6 GHz: a) V_{cc1} variation; b) V_{cc2} variation; c) V_{cc3} variation. 103
4.19 Two-tone IMD3 characteristic of the amplifier under the influence of the base bias current I_b at f = 1.6 GHz and frequency spacing Δf = 4 MHz: a) I_{b1} variation; b) I_{b2} variation; c) I_{b3} variation. 104
4.20 Two-tone IMD3 characteristic of the amplifier under the influence of the collector bias voltage V_{cc} at f = 1.6 GHz and frequency spacing Δf = 4 MHz: a) V_{cc1} variation; b) V_{cc2} variation; c) V_{cc3} variation. 104
4.21 Summary of small-signal and large-signal performances improvement under bias parameters variation. 106
4.22 Fabricated 3-stack HBT MMIC chip based amplifier. 107
4.23 Experimental setup for one-tone signal measurement (gain and efficiency). . 107
4.24 Experimental setup for two-tone signal or distortion (IMD3) measurement. 108
4.25 Realistic experimental setup for measurement of the fabricated amplifier. . 108
4.26 Measured results for the one-tone signal of gain and efficiency of the amplifier. Simulated results are also shown for comparison. 109
4.27 Measured results for two-tone signal (distortion) and one-tone signal (gain and efficiency) of the fabricated amplifier. The simulated results are also shown. 110
4.28 Frequency characteristic of the fabricated amplifier. Simulated results are also shown. 111
4.29 Comparison in distortion, power gain and efficiency performances between independently biased 3-stack amplifier and a conventional one. 112
4.30 The independently biased 3-stack GaN HEMT amplifier circuit with incorporating input and output matching networks for realization of high efficiency. 115
4.31 The ADS schematic of the independently biased 3-stack GaN HEMT MMIC chip based amplifier for simulation. 116

4.32 Dependence of output power, power gain and PAE for one-tone signal on the variation of the gate bias. Other bias values are: $V_{\rm g}$= -2.6 V; $V_{\rm d1}$= 5.0 V; $V_{\rm d2}$ = 4.0 V; $V_{\rm d}$ = 44.0 V 117

4.33 Dependence of IMD3 characteristic for two-tone signal on the variation of the gate bias. Other bias values are: $V_{\rm g}$= -2.6 V; $V_{\rm d1}$= 5.0 V; $V_{\rm d2}$ = 4.0 V; $V_{\rm d}$ = 44.0 V 118

4.34 Dependence of simultaneous PAE and IMD3 characteristics on the variation of the gate bias. Other bias values are: $V_{\rm g}$= -2.6 V; $V_{\rm d1}$= 5.0 V; $V_{\rm d2}$ = 4.0 V; $V_{\rm d}$ = 44.0 V 119

4.35 Dependence of output power, power gain and PAE for one-tone signal on the variation of the drain bias. Other bias values are: $V_{\rm g}$= -2.6 V; $V_{\rm d1}$= 5.0 V; $V_{\rm d2}$ = 4.0 V; $V_{\rm d}$ = 44.0 V 120

4.36 Dependence of IMD3 characteristic for two-tone signal on the variation of the drain bias. Other bias values are: $V_{\rm g}$ = -2.6 V; $V_{\rm d1}$ = 5.0 V; $V_{\rm d2}$ = 4.0 V; $V_{\rm d}$ = 44.0 V 121

4.37 Dependence of simultaneous PAE and IMD3 characteristics on the variation of the drain bias voltages. Other bias values are: $V_{\rm g}$ = -2.6 V; $V_{\rm d1}$ = 5.0 V; $V_{\rm d2}$ = 4.0 V; $V_{\rm d}$ = 44.0 V 122

4.38 Fabricated independently biased 3-stack GaN HEMT power amplifier. The amplifier was fabricated based on the independently biased 3-stack GaN HEMT chip including 3 transistors with the same size of 0.25 μm × 75 μm × 4 fingers. 123

List of Tables

2.1 Calculated results. 52

2.2 Physical parameters of the source tunnel junction. 57

3.1 Bias conditions for the calculation of I_{c2} and MAG of the Conventional CC and Independently Biased CC. 70

3.2 Bias conditions in the investigations (Exp.: experiment; Sim.: simulation). 76

4.1 Summary of the measured small-signal performance investigation. 94

4.2 Summary of the simulated large-signal performance investigation. 105

4.3 Megtron6 substrate information. 106

4.4 List of instruments used for measurement of the fabricated amplifier. . . . 109

4.5 Summary of the simulated and measured optimum performance for comparison. 110

Chapter 1

Introduction

1.1 Introduction to power gain and its related applications

In alternating current (AC) circuit, power is expressed as

$$P_{\mathrm{AC}} = \mathrm{V}_r \mathrm{I}_r \cos\varphi = \frac{1}{2}\mathrm{V}_0 \mathrm{I}_0 \cos\varphi \tag{1.1}$$

where V_r and I_r are root-mean-square values of the AC voltage and current, respectively; V_0 and I_0 are their respective peak values; φ is the phase difference between the AC voltage and current.
AC power can be alternatively given in the complex form as below

$$P_{\mathrm{AC}} = Re(\mathrm{IV}^*) = Re(\mathrm{VI}^*) = \frac{1}{2}(\mathrm{IV}^* + \mathrm{I}^*\mathrm{V}) \tag{1.2}$$

here V^* and I^* means the complex conjugate of V and I, respectively. Sign of the AC power can be minus or plus depending on the direction of the energy flowing into or out of a component. If the electrical energy goes in to a device, the power has a positive sign, this is so-called passive device whereas if the energy goes out of the component, the power has a negative sign, this is so-called active device. Hence, the power consumed on a passive component is positive whereas the active component has negative power consumption.

1.1.1 The need for power in conventional applications

Power in conventional applications are obviously necessary and this is illustrated in Fig. 1.1. In the RADAR system, power plays a key role since its detecting range is directly proportional to the transmitter's output power via the following equation [1]

$$R = \sqrt[4]{\frac{P_{\mathrm{S}}.G^2.\lambda.\sigma}{P_{\mathrm{E}}.(4\pi)^3}} \tag{1.3}$$

where

R: detecting range

P_{S}: transmitting power

P_{E}: receiving power

G: antenna gain

σ: radar cross section

λ: wavelength

In addition to the RADAR system, power is obviously important for mobile communication networks because the base transceiver station (BTS) needs high output power from the transmitter for increasing the coverage range. Moreover, in satellite information or universe exploring science and other related fields, power is crucially necessary for the signal transmitted in free space to be able to have enough energy to reach the destination. In addition to these, for microwave applications, power becomes much more important than the current and voltage since current and voltage cannot be measured directly as done in the low frequency regime. This is because at high frequency regime, the signal propagates in the form of electro-magnetic wave and it is characterized by the electro-magnetic energy. That is reason why all microwave circuit parameters such as power, impedance, etc. are represented through S-parameters which are derived under the view point of electro-magnetic wave [2] [3]. All these mean that for conventional applications power plays a key role for the signal transmitted.

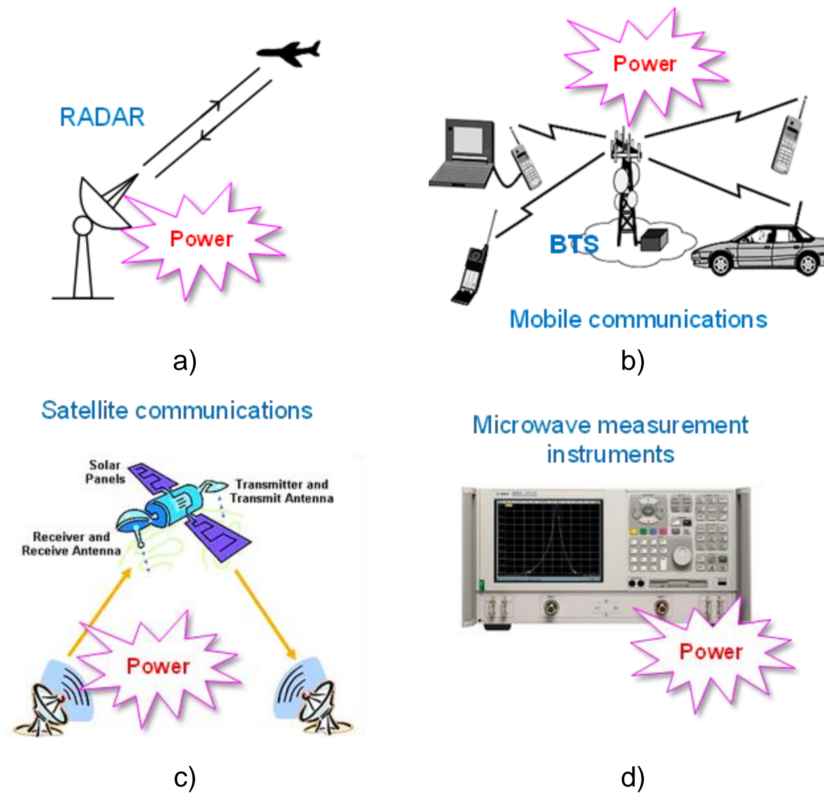


Figure 1.1: The importance of power in conventional applications: a) RADAR systems; b) mobile communication network; c) satellite communications; d) microwave area.

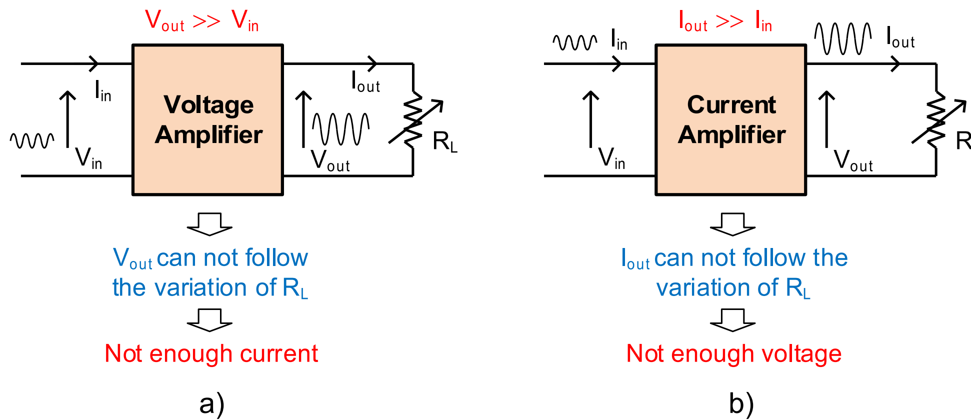


Figure 1.2: Illustration of sole voltage and current amplifier: a) voltage amplifier; b) current amplifier. In either case, there is not enough output power ($V_{\text{out}} I_{\text{out}}$) to follow the variation of the load R_{L}.

1.1.2 The need for power in quantum applications

In quantum applications where the nanoscale devices may not exhibit the power gain property for the signal transmitted as in conventional applications. Despite this fact of low power gain, increasing power gain still plays important role for quantum devices since increasing power gain is a method to enhance output power of the devices, or in other words, the devices can supply enough current and voltage at the output. This can be understood by considering the following simple example:
Figure 1.2 explains in details why power is important for the quantum devices but not the voltage or current. From Eq. (1.1) and Eq. (1.2), it can be seen that power is proportional to both voltage and current. This means to increase the power, solely increasing either voltage (using voltage amplifier) or current (using current amplifier) is not enough. We can easily understand this fact by considering the following simple examples :
- In Fig. 1.2a which relates to the sole voltage amplification, suppose that the voltage amplifier has a high voltage gain of 100, this means the output voltage V_{out} is equal to 1 V if the input voltage V_{in} is 10 mV. The V_{out} of 1 V is possible to supply enough current for a resistive load R_{L} of 1 kΩ with $I_{\text{out}} = 1$ mA. However if the load R_{L} decreases its value from 1 kΩ to a lower value of, says 10 Ω, V_{out} then becomes lower, consequently to remain V_{out} at 1 V, I_{out} must be increased but this is impossible since the voltage amplifier cannot produce extra current in this situation.
- Likewise in Fig. 1.2b which shows the sole current amplification. If the current amplifier has a high current gain of 100 with input current I_{in} of 0.01 mA, the output current I_{out} is then amplified to 1 mA. With R_{L} is, says 1 kΩ, the output voltage becomes 1 V. Nevertheless if R_{L} reduces to says 10 Ω, the current amplifier cannot supply extra voltage to keep the output current I_{out} at 1 mA.
This reveals that in either case, V_{out} and I_{out} cannot follow the variation of the load R_{L} since sole voltage and current amplifier cannot supply extra voltage or current. We all know that up till now major applications for quantum devices

are for logic and digital circuits. These applications take the advantage of the output current driving capability for driving the next circuit stage impedance. However quantum devices, says single electron transistor (SET) always exhibits low voltage gain, leading to the low output current driving capability of these devices. Consequently by increasing their power gain or the output power, the output current driving capability can be improved accordingly as explained in the above example.

1.2 Power gain mechanism

In order to characterize the power gain of a gain element, it is first noted that in general power gain is defined as the ratio of output power from the element to the input power as below:

$$G_{\mathrm{P}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}}. \tag{1.4}$$

we always wish to maximize the power gain of the device in order to provide enough energy to drive the load, this leads to one of the most important definition of power gain called maximum available power gain (MAG) which is expressed as a ratio of the available power from the source P_{avs} to the maximum power delivered to the load from the device P_{avd}

$$\mathrm{MAG} = \frac{P_{\mathrm{avd}}}{P_{\mathrm{avs}}}. \tag{1.5}$$

MAG is only archived under condition of simultaneous conjugate matched at both input and output sides of the gain element. Therefore, in practice it is nearly impossible to obtain MAG since it is unable to simultaneously conjugate match the input and output over a frequency range. However since MAG is the maximum capable of delivering power gain of a gain element, it becomes an important expression to compare the power gain capability among the gain elements and it is widely used in microwave applications. The mechanism of MAG can be simply understood in Fig. 1.3 which shows the general basic power gain mechanism under the view point of small-signal for two-port networks. As can be seen in the figure available power from the source P_{avs} can

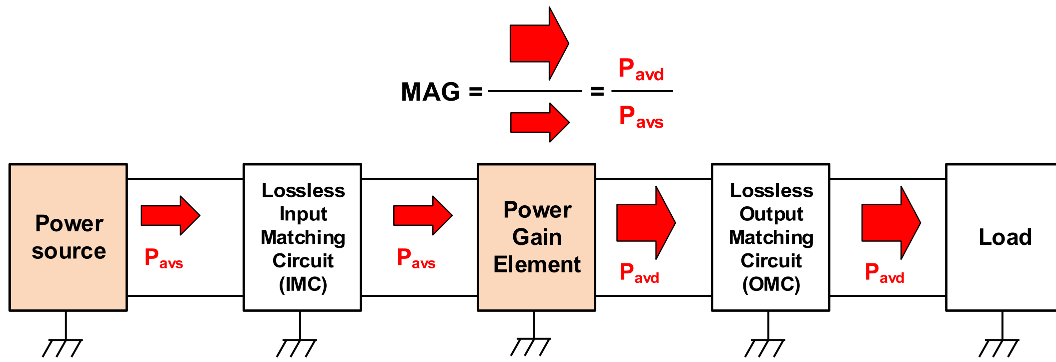


Figure 1.3: Illustration of the basic power gain mechanism for a gain element.

entirely enter the gain element by the use of a loss-less input matching circuit (IMC) to conjugate match the signal source impedance and input impedance of the element. Likewise the available power from the element P_{avd} can also entirely deliver to the load thanks to the use of a loss-less output matching circuit (OMC) to conjugate match the load impedance and the output impedance of the element. Hence the design of IMC and OMC is required to obtain the MAG. It is noted that OMC is more important than the IMC in power gain improvement since it maximizes the output power delivered to the load, thus design of OMC plays a crucial role. In power amplifier design, IMC and OMC are realized by using either lumped elements such as inductors, capacitors or distributed one such as transmission line and the use of whether lumped or distributed elements depends on the operation frequency.

In conclusion, output power and power gain (or MAG) in mechanism only depend on the gain element itself but not on the source or load impedance, purpose of IMC and OMC is just to maximize the intrinsic gain capability of the gain element. That is why device optimization of the gain element is key step for improving power gain and output power.

1.3 Power gain definitions for two-port networks

1.3.1 Power gain definitions

In addition to the MAG, other power gain expressions can be also derived for using in various specific applications. Power gain for a gain element treated as a two-port network can be categorized as the transducer gain, available gain, insertion gain, operating gain, and maximum available gain. These power gain definitions are described on Fig. 1.4 as below:

- Transducer gain (G_{T}): this is the power gain in most common cases, it is defined as the ratio of the power delivered to the load P_{L} (unmatched) to the available power from the source P_{avs} (unmatched)

$$G_{\mathrm{T}} = \frac{P_{\mathrm{L}}}{P_{\mathrm{avs}}} = \frac{|S_{21}|^2(1-|\Gamma_{\mathrm{L}}|^2)(1-|\Gamma_{\mathrm{S}}|^2)}{|1-\Gamma_{\mathrm{in}}\Gamma_{\mathrm{S}}|^2|1-\Gamma_{\mathrm{L}}S_{22}|^2}. \tag{1.6}$$

here Γ_{S}, Γ_{L}, Γ_{in} are the reflection coefficient at the source, load and input sides respectively. The transducer gain depends upon on both the source and load impedances Z_{S} and Z_{L}. It is noted that if the source and load is terminated with the same reference impedance, says 50 Ω, that is, $Z_{\mathrm{S}} = Z_{\mathrm{L}} = Z_0 = 50\,\Omega$ then $\Gamma_{\mathrm{S}} = \Gamma_{\mathrm{L}} = 0$, thus the transducer gain becomes

$$G_{\mathrm{T}} = |S_{21}|^2. \tag{1.7}$$

- Available gain (G_{A}): this power gain is illustrated on Fig. 1.4b. It is defined as the ratio of the matched output power P_{om} to the available power from the source P_{avs} (unmatched)

$$G_{\mathrm{A}} = \frac{P_{\mathrm{om}}}{P_{\mathrm{avs}}} = \frac{|S_{21}|^2(1-|\Gamma_{\mathrm{S}}|^2)}{|1-\Gamma_{\mathrm{S}}S_{11}|^2(1-|\Gamma_{\mathrm{out}}|^2)}. \tag{1.8}$$

in this research this power gain will be used for the investigation of power gain characteristic of the single electron transistor (SET).

- Operating gain (G_o): this power gain is illustrated on Fig. 1.4c. It is defined as the ratio of the matched input power P_{im} to the power delivered to the load

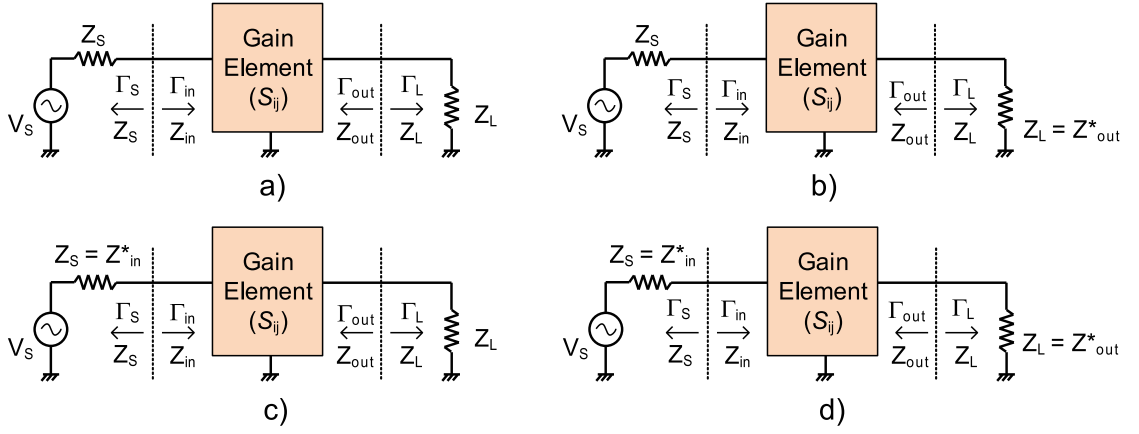


Figure 1.4: Types of power gain definitions for the gain element worked as a two-port network. Here: a) transducer gain; b) available gain; c) operating gain; d) maximum available gain (MAG).

P_{L} (unmatched)

$$G_o = \frac{P_{\mathrm{om}}}{P_{\mathrm{avs}}} = \frac{|S_{21}|^2(1-|\Gamma_{\mathrm{L}}|^2)}{|1-\Gamma_{\mathrm{L}}S_{22}|^2(1-|\Gamma_{\mathrm{in}}|^2)}. \tag{1.9}$$

It can be seen that the operating gain depends on the load impedance Z_{L} but not on the source impedance Z_{S}.

- Maximum available gain (G_{max}): this power gain is defined as the ratio of the input matched power to the output matched power as shown on Fig. 1.4d. Since the condition for power gain of a gain element to reach the maximum gain is simultaneously conjugate matching at the load and source sides, in practice it is nearly impossible to archive this gain. It is expressed as follows

$$\mathrm{MAG} = (K - \sqrt{K^2-1})\left|\frac{S_{21}}{S_{12}}\right|. \tag{1.10}$$

where $K > 1$ (or the circuit in a stable state), it is the Rollet stability factor. If $K < 1$ (or the circuit in an unstable state), maximum gain is then expressed in other term namely maximum stable gain (MSG) as below

$$\mathrm{MSG} = \left|\frac{S_{21}}{S_{12}}\right|. \tag{1.11}$$

here K is given as

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}S_{21}|}. \tag{1.12}$$

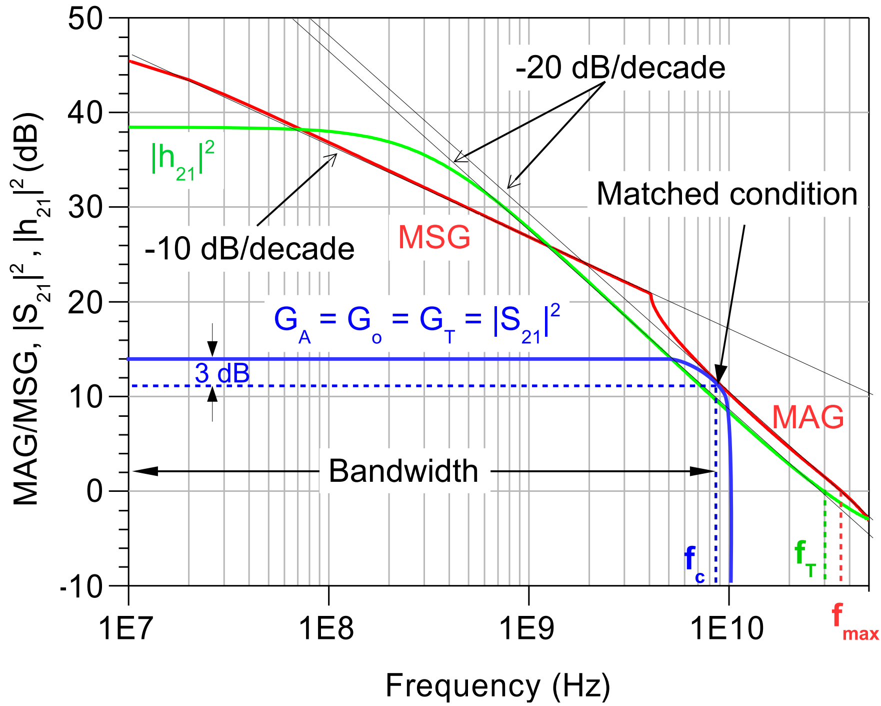


Figure 1.5: Typical curves for short-circuit current gain and power gains of a common-emitter (CE) 2 μm x 20 μm x 2 InGaP/GaAs heterojunction bipolar transistor (HBT) (WIN Semiconductor Corp. model) under bias condition: $V_{\mathrm{ce}} = 4.0$ V, $I_{\mathrm{b}} = 0.12$ mA. It is noted here that $|S_{21}|^2$ curve can reach to MAG curve at the point of matched condition. Here $f_{\mathrm{c}} = 9.2$ GHz, $f_{\mathrm{T}} = 29.7$ GHz, $f_{\max} = 36.4$ GHz.

with S_{ij} the two-port S-parameters. If the 2-port is terminated with the source and load impedance Z_0 which is equal to the reference impedance of the system, G_{T}, G_{A}, and G_{o} then become to an unique expression as:

$$G_{\mathrm{T}} = G_{\mathrm{A}} = G_{\mathrm{o}} = |S_{21}|^2. \tag{1.13}$$

It is noted that since MAG is widely used in microwave applications, it will be used for power gain investigation of the conventional transistors including InGaP/GaAs HBT and GaN HEMT in chapter 3 and chapter 4 of this research. In summary, it once again concluded that maximum gain (MAG/MSG) is the maximum capability of delivering power gain for a gain element or in general a two-port network. This fact is illustrated in Fig 1.5 where shows the typical

curves for MAG/MSG and other power gains of a gain element under a matched condition $Z_S = Z_L = Z_0 = 50\,\Omega$.

1.3.2 Figures of merits of device related to power gain definitions

According to the power gain definitions in previous section, several figures of merits of the device can be derived from Fig. 1.5. These merits are very important to determine potential practical applications for the device and they are power gain cut-off frequency f_c, short-circuit current gain cut-off frequency f_T, and maximum oscillation frequency f_{max}. In Fig. 1.5, it can be seen that f_c is defined as the frequency at which the power gain in Eq. (1.13) drops by 3 dB and f_T is defined as the frequency at which the short-circuit current gain of the device $|h_{21}|^2$ becomes unity whereas f_{max} is defined as the frequency at which the maximum available gain (MAG) of the device becomes unity. Here, because at low frequency the maximum power gain is proportional to $1/f$ with f the operation frequency, it rolls off by -10 dB/decade whereas at high frequency it is proportional to $1/f^2$, therefore it rolls off by -20 dB/decade; the short-circuit current gain $|h_{21}|^2$ rolls off by a slope of -20 dB/decade. While f_c is used to determine bandwidth of the device and it is directly proportional to f_{max} under a matched condition, f_T and f_{max} are used to define that whether the device can be used for digital or communication applications respectively. Since f_T relates to the intrinsic operation speed which is corresponding to the carrier transit time of the device τ_t or the response time, it is always used for digital application whereas since f_{max} relates to the power gain capability of the device, it is always used for microwave and communication applications. Following section will consider more details the practical applications of the device regarding to these figures of merits of the device using step response simulation.

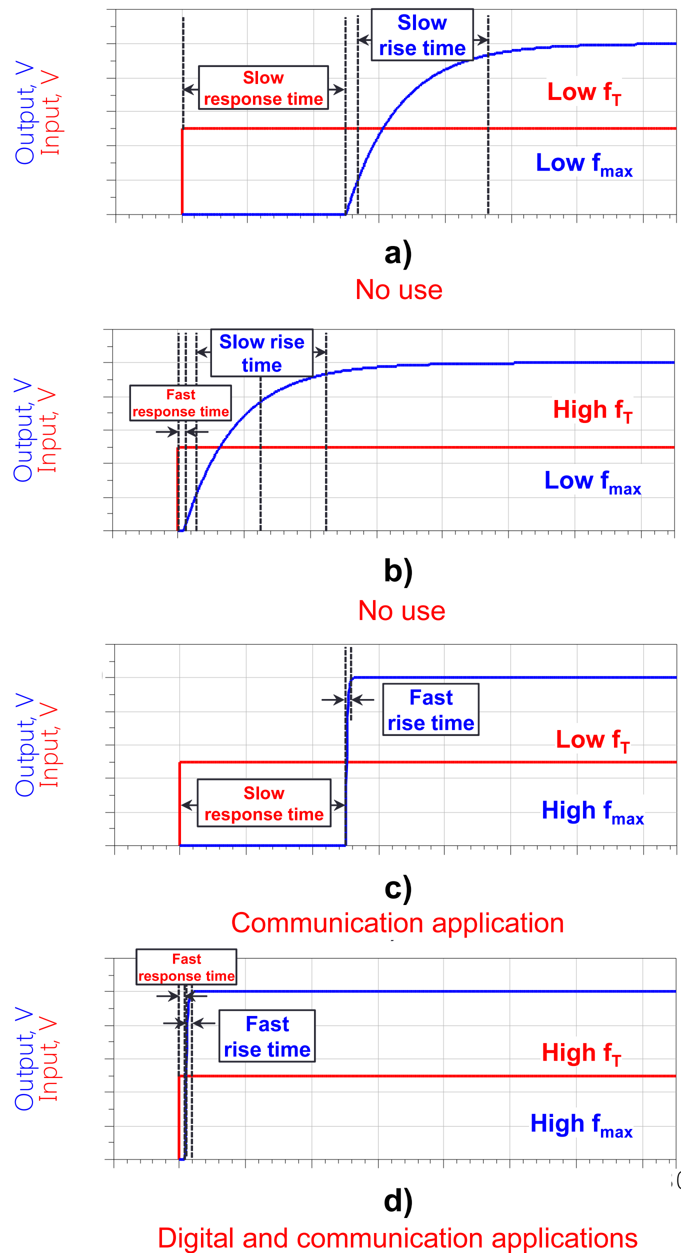


Figure 1.6: Typical step response of a transistor and its related possible applications: a) the output signal having slow response time and slow rise time; b) the output signal having fast response time and slow rise time; c) the output signal having slow response time and fast rise time; d) the output signal having fast response time and fast rise time. Here fast response time and fast rise time means high f_T and high f_{max} respectively and vice verse.

1.4 Practical applications related to figure of merits of the device

This section introduces to practical applications for device in term of its figure of merits including f_{T} and f_{max}, the two most important merits of the device as introduced in previous section. It is widely known that f_{T} relates to the carrier transit time of an active device as

$$f_{\mathrm{T}} \simeq \frac{1}{2\pi\tau_{\mathrm{t}}}. \tag{1.14}$$

where τ_{t} is the electron transit time from source to drain for an FET and from emitter to collector for a BJT. This implies the higher the f_{T}, the faster the output response time or the higher the operation speed of the device.
In a same manner, f_{c} which is directly proportional to f_{max} as can be seen in Fig. 1.5 under a matched condition relates to the rise time of the output signal t_{a} as below equation [4]

$$f_{\mathrm{c}}t_{\mathrm{a}} \simeq 1/3. \tag{1.15}$$

The above equation means the higher the f_{c} (hence f_{max}), the faster the rise time of the output signal. Therefore, by considering these merits of the device, their potential applications can be realized as summarized in Fig. 1.6. The figure illustrates typical cases corresponding to potential applications of the device regarding to its merits. In Fig. 1.6d if the device exhibiting both fast output response time (high f_{T}) and fast output rise time (high f_{max}) suits for both digital and communications applications, consequently this is the most desirable case. In Fig. 1.6c where the device shows slow output response time (low f_{T}) and fast output rise time (high f_{max}) is just suitable for communication applications but not digital applications. On the other hand, in Fig. 1.6b in which although the device exhibits fast output response time (high f_{T}), it shows slow output rise time (low f_{max}), making it not suitable for both digital and communication applications. The worst case can be seen in Fig. 1.6a where the device shows both slow output response time (low f_{T}) and slow output rise time (low f_{max}), as a result the device owing such a behavior

cannot be used for any practical applications as well.

In summary from the above discussion it can be clearly seen that finding methods for increasing the device's power gain as well as its merits including f_T and f_{max} is obviously crucial to bring the device into practical applications. However before introducing to classical methods for power gain improvement, it is first necessary to review power gain mechanism and power gain definitions of the devices which will be presented in the next section.

1.5 Methods for power gain improvement

Mechanism of power gain improvement for electron devices can be easily understood by considering below simple power gain formulas:

$$G_p = \frac{P_{out}}{P_{in}}. \tag{1.16}$$

while the power is given as

$$P = i^2 R. \tag{1.17}$$

This means

$$G_p = \left(\frac{i_{out}}{i_{in}}\right)^2 \left(\frac{R_{out}}{R_{in}}\right). \tag{1.18}$$

Eq. (1.18) reveals that in mechanism power gain can be enhanced by two ways. The first one is controlling the ratio of output resistance to input resistance while the same current flowing from input to output and this is so-called *tran*sfer re*sistor* (*transistor*) method. The second one is controlling the ratio of output current to the input current, thus this method is so-called current transfer. Following sections will show how these methods can apply to conventional transistors including BJT and FET.

1.5.1 Power gain improvement for BJT/HBT

As the name suggested this section outlines the method for power gain improvement of conventional transistors (BJT and HBT) by the use of resistance and current transfer control.

Firstly, let's consider the case of BJT. For a simple analysis, assuming that

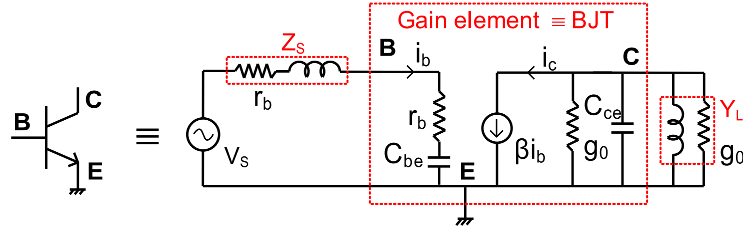


Figure 1.7: Simplified small-signal equivalent circuit for BJT where both the input and output sides are simultaneous conjugate matched.

the BJT is unilateral or in other words, the collector-base capacitance (C_{bc}) is not dealt with. Figure 1.7 shows a simplified small-signal equivalent circuit for a typical common-emitter (CE) BJT which is always used for the purpose of power gain investigation. It can be seen in the figure that output and input sides are conjugate matched for deriving the expression of MAG. MAG of BJT then can be derived as

Available power from the source P_{avs}:

$$P_{\mathrm{avs}} = \frac{|i_{\mathrm{b}}|^2 r_{\mathrm{b}}}{4}. \tag{1.19}$$

where r_{b} is the base resistance of BJT.

Matched output power

$$P_{\mathrm{matched}} = \frac{|i_{\mathrm{c}}|^2 r_0}{4}. \tag{1.20}$$

MAG of the BJT is then given as

$$\mathrm{MAG} = \frac{P_{\mathrm{matched}}}{P_{\mathrm{avs}}} = \left|\frac{i_{\mathrm{c}}}{i_{\mathrm{b}}}\right|^2 \frac{r_0}{r_{\mathrm{b}}}. \tag{1.21}$$

where r_0 and r_{b} are the BJT's output and base resistances respectively.

Using the following relationship

$$i_{\mathrm{c}} = \beta i_{\mathrm{b}}. \tag{1.22}$$

here β is the beta current gain of the BJT, finally the MAG expression becomes

$$\mathrm{MAG} = \beta^2 \left(\frac{r_0}{r_{\mathrm{b}}}\right). \tag{1.23}$$

The above equation is very insightful because the ratio r_0/r_b means power gain of a BJT originates from the mechanism of resistance transfer. In other words, in order to exhibit the power amplification, BJT must be fabricated in such a way that the base resistance r_b is reduced. It is widely known that reduction of base resistance relates to the high doping in the base region. As a result increasing base doping concentration is a way for power gain improvement of BJT.

Furthermore, consideration for power gain improvement of BJT in term of the current transfer control in Eq. 1.19 can be realized using below relationship

$$\beta i_\mathrm{b} = g_\mathrm{m} v_\mathrm{b}. \tag{1.24}$$

then β becomes

$$\beta = \frac{g_\mathrm{m}}{\omega C_\mathrm{be}}. \tag{1.25}$$

where g_m is the BJT's transconductance, now MAG has a new form

$$\mathrm{MAG} = \left(\frac{r_0}{r_\mathrm{b}}\right) \frac{g_\mathrm{m}^2}{\omega^2 C_\mathrm{be}^2}. \tag{1.26}$$

with $\omega = 2\pi f$ the operation frequency. From the above equation we can see that the increase of current transfer now can be realized through increasing BJT's transconductance g_m. In small-signal analysis, g_m is expressed via below formula [5]

$$g_\mathrm{m} = \frac{I_\mathrm{C}}{V_\mathrm{T}}. \tag{1.27}$$

where V_T is the thermal voltage, it is typically equal to 26 mV at room temperature. The above formula shows that transconductance of BJT is directly dependent on its collector current. This dc collector current in turn depends on the BJT's structure parameters at a specific bias point as follows [6]

$$I_\mathrm{C} = \frac{qAD_\mathrm{n}n_\mathrm{i}^2}{2W_\mathrm{B}N_\mathrm{A}} e^{(V_\mathrm{BE}/V_\mathrm{T})}. \tag{1.28}$$

where:

q: electric charge

A: base-emitter junction area

W_B: base width or base region thickness

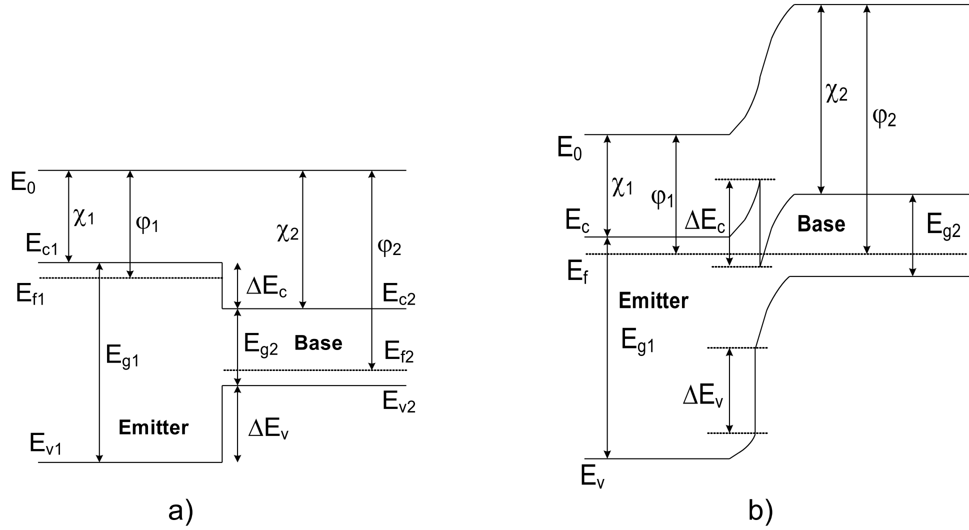


Figure 1.8: Typical energy band diagram of an HBT: a) before energy band formation and b) after energy band formation.

D_n: diffusion constant in the base region

n_i: intrinsic carrier concentration

V_BE: DC base voltage

V_T: thermal voltage

N_A: doping density in the base region

From Eq. (1.26)-Eq. (1.28), it is evident that decreasing the base width W_B increases the transconductance of BJT, making its current gain (or current transfer) to increase, as a result power gain is improved. However one issue arises here is decreasing W_B results in the increase of the base resistance, making power gain degraded. Hence in the conventional BJT or homojunction BJT, its power gain cannot be enhanced by reducing the base width and base resistance simultaneously. In other words we cannot use the methods of resistance transfer and current transfer for power gain improvement in the case of homojunction BJT simultaneously.

The mentioned issue can be overcome by taking the advantage of the heterojunction structures and this leads to a new BJT is so-called heterojunction bipolar transistor (HBT). In 1950s Schockley proposed a way of using two ma-

terials with different bandgap, a wide bandgap material (AlGaAs, InGaP, InP) in the emitter and a narrow bandgap material (GaAs, InGaAs) in the base in order to form a heterojunction device [7]. A typical energy band diagram of the HBT is described in Fig. 1.8 where we can see the different bandgaps E_{g1} and E_{g2} for two materials in the emitter and base. This creates a discontinuity in conduction and valance band of the heterojunction between the emitter and base of the HBT as shown in Fig. 1.8b. Here the total discontinuity ΔE_g is equal to the sum of the discontinuity in conduction band ΔE_c and the discontinuity in valance band ΔE_v, that is

$$\Delta E_g = \Delta E_c + \Delta E_v. \tag{1.29}$$

the different in energy between two materials in the conduction band and valance band has become the most important feature of the HBT compared to the conventional BJT. Thanks to this discontinuity in energy band ΔE_g, the above intrinsic drawbacks of conventional BJT can be resolved by considering the following equation relating to the maximum current gain of HBT

$$\beta_{max} = \frac{N_{De} L_e D_b}{N_{Ab} W_{bn} D_e} e^{(\Delta E_g / k_B T)}. \tag{1.30}$$

where N_{De}: emitter doping level
D_b: diffusion coefficient in the base
L_e: diffusion length in the emitter
N_{Ab}: base doping level
W_{bn}: base thickness
D_e: diffusion coefficient in the emitter
k_B: Boltzmann constant
T: temperature
the above equation shows that since current gain (or current transfer) of HBT can be very high (on the order of thousands) arising from energy band difference ΔE_g between two materials, we can simultaneously decrease the base thickness W_{bn} and increase the base doping level (for low base resistance) with a little sacrifice of the high current gain. In other words by applying the heterojunction structure to BJT, the increase of current transfer and resistance

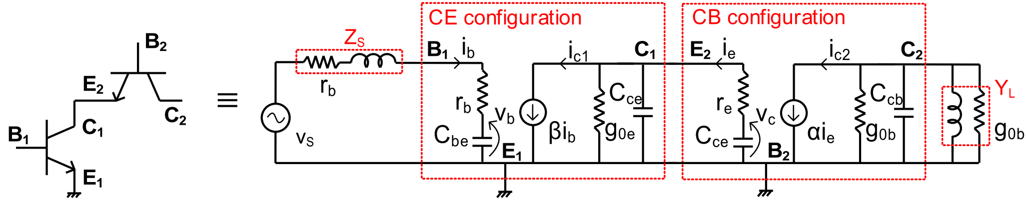


Figure 1.9: Simplified small-signal equivalent circuit with both input and output conjugate matched of the BJT cascode configuration.

transfer for power gain improvement can be archived simultaneously for the case of HBT. This is an obvious advantage of the HBT compared with the conventional BJT and it makes HBT to be a promising device for high power and high frequency applications.

- **Power gain improvement by increasing of resistance transfer using multi-stage devices connection**.

An alternative way to control the resistance transfer for power gain improvement of BJT is using the multi-stage devices connection. The multi-stage configuration is investigated in this section is so-called cascode configuration. BJT Cascode configuration is realized by connecting the first-stage common-emitter (CE) transistor and the second-stage common-base (CB) transistor [8] [9] [10]. Simplified equivalent circuit for this type of circuit configurations is illustrated in Fig. 1.9. The cascode configuration can deliver higher power gain compared to the single-stage transistor (CE configuration) in term of resistance transfer by considering the following MAG expressions:

- *MAG of the BJT-based cascode structure.*

$$\mathrm{MAG} = \frac{P_{\mathrm{matched}}}{P_{\mathrm{avs}}} = \left|\frac{i_{\mathrm{c2}}}{i_{\mathrm{b}}}\right|^2 \frac{r_{0\mathrm{b}}}{r_{\mathrm{b}}}. \tag{1.31}$$

Since in cascode operation, the collector current flowing through CE and CB transistors has the same value, or $i_{\mathrm{c2}} = i_{\mathrm{c1}}$, the difference in MAG between the cascode and CE circuit is the difference between their output resistance under

conjugate matched condition. Or in other words

$$\frac{\mathrm{MAG_{cascode}}}{\mathrm{MAG_{CE}}} = \frac{r_{\mathrm{ob}}}{r_{\mathrm{oe}}}. \tag{1.32}$$

here r_{ob} and r_{oe} are the output resistances of CE and CB transistors respectively. We all know that output resistance of CB transistor r_{ob} is relatively larger than that of CE transistor r_{oe} because in the CB configuration collector-base junction is inversely biased whereas in the CE configuration the base-emitter is forwards biased. Consequently power gain of the cascode configuration becomes higher than that of the single-stage or CE configuration as expected.

- **High frequency figure of merits of BJT/HBT**.

Besides power gain improvement analysis, now let's consider high-frequency figure of merits for BJT/HBT as analyzed in previous section to see how to enhance these merits. The current gain cut-off frequency f_{T} of BJT/HBT is given as:

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{be}}}. \tag{1.33}$$

where g_{m} and C_{BE} are BJT/HBT transconductance and its base-emitter capacitance, respectively. Clearly f_{T} can be enhanced by improving g_{m} and decreasing C_{BE}. This is the same as improvement of the power gain by decreasing the base width using heterojunction structure. Moreover, by using the heterojunction structure, the C_{BE} is also decreased, making f_{T} to be improved significantly.

The maximum oscillation frequency f_{max} of BJT/HBT is given as:

$$f_{\mathrm{max}} = \sqrt{\frac{f_{\mathrm{T}}}{8\pi C_{\mathrm{bc}} R_{\mathrm{b}}}}. \tag{1.34}$$

The above equation shows that f_{max} is improved by reducing the base resistance R_{b}. This can once again be done by taking the advantage of the heterojunction structure of HBT. As mentioned before, thanks to the heterojunction structure, the W_{B} can be increased and the R_{b} can be decreased simultaneously for power gain enhancement. This means that by using this technique, not only improved the power gain, but also the figure of merits can be improved as well.

1.5.2 Power gain improvement for FET and high electron mobility transistor (HEMT)

In addition to the BJT and HBT, the same power gain improvement methods for a device in term of current transfer and resistance transfer can also be applied to FET and HEMT which is described through MAG expression as below regarding to the Fig. 1.10:
Available power from the source P_{avs}:

$$P_{\mathrm{avs}} = \frac{|v_{\mathrm{S}}|^2}{4r_{\mathrm{g}}}. \tag{1.35}$$

where r_{g} is the gate resistance of FET.
Matched output power

$$P_{\mathrm{matched}} = \frac{|i_{\mathrm{d}}|^2 r_{\mathrm{ds}}}{4} = \frac{(g_{\mathrm{m}}|v_1|)^2 r_{\mathrm{ds}}}{4}. \tag{1.36}$$

MAG of the FET then becomes

$$\mathrm{MAG} = \frac{P_{\mathrm{matched}}}{P_{\mathrm{avs}}} = g_{\mathrm{m}}^2 \left|\frac{v_1}{v_S}\right|^2 r_{\mathrm{ds}} r_{\mathrm{g}}. \tag{1.37}$$

here v_{S} and v_1 relates to each other through following relationship

$$\left|\frac{v_1}{v_{\mathrm{S}}}\right| = \frac{1}{2r_{\mathrm{g}}\omega C_{\mathrm{gs}}}. \tag{1.38}$$

Finally MAG expression of FET becomes

$$\mathrm{MAG} = \left(\frac{r_{\mathrm{ds}}}{r_{\mathrm{g}}}\right) \frac{g_{\mathrm{m}}^2}{4\omega^2 C_{\mathrm{gs}}^2}. \tag{1.39}$$

here C_{gs} is the gate-source capacitance. Equation 1.25 has the same form as BJT. This means FET also has the following features related to the power gain enhancement:

+ The resistor transfer mechanism which is represented by the ratio $r_{\mathrm{ds}}/r_{\mathrm{g}}$.

+ The current transfer improvement is also expressed in term of transconductance g_{m} improvement.

+ The gate resistance r_{g} should be decreased to improve power gain. This relates to the optimization of the gate geometry.

However the main difference in power gain enhancement between FET and

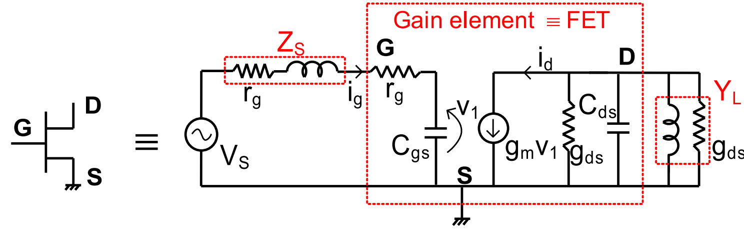


Figure 1.10: Simplified small-signal equivalent circuit for FET where both the input and output sides are simultaneous conjugate matched.

BJT is in the transconductance g_{m} improvement or current transfer improvement. g_{m} of FET has the following expression [11]

$$g_{\mathrm{m}} = 2\frac{I_{\mathrm{ds}}}{(V_{\mathrm{GS}} - V_{\mathrm{th}})}. \tag{1.40}$$

with I_{ds} the drain current of FET and it is given as

$$I_{\mathrm{ds}} = \frac{\mu C_{\mathrm{ox}}}{2}\frac{W_{\mathrm{c}}}{L_{\mathrm{c}}}(V_{\mathrm{gs}} - V_{\mathrm{th}})^2. \tag{1.41}$$

where:

μ: surface mobility of electron in the channel

C_{ox}: gate oxide capacitance

W_{c}: channel width

L_{c}: channel length

V_{DS}: DC drain-source voltage

V_{GS}: DC gate-source voltage

V_{th}: threshold voltage

From Eq. (1.39)-Eq. (1.41), it can be seen that to improve MAG of FET, its channel length L_{g} should be decreased for the transconductance increase.

In summary, in the case of FET, resistance transfer increase is realized by modifying the gate geometry while the current transfer increase is realized by the reduction of its channel length. Besides these ways, the current transfer of FET can be also enhanced by increasing the output current using heterojunction structure which is the same as HBT. The heterojunction used for FET is so-called HEMT. Today HEMT is the most important active electronic device

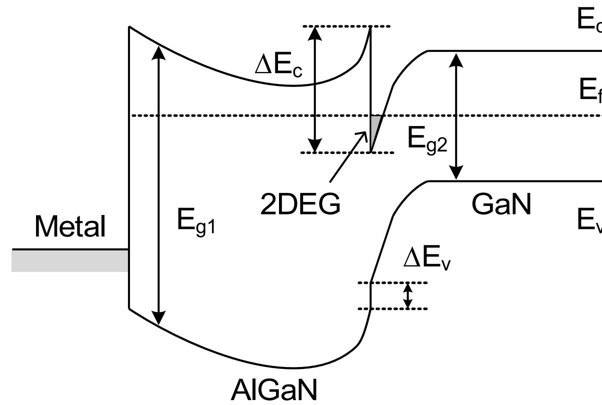


Figure 1.11: Typical energy band diagram of an AlGaN/GaN HEMT.

for high power and high frequency applications. It was first developed by T. Mimura *et al.* [12] in 1980 and this device also benefits from the formation of heterojunciton which is formed from two compound semiconductor materials with different bandgap [13]. The most common materials used in HEMT are InAlAs/InGaAs, AlGaAs/GaAs or AlGaN/GaN. A typical energy band diagram after formation for an AlGaN/GaN HEMT device is illustrated in Fig. 1.11. The key point in operation of the HEMT compared with Si-based conventional FET is the formation of two-dimensional electron gas (2DEG) originated from the difference in bandgap between E_{g1} and E_{g2} as can be seen in the figure. Thanks to this feature, the mobility of electrons in the 2DEG becomes extremely high due to the reduction of their degree of freedom, that is 3 reduced to 2. The high electron mobility feature makes HEMT to be able to operate at a very high frequency range, or in other word a high speed device. Moreover, by the use of GaN material which has wide bandgap (3.4 eV) and high breakdown field (3.5 MV/cm), HEMT can deliver very high output current density (about 1 A/mm), this leads to a very high current transfer characteristic, making its power gain remarkably improved.

- **Power gain improvement by increasing of resistance transfer using multi-stage devices connection**.

By connecting FET or HEMT in multi-stage configuration, the resistance

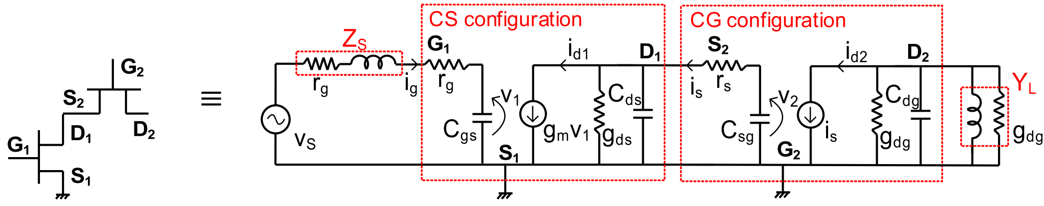


Figure 1.12: Simplified small-signal equivalent circuit with both input and output conjugate matched of the FET cascode configuration.

transfer becomes increased accordingly. Here the cascode configuration which is realized by connecting the first common-source (CS) FET and the second common-gate (CG) FET is always considered for power gain study. Similar to the case of BJT, from Fig. 1.12, MAG difference between the FET-based cascode structure and single-stage (or CS) transistor can be easily derived as below:

$$\frac{\mathrm{MAG}_{\mathrm{cascode}}}{\mathrm{MAG}_{\mathrm{CS}}} = \frac{r_{\mathrm{gd}}}{r_{\mathrm{ds}}}. \tag{1.42}$$

where r_{gd} and r_{ds} are the output resistances of CG and CS transistors under conjugate matched condition respectively. It is also well known that in the case of FET output resistance of CG is usually higher than that of the CS. This once again confirms the benefits of using the cascode configurations not only for BJT but also FET for power gain improvement in term of resistance transfer control.

- **High frequency figure of merits of FET/HEMT**.

Now in addition to power gain improvement for FET/HEMT, let's find out solutions how to enhance figure of merits of FET/HEMT as analyzed in the case of BJT/HBT. f_{T} of FET/HEMT is expressed as:

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{gs}}}. \tag{1.43}$$

It is once again seen that enhancement of f_{T} by increasing g_{m} is the same as power gain improvement method, that is, using wide bandgap materials like GaN of HEMT to increase the drain current or the g_{m}. $f_{\max}$ of FET/HEMT

is given as:

$$f_{\max} = \sqrt{\frac{f_{\mathrm{T}}}{2\pi C_{\mathrm{gd}} r_{\mathrm{g}}}}. \tag{1.44}$$

Eq. (1.44) means $f_{\max}$ is enhanced by reducing the gate resistance r_{g}, similar to the method of power gain improvement.

From the above discussions on the power gain and figure of merits enhancement of BJT/HBT and FET/HEMT, it can be concluded that power gain and figure of merits of BJT/HBT and FET/HEMT can be improved using the same method.

In this thesis, the use of current transfer or transconductance improvement method will be applied to a quantum device (single-electron transistor (SET)) whereas power gain improvement for a new cascode configuration namely independently biased cascode structure is studied and compared with a conventional cascode structure using the resistance transfer method. Before starting the main chapters for power gain study of the quantum and conventional devices, brief introduction to the most important quantum devices including single-electron transistor and resonant tunneling device will be shortly outlined in the next section.

1.6 Brief introduction to two important quantum devices

Transistor scaling bring us obvious benefits including higher device density, higher speed and lower power consumption. Hence this trend is now becoming a great attention of researchers, leading to the development of emerging devices such as resonant tunneling and single electron transistor (SET).

- **Single electron transistor (SET)**.

This section just briefly introduces to the SET, its detailed operation as well as our related study on SET will be presented in the next chapter. SET is a nanoscale device and it is the key element in the recent field of nanotechnology

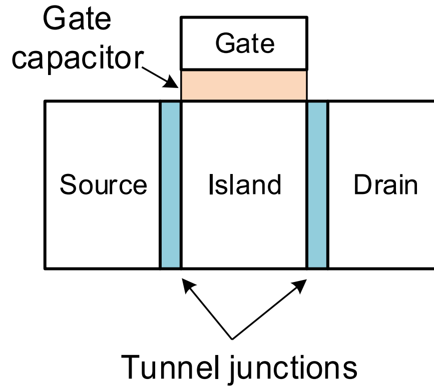


Figure 1.13: Illustration of the SET structure.

due to its advantages such as ultra-low power consumption, and especially extremely small size (at nanoscale) [14] [15] [16]. However an intrinsic drawback of SET is it can only work under a very low temperature condition. Figure 1.13 shows an illustration of SET's structure where we can see it consists of a nanoscale island or a quantum dot which is isolated with the source and drain terminals by two tunneling junctions. These two tunneling junctions usually made with metal while the island can be made with metal or Si material and they build the potential barriers to block electron to tunnel through from source to drain via island if the charging energy is not high enough. The mechanism in operation of the SET bases on the Coulomb blockade effect [17] [18] which can be simply explained in Fig. 1.14. If the electrostatic energy on the island is not high enough for the electron injected from the source to the island, it is blocked as illustrated in Fig. 1.14a. By adjusting the island's energy via tuning the gate potential, discrete electron can be tunnel through the source and drain junctions one by one, resulting in tunneling current. Here the charging energy E_c or the energy necessary for an electron tunneling via thin junction is given by

$$E_\mathrm{c} = \frac{e^2}{2C_\Sigma}. \tag{1.45}$$

where e and C_Σ are elementary charge and total capacitance of SET respectively. The above interesting phenomenon is so called Coulomb blockade and it

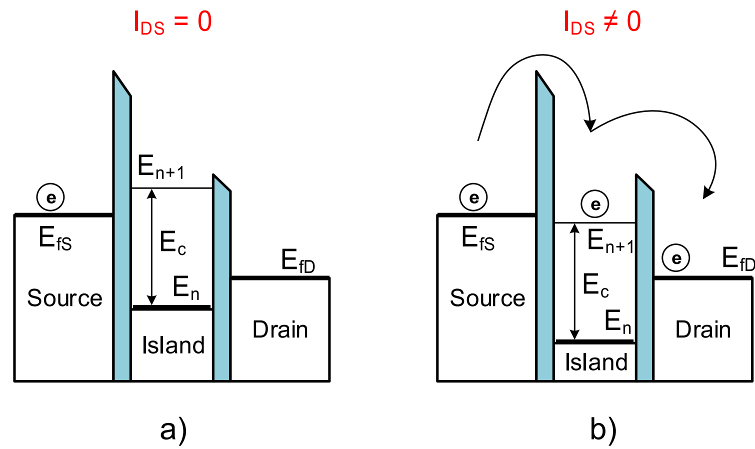


Figure 1.14: Illustration of operation of SET.

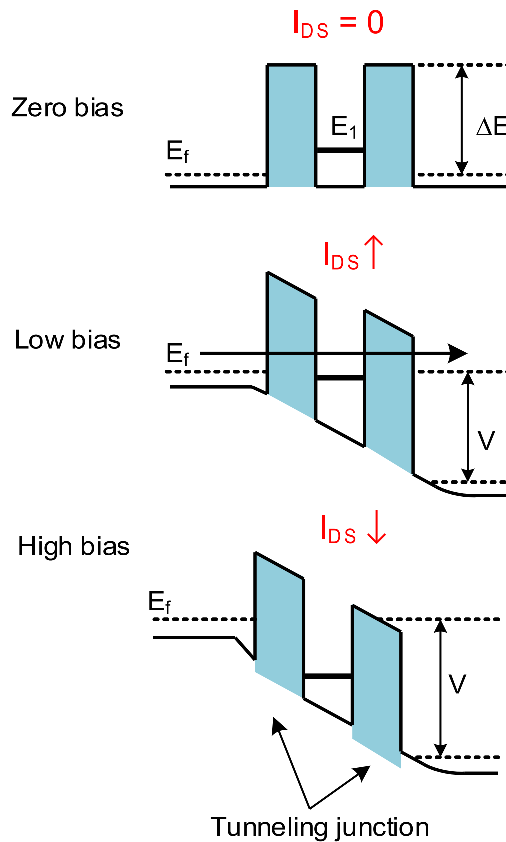


Figure 1.15: Typical energy band structure of a resonant tunneling device.

plays a key role in not only SET but in all quantum devices of single-electronic area. From the above discussion, SET can be considered as an ultra-high speed device due to the fact that the tunneling time of electron through a thin

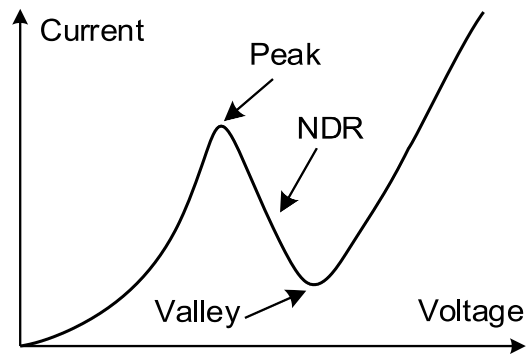


Figure 1.16: Typical IV characteristic of an RTD which exhibits the negative differential resistance (NDR).

junction is extremely fast. In addition the advantage of high speed, power consumption on the SET is also very low since its tunneling current is just on the order of nano ampere. To date, most studies of SET have been focused on its current and voltage gain for logical and memory applications by taking the advantage of the Coulomb blockade phenomenon. To our best knowledge, its power and power gain has never been investigated before. For this reason, in this thesis, power characteristic of the SET is studied for the first time using the method of current transfer control as mentioned before.

- **Resonant tunneling transistor (RTT)**.

Besides SET there exists another promising device which also takes the advantage of quantum effect for high speed and low power consumption namely resonant tunneling transistor (RTT) [19] [20] [21]. A very important advantage of RTT over SET is it can operate at room temperature. The typical energy band diagram for an resonant tunneling structure is described in Fig. 1.15. The figure shows that when the device is under an applied voltage V, electrons tunnel through two thin potential barriers. This means the carrier transport mechanism in RTT is also tunneling and this makes the device to work at very high speed as the same mechanism as the SET. When the voltage increases the tunneling current accordingly increases and reaches a peak value, if we further increase the applied voltage the tunneling current decreases from the peak to

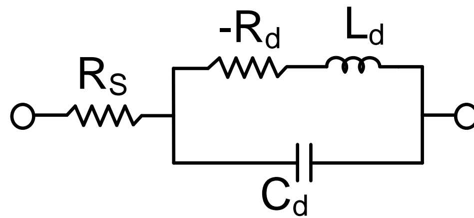


Figure 1.17: Small-signal equivalent circuit of RTT. Here R_S is series resistance, R_d, L_d and C_d are internal resistance, inductance and capacitance, respectively.

a valley value. This behavior of the RTT is represented by its IV characteristic as illustrated in Fig. 1.16. Another key feature of the RTT which is shown in its IV characteristic is it exhibits the negative differential resistance (NDR), this means it can be regarded as an active device, therefore it can exhibit gain characteristic. The small-signal equivalent circuit of RTT is illustrated in Fig. 1.17, here the most important parameter of RTT is R_d which accounts for the negative differential resistance region. From this equivalent circuit, maximum oscillation frequency f_max of RTT is derived as:

$$f_\mathrm{max} = \frac{1}{2\pi R_\mathrm{d} C_\mathrm{d}}. \tag{1.46}$$

According to Eq. (1.46), in order to enhance f_max of RTT, its internal resistance and capacitance must be reduced. This can be done by optimizing the doping profile of the layers, the geometry as well as increasing peak current and reducing valley current. Various applications for RTT to date has been realized like high speed switching and logic applications [22]. The recent research trend on RTT is the same as SET, that is mainly focused on the logic and digital applications [23] [24] but not the power. However It is very possible that in the near future along with the main study on high frequency and switching speed, power gain of quantum devices including SET and RTT will attract much concern from the researchers for wireless data transmission applications.

1.7 Outline of the thesis

This thesis includes two main goals, the first is studying power gain improvement methods for quantum device and conventional transistors and the second one is investigating microwave performances including power gain, isolation, stability, efficiency and linearity for independently biased 3-stack InGaP/GaAs HBT and GaN HEMT configurations. With these major goals taken into account, the thesis is structured as follows:
The first chapter presents the motivation and background of the thesis on the power gain and introduces the methods for power gain improvement for conventional transistors including BJT/HBT and FET/HEMT. In chapter 2, power gain and its improvement using the current transfer method for single electron transistor (SET) is studied for the first time. From the view point of resistance transfer method for power gain improvement, chapter 3 takes the advantage of the independently biased cascode configuration to study its power gain in comparison with that of the conventional cascode configuration based on InGaP/GaAs HBT MMIC chips. In chapter 4, various microwave performance improvements including high power gain, low distortion of 3-stack InGaP/GaAs HBT and GaN HEMT configurations is investigated by taking the advantage of two added bias terminals to realize another much more effectively independently biased feature. Finally chapter 5 will summarize the main points of the thesis.

Chapter 2

Method for power gain enhancement of single-electron transistor (SET)

2.1 Introduction

The invention of transistor, the key active device in electronic circuits and systems, is considered one of the greatest invention in 20th century. Over the years, attempt to scale down the transistor, especially the metal oxide semiconductor field effect transistor (MOSFET), to sub-micron size has been done to realize the higher density of the devices, smaller chip, lower power dissipation, higher speed and lower cost per functionality. This trend is natural and cannot be persist as predicted by the Moore's law which stated the density of transistors per integrated circuit had been doubling by manufacturers per regular intervals and this trend would continue [25]. However when scaling down to sub-micron size, MOSFET faces a number of issues such as short channel effect, gate leakage, high field mobility degradation etc. [26] [27]. Although there have been various technological solutions to these issues including high-k gate dielectric, silicon-on-insulator (SOI), ultrathin body (UTB) etc. [28] they are still inherent problems of the MOSFET when being scaled down. In addition, the size of the MOSFET cannot be reduced to any scale, for instance at nanoscale, since

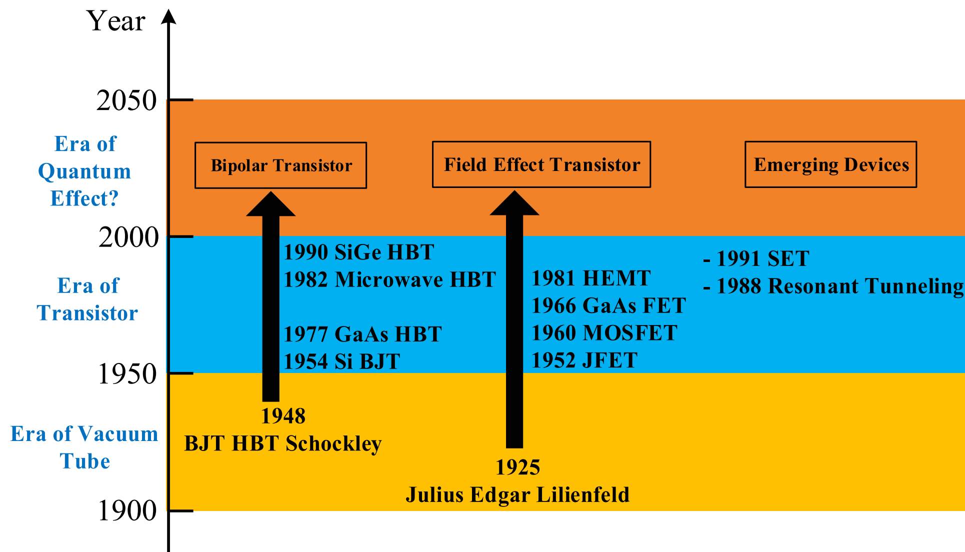


Figure 2.1: The evolution of transistor from the beginning to the appearance of emerging devices.

at this scale the fabrication process encounters very strong challenges such as dopant fluctuations and the cost for fabrication measurement instruments. That is the reason why it is necessary to find out emerging technologies to invent new devices at nanoscale in order to co-operate with conventional CMOS devices in order to overcome their drawbacks. The evolution of the transistors from the time of invention to date is illustrated in Fig. 2.1 [29]. As can be seen in the figure, in the near future, nanoscale devices can be probably replace the conventional devices as the same trend in history when bipolar junction transistor (BJT) replaced the vacuum tube and then BJT was replaced with field effect transistor (FET). This is possible because the nanoscale devices such as nanotube, single-electron transistor, resonant tunneling diode, etc are considered to have many advantages compared with the conventional devices. These advantages include ultra low power dissipation, high integration and high speed [30] [31]. On the other hand, they also face obvious problems and one of the most challenging issue is room temperature-operation [32]. This issue arises from the mechanism of nanoscale devices' operation in which only discrete electron moves across tunneling junctions, resulting in tunneling cur-

rent while in conventional semiconductor devices, the current is created by the movement of masses of the electrons. This means in nanoscale devices the electron addition energy, the energy necessary for one electron tunnels through a junction

$$E_{\mathrm{A}} = E_{\mathrm{C}} + E_{\mathrm{K}} \simeq E_{\mathrm{C}}. \tag{2.1}$$

must be greater than the thermal energy $k_{\mathrm{B}}T$, or

$$E_{\mathrm{A}} > k_{\mathrm{B}}T. \tag{2.2}$$

where $E_{\mathrm{A}}, E_{\mathrm{C}}, E_{\mathrm{K}}$ denote addition energy, charging energy and quantum kinetic energy respectively, k_{B} and T are the Boltzmann constant and operation temperature. This condition is so-called the Coulomb blockade effect [33] [34] [35], it ensures that the operation of single-electron devices is not affected by the thermal fluctuation. Eq. (2.2) also shows that the operation temperature of single-electron devices must be very low, on the order of tens of Kelvin compared to the room temperature 300 K. Despite low temperature operation and other drawbacks, until now there have been many potential applications for nanoscale devices such as memory, RF, multiple valued logic, interconnects, etc. [36] [37] [38].

As discussed above, in the future the nanoscale devices will possibly replace the conventional ones as a natural trend of transistor evolution and among the nanoscale devices, single-electron transistor (SET) is one of the most interesting devices since in operation it actually works as a transistor like a FET with three terminals: gate, drain and source and moreover it works under the govern of quantum effects. The operation mechanism of this device will be explained in details in the next section. Over the years, although many researches have been done focusing on the theory as well as applications of SET, the practical applications of this device are still in early stage and remain uncertain due to its operation temperature limit and difficulty in fabrication process. Recent studies on SET are mainly about logic and memory applications which only takes the advantage of its Coulomb staircase and oscillation [39] [40]. Other

articles focused on radio-frequency SET (RF-SET) electro-meters [41] [42]. In addtion to these studies, some researches concerned the hybrid operation of SET and conventional MOSFET [43] [44]. Although voltage and current gain of SET have been also investigated in some literature [45] [46] [47], one of the most important characteristics of active devices, the power gain which relates to the current driving capability of nanoscale devices, has never been investigated, especially for the SET. For this reason, in this chapter, study on the power gain characteristic and novel method to improve the power gain of SET is carried out and it is found that by reducing the source junction thickness, power gain of SET can be enhanced remarkably.

2.2 Operation of single-electron transistor (SET)

2.2.1 Background of SET

SET is a nanoscale device, its structure is shown on Fig. 2.2. As can be seen in the figure, SET consists of small "island" (or a quantum dot) with the diameter on the order of nano meter and it is isolated from around by two tunnel junctions. The island can be made with either metal (Al, Ti, Au, etc) or silicon (Si) whereas the tunnel junction is created with two conducting electrodes separated by an insulator (AlO_x, SiO_2, etc) which is thin enough so that electron can tunnel through. Electrically the tunnel junction can be modeled by a parallel connection of a resistor (R_{TS} and R_{TD}) and a capacitor (C_{TS} and C_{TD}) and its value depends on the size of the junction such as the thickness and area. The potential of the island is controlled by the gate terminal or gate-to-source voltage (V_{GS}) through the gate capacitor. In theory, the gate terminal can be coupled to the island whether by capacitive coupling or resistive coupling , however in practice, most of the SET devices use the capacitive coupling. According to "Orthodox" theory [48] [49] which was developed by Kulik and Shkhter, to ensure that the quantizied charge Q = Ne, with N an integer, tunnels from the source terminal to the drain terminal via the island, creating the tunneling current, the following requirements must be fulfilled: +

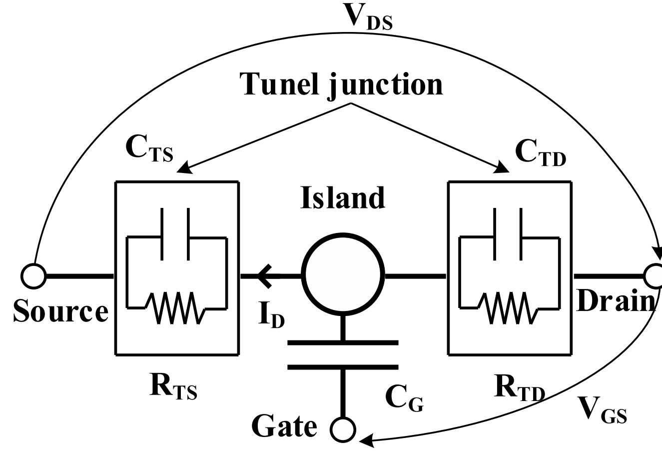


Figure 2.2: The equivalent basic diagram of SET.

Condition for junction resistance:

$$R_T > R_k = h/e^2 \simeq 25.8\,k\Omega \tag{2.3}$$

here R_k is the resistance quantum. This condition is satisfied to guarantee that the "cotunneling" effect which means several simultaneous electrons tunnel via junction, doesn't take place. + Condition for operation temperature:

$$T \ll e^2/(2k_B C_\Sigma) \tag{2.4}$$

This condition is the same as (2.2) and it means SET can only operate at low temperature, here e is elementary charge and the total capacitor is given as

$$C_\Sigma = C_{\mathrm{TS}} + C_{\mathrm{TD}} + C_{\mathrm{G}} \tag{2.5}$$

where $C_{\mathrm{TS}}, C_{\mathrm{TD}}, C_{\mathrm{G}}$ are the source junction, drain junction and gate capacitors respectively. We can see that the current in SET is the tunneling current which is governed by quantum mechanical law, it is in natural different from the drift and diffusion currents in conventional MOSFET device. Hence, in order to study characteristics of SET, especially the power gain functionality, it is required to develop an appropriate and precise drain current model of SET which taking the advantage of the quantum effect especially the Coulomb

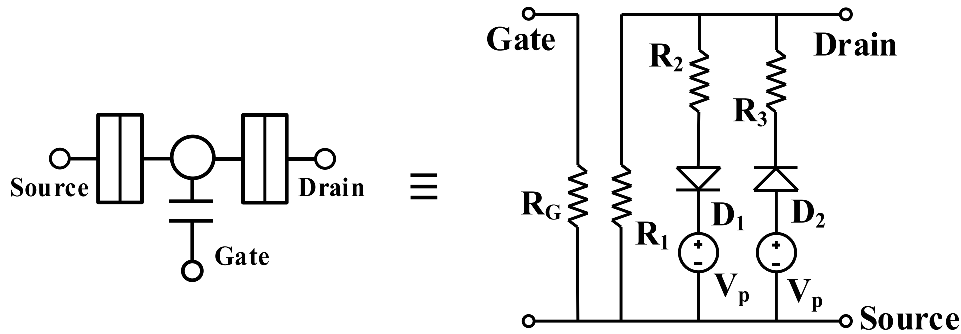


Figure 2.3: The SPICE macro model proposed by Yu. Here $R_{\mathrm{G}} = 100\,\mathrm{G\Omega}$; $R_1(V_{\mathrm{GS}}) = CR_1 + CR_2 cos(\pi CF_1 V_{\mathrm{GS}})$; $R_2 = R_3 = CV_{\mathrm{p}}/(CI_2 - 2CV_{\mathrm{p}}/R_1(V_{\mathrm{GS}}))$.

blockade phenomenon. Until now, such models have been proposed and developed by many researchers and group researches. Uchida [34], from Toshiba Inc. had developed his SET model in 2000. However, this model is only applied to symmetrical devices, that is the source junction resistance is equal to the drain junction resistance. In 2003, Inokawa [50] from NTT Laboratory, improved Uchida model to work with symmetrical devices. Nevertheless, both two models are limited by condition $| V_{\mathrm{DS}} | \leq e/C_{\Sigma}$. MIB model (Mahapatra, Ionescu, and Banerjee [49], from Ecole Polytechnique Federale de Lausanne (EPFL)) had been proposed in order to overcome the drawbacks of the Uchida and Inokawa model. This model is based on the master equation (ME) method and it can be applied to both symmetrical and asymmetrical devices. Moreover, it takes into account the effect of background charge and not limited by the condition $| V_{\mathrm{DS}} | \leq e/C_{\Sigma}$ as the previous two models. In addition to the models of SET, various methods applied to Computer-Aided Design (CAD) tools have been also introduced to simulate the operation of the device. Monte Carlo (MC) technique is one of such methods. In this method, electron transports based on the probabilities of tunneling events which are chosen randomly. This method is considered to be most accurate among SET's simulation methods. Some popular MC-based simulators are SIMON [51] [52], KOSEC [53], SENECA [54], MOSES [55]. Another simulation method is master equation

(ME). Contrary to MC method, in ME method, one needs to solve the master equation to find out the state of the circuit. One ME-based simulator is SETTRANS [56]. The last simulation technique is using SPICE macro model as can be seen on Fig. 2.3 which was developed by Yu [57] in 1999. This technique is quite accurate and consumes less CPU time than MC simulation and it may be a good solution for co-operation between the SET and CMOS devices because SET behavior are studied by using its equivalent circuit. In spite of the mentioned advantages, this method is empirical and not physically based. To date, SIMON simulator which is based on MC technique is still considered to be the most accurate and popular among the SET simulators. Hence in our study, this simulator is chosen to validate and confirm our calculated results for power gain investigation of the SET.

2.2.2 Important parameters of the SET

+) SET's drain current:

In this section, drain current of SET is analytically calculated using Inokawa model . This is not only a compact and but also high accuracy model with just 5% error compared with the SIMON simulator [58]. Moreover, the model can be applied for not only symmetrical but asymmetrical devices. It is expressed by the following equations [50]:

$$I_n = \frac{e}{4C_\Sigma R_\mathrm{T}} \frac{(1-r^2)(\tilde{V}_\mathrm{GS}^2 - \tilde{V}_\mathrm{DS}^2)\sinh\left(\frac{\tilde{V}_\mathrm{DS}}{\tilde{T}}\right)}{A}, \tag{2.6}$$

where

$$\begin{aligned} A = &\left[\tilde{V}_\mathrm{GS}\sinh\left(\frac{\tilde{V}_\mathrm{GS}}{\tilde{T}}\right) - \tilde{V}_\mathrm{DS}\sinh\left(\frac{\tilde{V}_\mathrm{DS}}{\tilde{T}}\right)\right] \\ &+ r\left[\tilde{V}_\mathrm{DS}\sinh\left(\frac{\tilde{V}_\mathrm{GS}}{\tilde{T}}\right) - \tilde{V}_\mathrm{GS}\sinh\left(\frac{\tilde{V}_\mathrm{DS}}{\tilde{T}}\right)\right], \end{aligned} \tag{2.7}$$

with

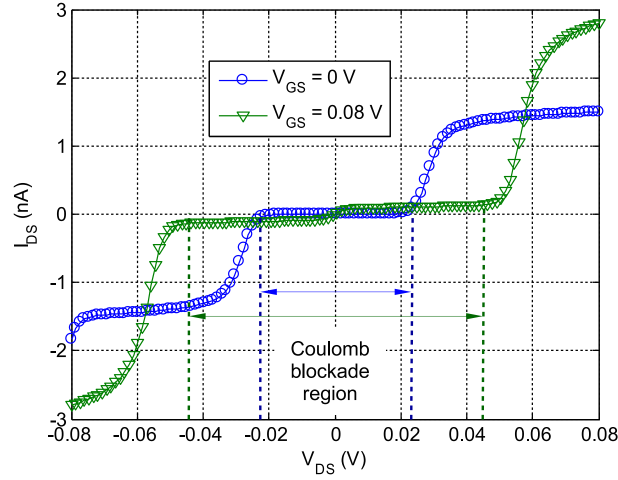


Figure 2.4: The typical $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic of SET plotted by using Eq. (2.9). The parameters' values are $R_{\mathrm{TD}} = 1\,\mathrm{M}\Omega$, $R_{\mathrm{TS}} = 19\,\mathrm{M}\Omega$, $C_{\mathrm{G}} = 1\,\mathrm{aF}$, $C_{\mathrm{TS}} = 1.9\,\mathrm{aF}$, $C_{\mathrm{TD}} = 0.1\,\mathrm{aF}$, $T = 18.6\,\mathrm{K}$.

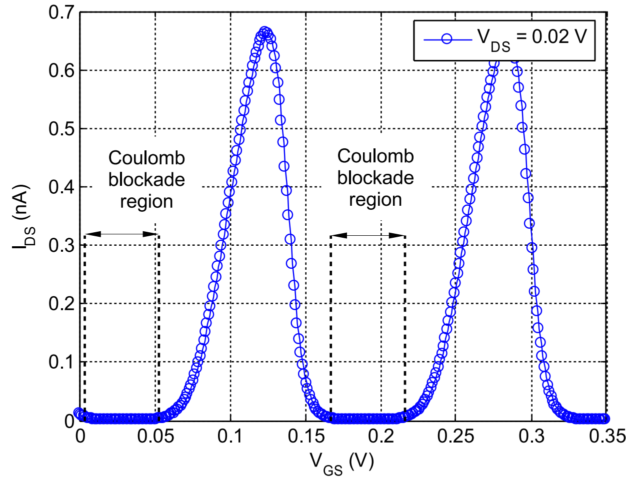


Figure 2.5: The typical $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ characteristic of SET plotted by using Eq. (2.9). The parameters' values are the same as $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic.

$$\tilde{V}_{\mathrm{GS}} = \frac{2C_G V_{\mathrm{GS}}}{e} - \frac{(C_G + C_{\mathrm{TS}} - C_{\mathrm{TD}})V_{\mathrm{DS}}}{e} - 2n - 1, \tag{2.8a}$$

$$\tilde{V}_{\mathrm{DS}} = \frac{C_\Sigma V_{\mathrm{DS}}}{e}; \; \tilde{T} = \frac{k_B T}{e^2/2C_\Sigma}, \tag{2.8b}$$

$$r = \frac{R_{\mathrm{TD}} - R_{\mathrm{TS}}}{R_{TD} + R_{\mathrm{TS}}}; \; R_T = \frac{2R_{\mathrm{TD}} R_{\mathrm{TS}}}{R_{\mathrm{TD}} + R_{\mathrm{TS}}}. \tag{2.8c}$$

the drain current of SET is then calculated as

$$I_{\mathrm{D}} = \sum_{n} I_{\mathrm{n}}. \tag{2.9}$$

here k_{B} is the Boltzmann constant while V_{GS} and V_{DS} represent the gate-to-source and drain-to-source voltages respectively; $\tilde{V}_{\mathrm{GS}}$ and $\tilde{V}_{\mathrm{DS}}$ denote their normalized values; T and $\tilde{T}$ are operation temperature and normalized temperature respectively whereas R_{T} is the harmonic mean of tunneling resistance. In this model, the island of SET is considered to be made with metal. Using this analytic model, I-V characteristic of the SET has been constructed as shown in Fig. 2.4 and Fig. 2.5. In these figures, it can be clearly seen the Coulomb blockade effect which takes place periodically with respect to the variation of V_{GS}. Within the Coulomb blockade region, the drain current becomes zero, this means there is no electrons tunneling through the junctions. On the other hand outside this region, discrete electron tunnels through source and drain junctions via the island, creating tunneling current or drain current. Thanks to this behavior, SET is obviously suitable for logic applications since it exhibits two states ON and OFF due to the variation of V_{GS} and V_{DS}.

+) SET's drain conductance and transconductance:

Drain conductance and transconductance of the SET, namely g_{d} and g_{m} respectively, can be easily derived by taking the derivatives of the drain current (2.9) with respect to V_{DS} and V_{GS} respectively, this means

$$g_{\mathrm{d}} = \left.\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{DS}}}\right|_{V_{\mathrm{GS}}=\mathrm{constant}} \tag{2.10}$$

$$g_{\mathrm{m}} = \left.\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}}\right|_{V_{\mathrm{DS}}=\mathrm{constant}} \tag{2.11}$$

From (2.10) and (2.11), drain conductance and transconductance characteristics of the SET are plotted on Fig. 2.6 and Fig. 2.7.

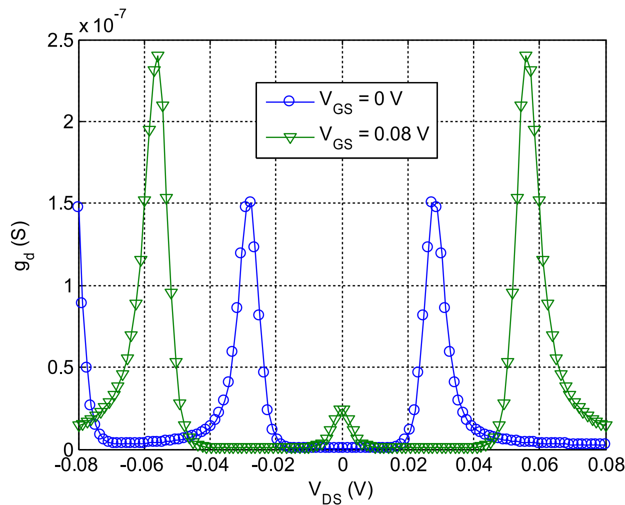


Figure 2.6: Drain conductance characteristic of the SET. The Coulomb blockade effect still exists and repeats periodically. The SET's parameters still remain same as when calculating $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic.

2.2.3 Conductance and transconductance characteristics of SET according to MIB model

This section will analytically investigate the conductance and transconductance of SET utilizing MIB model. As discussed before, to date the MIB model which is based on MC technique has many advantages compared to other models such as simplicity, compact, yet high accuracy, and efficient. The model requires the two assumptions: the first one is it obeys the orthodox theory and the second one is the interconnect capacitances of SET are much larger than the device capacitances, or in other words, the total capacitance of the SET (C_{Σ}) is equal to the sum of the junction capacitances plus the gate capacitance

$$C_{\Sigma} = C_{\mathrm{TS}} + C_{\mathrm{TD}} + C_{\mathrm{G}}. \tag{2.12}$$

Now the drain current of SET is calculated by the following equation [49]:

$$I_{\mathrm{D}} = e \sum_{n=-\infty}^{\infty} p_n \left(\overrightarrow{\Gamma}_{\mathrm{S}}(n) - \overleftarrow{\Gamma}_{\mathrm{S}}(n) \right) = e \sum_{n=-\infty}^{\infty} p_n \left(\overrightarrow{\Gamma}_{\mathrm{D}}(n) - \overleftarrow{\Gamma}_{\mathrm{D}}(n) \right). \tag{2.13}$$

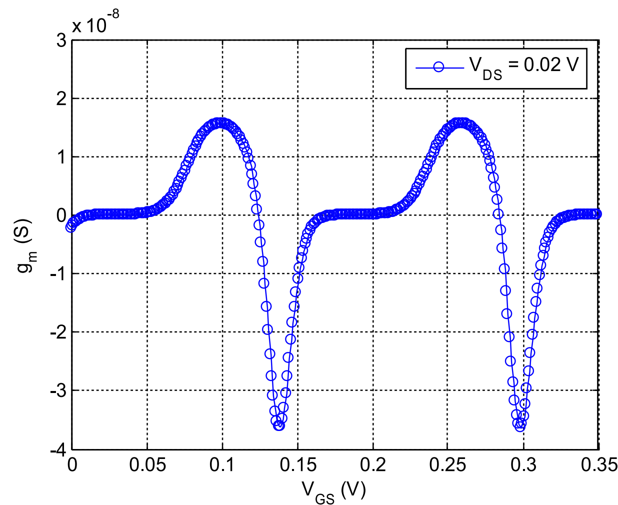


Figure 2.7: Transconductance characteristic of the SET. The Coulomb blockade effect still exists and repeats periodically.

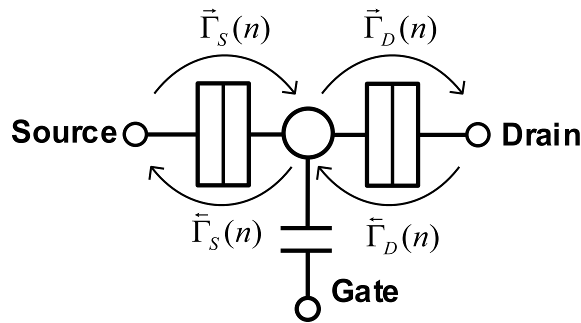


Figure 2.8: Transconductance characteristic of the SET. The Coulomb blockade effect still exists and repeats periodically.

where n is the number of electrons on the island of the SET and p_n is the probability of finding that n electrons on the island. As we can clearly see on the Fig.2.8, the notation $\overleftarrow{\Gamma}_S$ and $\overrightarrow{\Gamma}_S$ represent the electrons tunnel through the source junction from the source terminal to the island and from the island to the source terminal respectively. Similarly, $\overleftarrow{\Gamma}_S$ and $\overrightarrow{\Gamma}_S$ represent the electrons tunnel through the drain junction from the island to the drain terminal and from the drain terminal to the island respectively. According to the orthodox theory Γ is the tunneling rate of one electron tunneling through the junction.

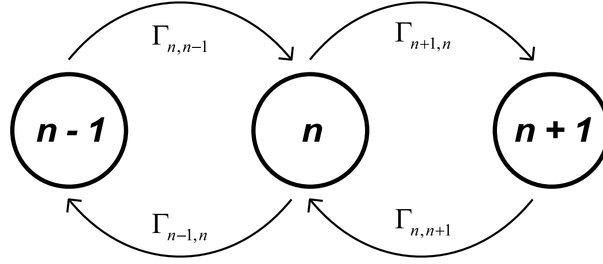


Figure 2.9: Transconductance characteristic of the SET. The Coulomb blockade effect still exists and repeats periodically.

It is given as [49]

$$\Gamma(\Delta G) = \frac{-\Delta G}{e^2 R_T \left(1 - e^{\frac{-\Delta G}{k_B T}}\right)}. \tag{2.14}$$

here ΔG means the difference in Gibbs energy between the initial and final state of the device and R_T is the junction resistance. The probability of finding n electrons on the island p_n is expressed by the master equation (ME) as below

$$\frac{dp_n}{dt} = \Gamma_{n,\,n+1} \cdot p_{n+1} + \Gamma_{n,\,n-1} \cdot p_{n-1} - (\Gamma_{n+1,\,n} + \Gamma_{n-1,\,n}) \cdot p_n. \tag{2.15}$$

From the Fig.2.8 and Fig.2.9, it can be seen that if the island is charged from n electrons to $n+1$ electrons, there are two such possibilities, that are tunnel from the source terminal to the island and from the drain terminal to the island. On the other hand, if the electrons on the island reduce from n to $n-1$ electrons, there are also two possibilities, that are tunnel from the island to the source terminal and from the island to the drain terminal. This implies

$$\Gamma_{n+1,\,n} = \overrightarrow{\Gamma}_\mathrm{S}(n) + \overleftarrow{\Gamma}_\mathrm{D}(n). \tag{2.16}$$

$$\Gamma_{n-1,\,n} = \overleftarrow{\Gamma}_\mathrm{S}(n) + \overrightarrow{\Gamma}_\mathrm{D}(n). \tag{2.17}$$

Now let me calculate the change in Gibbs free energy ΔG. We can see that the total charges on the island relates to the charges on the gate, source and drain capacitances via below equation

$$Q_\mathrm{t} = Q_\mathrm{S} - Q_\mathrm{D} - Q_\mathrm{G}. \tag{2.18}$$

where Q_{t}, Q_{S}, Q_{D}, and Q_{G} are the total charge on the island, the charge on the gate, source and drain capacitances respectively. Applying the Kirchhoff's voltage law, these charges are dependent on the respective voltages and capacitances as

$$V_{\mathrm{GS}} = \frac{Q_{\mathrm{S}}}{C_{\mathrm{TS}}} + \frac{Q_{\mathrm{G}}}{C_{\mathrm{G}}}. \tag{2.19}$$

$$V_{\mathrm{DS}} = \frac{Q_{\mathrm{S}}}{C_{\mathrm{TS}}} + \frac{Q_{\mathrm{D}}}{C_{\mathrm{TD}}}. \tag{2.20}$$

From (2.16), (2.17), (2.18) we can find the solution for the charges

$$Q_{\mathrm{G}} = \frac{C_G}{C_\Sigma}\left[V_{\mathrm{GS}}C_{\mathrm{TS}} + C_{\mathrm{TD}}(V_{\mathrm{GS}} - V_{\mathrm{DS}}) - Q_{\mathrm{t}}\right]. \tag{2.21}$$

$$Q_{\mathrm{S}} = \frac{C_{\mathrm{TS}}}{C_\Sigma}\left[V_{\mathrm{DS}}C_{\mathrm{TD}} + C_{\mathrm{G}}V_{\mathrm{GS}} + Q_t\right]. \tag{2.22}$$

$$Q_{\mathrm{D}} = \frac{C_{\mathrm{TD}}}{C_\Sigma}\left[V_{\mathrm{DS}}C_{\mathrm{TS}} + C_{\mathrm{G}}(V_{\mathrm{GS}} - V_{\mathrm{DS}}) - Q_{\mathrm{t}}\right]. \tag{2.23}$$

The Gibbs free energy of an SET is given as

$$G = E - Q_{\mathrm{D}}V_{\mathrm{DS}} - Q_{\mathrm{G}}V_{\mathrm{GS}}. \tag{2.24}$$

where E is electrostatic energy and then the difference in the free energy is

$$\Delta G = G_{\text{final}} - G_{\text{initial}} = \Delta E - \Delta Q_{\mathrm{D}}V_{\mathrm{DS}} - \Delta Q_{\mathrm{G}}V_{\mathrm{GS}}. \tag{2.25}$$

Let's consider the following cases when the island is charged by the tunnel of electrons from the source terminal to the drain terminal and vice verse one by one:

- **The island is charged when an electron tunnels from the source terminal to the island.**

In this case, the change in the electrostatic energy can be calculated as

$$\Delta E = \frac{\left[-(n+1)e\right]^2 - (-ne)^2}{2C_\Sigma} = \frac{(2n+1)e^2}{2C_\Sigma}. \tag{2.26}$$

In addition, the changes of the charges in Eq. 2.24 is calculated from (2.21) and (2.23) as follows

$$\Delta Q_{\mathrm{G}} = \frac{C_{\mathrm{G}}}{C_\Sigma}e. \tag{2.27}$$

$$\Delta Q_{\mathrm{D}} = \frac{C_{\mathrm{TD}}}{C_\Sigma}e. \tag{2.28}$$

Finally, the expression for ΔG can be obtained

$$\begin{aligned}\Delta G|_{S\to I} &= \frac{(2n+1)e^2}{2C_\Sigma} - e\frac{C_{\mathrm{TD}}}{C_\Sigma}V_{\mathrm{DS}} - e\frac{C_G}{C_\Sigma}V_{\mathrm{GS}} = \\ &= \frac{(2n+1)e^2}{2C_\Sigma} - eV_{island}.\end{aligned} \tag{2.29}$$

From this, the tunneling rate of one electron tunneling from the source to the island $\overrightarrow{\Gamma}_{\mathrm{S}}$ according to (2.14) is given as

$$\overrightarrow{\Gamma}_S(n) = \frac{eV_{island} - \frac{(2n+1)e^2}{2C_\Sigma}}{e^2R_T\left[1 - e^{\frac{\frac{(2n+1)e^2}{2C_\Sigma} - eV_{island}}{k_BT}}\right]}. \tag{2.30}$$

- The island is charged when an electron tunnels from the island to the source terminal.

In a same manner as previous case, we can obtain the expressions for ΔG and $\overleftarrow{\Gamma}_{\mathrm{S}}$ as below

$$\Delta G|_{I\to S} = eV_{island} - \frac{(2n+1)e^2}{2C_\Sigma}. \tag{2.31}$$

$$\overleftarrow{\Gamma}_{\mathrm{S}}(n) = \frac{\frac{(2n+1)e^2}{2C_\Sigma} - eV_{island}}{e^2R_T\left[1 - e^{\frac{eV_{island} - \frac{(2n+1)e^2}{2C_\Sigma}}{k_BT}}\right]}. \tag{2.32}$$

- The island is charged when an electron tunnels from the island to the drain terminal.

Similar to the two previous cases, we have

$$\Delta G|_{I\to D} = e(V_{island} - V_{\mathrm{DS}}) - \frac{(2n-1)e^2}{2C_\Sigma}. \tag{2.33}$$

$$\overrightarrow{\Gamma}_D(n) = \frac{\frac{(2n-1)e^2}{2C_\Sigma} - e(V_{island} - V_{\mathrm{DS}})}{e^2R_T\left[1 - e^{\frac{e(V_{island} - V_{DS}) - \frac{(2n-1)e^2}{2C_\Sigma}}{k_BT}}\right]}. \tag{2.34}$$

- The island is charged when an electron tunnels from the drain terminal to the island.

In this case, the expressions for ΔG and $\overleftarrow{\Gamma}_S$ are derived as follows

$$\Delta G|_{D\to I} = \frac{(2n+1)e^2}{2C_\Sigma} - e(V_{island} - V_{DS}). \tag{2.35}$$

$$\overleftarrow{\Gamma}_D(n) = \frac{e(V_{island} - V_{\mathrm{DS}}) - \frac{(2n-1)e^2}{2C_\Sigma}}{e^2 R_T \left[1 - e^{\frac{\frac{(2n-1)e^2}{2C_\Sigma} - e(V_{island} - V_{\mathrm{DS}})}{k_B T}}\right]}. \tag{2.36}$$

In order to reduce the complexity for the calculation of the drain current, it is assumed that the operation temperature is low enough and the SET is symmetric, moreover the tunneling phenomenon occurs only in one direction. The last assumption gives

$$\overrightarrow{\Gamma}_{\mathrm{S}}, \overrightarrow{\Gamma}_{\mathrm{D}} \gg \overleftarrow{\Gamma}_S, \overleftarrow{\Gamma}_{\mathrm{D}}. \tag{2.37}$$

The above condition shows that we can ignore the expressions (2.32) and (2.36) in calculating the drain current. As a result Eq. (2.13) now can be rewritten as

$$I_{\mathrm{D}} = e \sum_{n=-\infty}^{\infty} p_n \overrightarrow{\Gamma}_S(n) = e \sum_{n=-\infty}^{\infty} p_n \overrightarrow{\Gamma}_{\mathrm{D}}(n). \tag{2.38}$$

where $\overrightarrow{\Gamma}_S(n)$ and $\overrightarrow{\Gamma}_D(n)$ are represented byEq. (2.30) and Eq. (2.34) respectively. And the Eq. (2.16) and Eq. (2.17) now have the new forms

$$\Gamma_{n+1,n} = \overrightarrow{\Gamma}_{\mathrm{S}}(n). \tag{2.39}$$

$$\Gamma_{n-1,n} = \overrightarrow{\Gamma}_{\mathrm{D}}(n). \tag{2.40}$$

Now let solve the master equation (2.15) in steady state ($dp_n/dt = 0$) for just two states "0" and "1" applying the following condition

$$\sum_n p_n = 1. \tag{2.41}$$

In the steady state with two states "0" and "1", Eq. (2.15) becomes

$$0 = \Gamma_{0,1} \cdot p_1 + \Gamma_{0,1} \cdot p_{-1} - (\Gamma_{1,0} + \Gamma_{-1,0}) \cdot p_0. \tag{2.42}$$

From (2.41) and (2.42), the solutions for p_1 and p_0 can be easily obtained

$$p_1 = \frac{\Gamma_{1,0}}{\Gamma_{0,1}} p_0 = \frac{\overrightarrow{\Gamma}_S(0)}{\overrightarrow{\Gamma}_{\mathrm{D}}(1)} p_0, \tag{2.43}$$

with

$$p_0 = \frac{\overrightarrow{\Gamma}_{\mathrm{D}}(1)}{\overrightarrow{\Gamma}_{\mathrm{S}}(0) + \overrightarrow{\Gamma}_{\mathrm{D}}(1)}. \tag{2.44}$$

with just two states "0" and "1", Eq. (2.38) then becomes

$$I_{\mathrm{D}} = e \sum_{n=0}^{1} p_n \overrightarrow{\Gamma}_{\mathrm{S}}(n) = e \left[p_0 \overrightarrow{\Gamma}_{\mathrm{S}}(0) + p_1 \overrightarrow{\Gamma}_{\mathrm{S}}(1) \right]. \tag{2.45}$$

Substituting p_0 from (2.44) into (2.45) we have

$$I_{\mathrm{D}} = e \frac{\overrightarrow{\Gamma}_{S}(0) \left[\overrightarrow{\Gamma}_{D}(1) + \overrightarrow{\Gamma}_{D}(1) \right]}{\overrightarrow{\Gamma}_{S}(0) + \overrightarrow{\Gamma}_{D}(1)}. \tag{2.46}$$

From Eq. (2.30), Eq. (2.34), and Eq. (2.46) the final expression for the drain current of SET can be derived as below

$$I_{\mathrm{D}} = \frac{\left(V_{\mathrm{island}} - \frac{e}{2C_{\Sigma}} \right) \left(V_{\mathrm{DS}} - V_{island} + \frac{e}{2C_{\Sigma}} \right)}{R_{\mathrm{T}} V_{\mathrm{DS}}}. \tag{2.47}$$

here V_{island} is represented via V_{DS} and V_{GS} by the following relationship

$$V_{\mathrm{island}} = \frac{C_{\mathrm{T}}}{C_{\Sigma}} V_{\mathrm{DS}} + \frac{C_{\mathrm{G}}}{C_{\Sigma}} V_{\mathrm{GS}}. \tag{2.48}$$

By taking the derivatives of I_{D} in Eq. (2.47) with respect to V_{DS} and V_{GS}, we obtain the expressions for the conductance and transconductance of the SET respectively [49]

$$g_{\mathrm{d}} = \left. \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{DS}}} \right|_{V_{\mathrm{GS}}=\mathrm{constant}} = \left[\left(\frac{C_{\mathrm{T}}}{C_{\Sigma}} \right) - \left(\frac{C_{\mathrm{T}}}{C_{\Sigma}} \right)^2 + \frac{(2C_G V_{\mathrm{GS}} - e)^2}{4C_{\Sigma}^2 V_{\mathrm{DS}}^2} \right] \frac{1}{R_{\mathrm{T}}}. \tag{2.49}$$

$$g_{\mathrm{m}} = \left. \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}} \right|_{V_{\mathrm{DS}}=\mathrm{constant}} = \left(\frac{C_{\mathrm{G}}}{C_{\Sigma}} \right) \left(\frac{1}{R_{\mathrm{T}}} \right) \left[1 - \frac{2(C_G V_{\mathrm{GS}} + C_T V_{\mathrm{DS}})}{C_{\Sigma} V_{\mathrm{DS}}} \right]. \tag{2.50}$$

The maximum values for g_{d} and g_{m} can be derived as following equations [49]

$$g_{\mathrm{d}}\,(max) = \left[\left(\frac{C_{\mathrm{T}}}{C_{\Sigma}} \right) - \left(\frac{C_{\mathrm{T}}}{C_{\Sigma}} \right)^2 \right] \frac{1}{R_{\mathrm{T}}}. \tag{2.51}$$

$$g_m\,(max) = \left(\frac{C_{\mathrm{G}}}{C_{\Sigma}} \right) \left(\frac{1}{R_{\mathrm{T}}} \right). \tag{2.52}$$

From Eq. (2.51) and Eq. (2.52), even with many assumptions given for simplicity, the dependence of g_{d} and g_{m} on the SET's parameters including tunnel capacitance and resistance (C_{T} and R_{T}) and the gate capacitance (C_G) can be

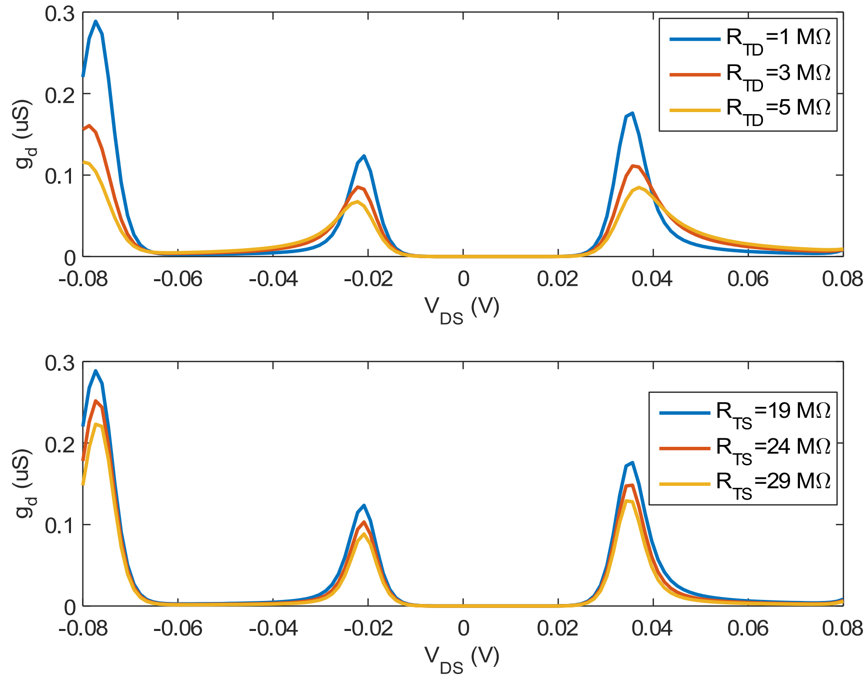


Figure 2.10: Dependence of g_d on tunnel resistances (R_TD and R_TS). It can be seen that g_d increases with the decreasing R_TD and R_TS. Here $V_\mathrm{GS} = 0.02\,\mathrm{V}$.

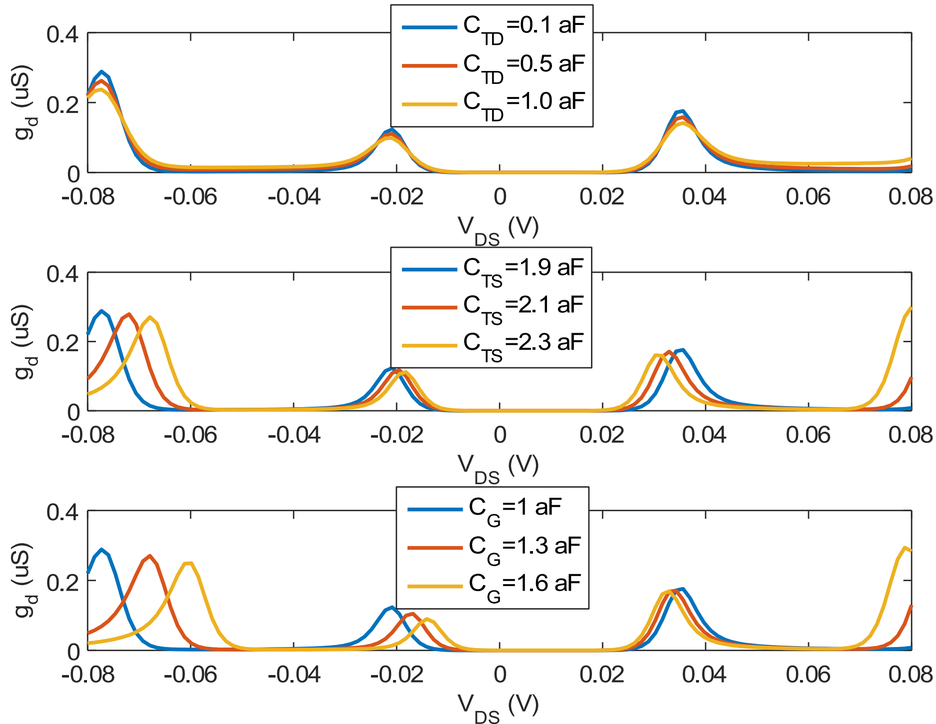


Figure 2.11: Dependence of g_d on tunnel capacitances (C_TD and C_TS) and the gate capacitance (C_G). Although g_d increases with the decreasing C_TD, the effect of C_TS and C_G on g_d is not so clear. Here $V_\mathrm{GS} = 0.02\,V$.

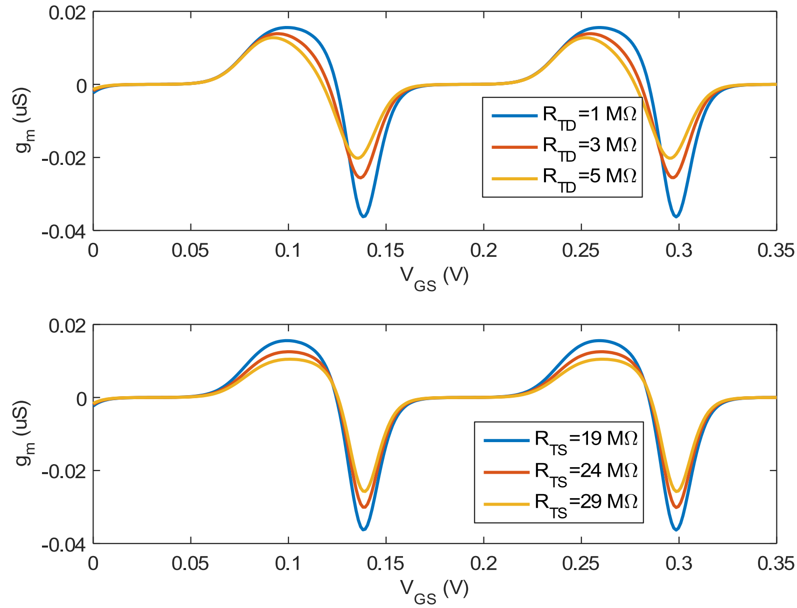


Figure 2.12: Dependence of g_{m} on tunnel resistances (R_{TD} and R_{TS}). It can be seen that g_{m} increases with the decreasing R_{TD} and R_{TS} as the same g_{d}. Here $V_{\mathrm{DS}} = 0.02\,V$

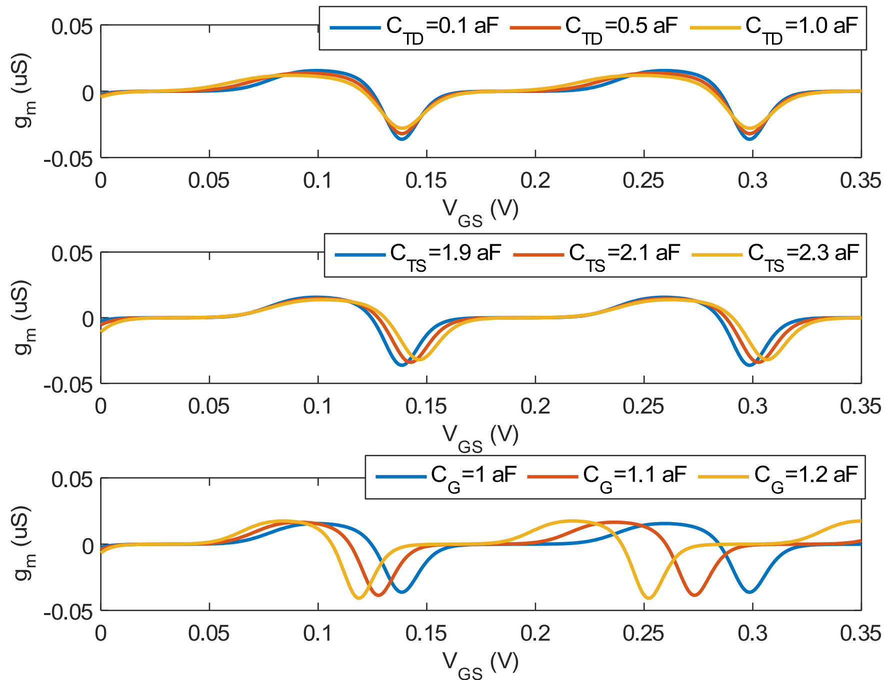


Figure 2.13: Dependence of g_{m} on tunnel capacitances (C_{TD} and C_{TS}) and the gate capacitance (C_{G}). The effect of C_{G}, C_{TS} and C_{G} on g_{m} is also not so clear. Here $V_{\mathrm{GS}} = 0.02\,V$.

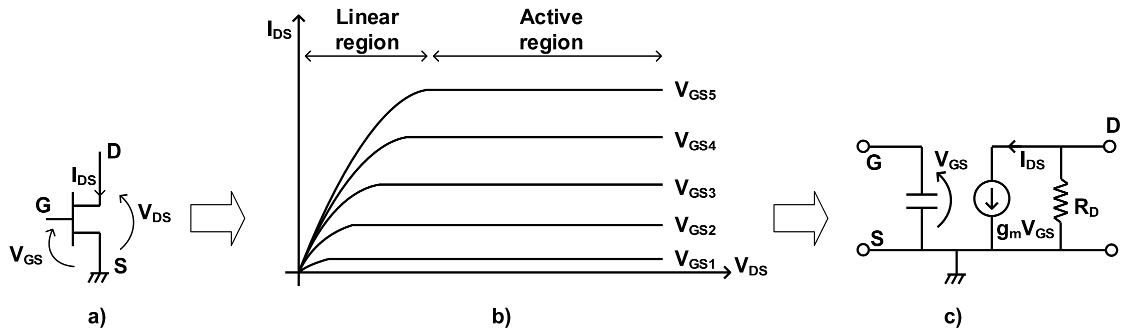


Figure 2.14: The construction of equivalent circuit for MOSFET devices based on their active region of the $I_{\mathrm{DS}}-V_{\mathrm{DS}}$ characteristic. Here: a) MOSFET device, b) The $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic, and c) The simplified equivalent circuit.

roughly evaluated that g_{d} increases with the decreasing R_{T} and C_{G} and with the increasing C_{T} whereas g_{m} increases with the decreasing R_{T} and C_{T} and with the increasing C_{G}. These conclusions somewhat can be confirmed using Inokawa drain current model in Sec. 2.2.2 as shown in Fig. 2.10, Fig. 2.11, Fig. 2.12, and Fig. 2.13.

2.3 Method for power gain enhancement of single-electron transistor (SET)

To date, all researches on the SET have been conducted to study on the aspect of the logic applications of the SET. This means voltage and voltage gain are the main concerns of these researches. However, as discussed before, power gain which is one the most important functionality of active device, that it relates to the current driving capability of the nanoscale devices, has never been studied. Hence in this section, power gain characteristic of the SET is investigated for the first time.

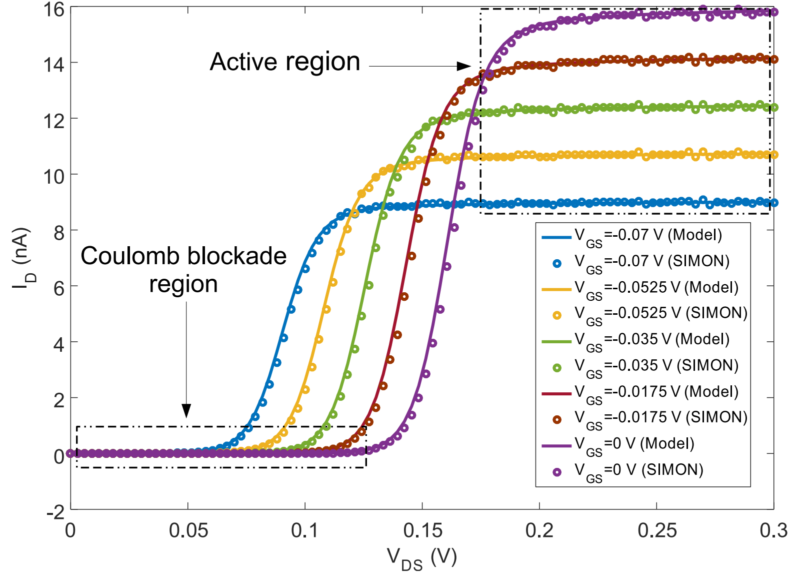


Figure 2.15: New $I_{\mathrm{D}} - V_{\mathrm{DS}}$ characteristic of the SET. The calculated characteristic by Inokawa model coincides well with SIMON simulator. The SET parameters values are $R_{\mathrm{TD}} = 0.1$ MΩ, $R_{\mathrm{TS}} = 10$ MΩ, $C_{\mathrm{G}} = 0.5$ aF, $C_{\mathrm{TD}} = 10^{-3}$ aF, $C_{\mathrm{TS}} = 2 \times 10^{-4}$ aF.

2.3.1 Small-signal equivalent circuit

In this section, a new $I_{\mathrm{D}} - V_{\mathrm{DS}}$ characteristic of the SET which includes both Coulomb blockade region and MOSFET-like active region is reconstructed to investigate the power gain of the SET in active region. As we can see on the Fig. 2.14, the equivalent circuit for conventional MOSFET devices are constructed based on the active region in the $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic where the drain current I_{DS} is dependent only on the variation of the gate-source voltage V_{GS} but not on the drain-source voltage V_{DS}. From Fig. 2.14c, the maximum available power gain (MAG) of the MOSFET devices can be calculated by the following equation

$$\mathrm{MAG} = \frac{R_{\mathrm{DS}}}{R_{\mathrm{GS}}} \frac{g_{\mathrm{m}}^2}{4\omega^2 C_{\mathrm{GS}}^2}. \tag{2.53}$$

where R_{DS} is the real part of the drain impedance Y_{DS} and g_{m} is transconductance. The above equation means we can improve the power gain of the device by enhancing the transconductance value or by tuning the ratio $R_{\mathrm{DS}}/R_{\mathrm{GS}}$ or

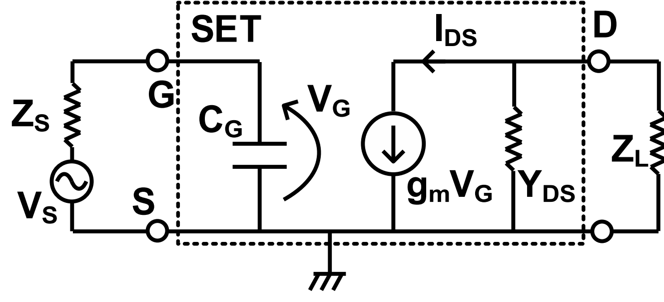


Figure 2.16: Small-signal equivalent circuit of the SET for power gain investigation as a MOSFET-like common-source configuration. $V_{\rm S}$ and $Z_{\rm S}$ denote the source voltage and impedance respectively while $Z_{\rm L}$ represents the load impedance. Here the gate resistance of the SET is not considered.

decreasing $C_{\rm GS}$. Similarly in order to construct an equivalent circuit as well as derive such a Eq. (2.53) for the case of the SET, it is necessary to construct a new novel $I_{\rm DS} - V_{\rm DS}$ characteristic for the SET which includes the active region along with the Coulomb blockade region. Such a characteristic for the SET has been successfully derived for the first time as illustrated on Fig. 2.15. In the figure, we can see that by appropriately tuning the parameters, SET can exhibit both Coulomb blockade and active regions like that of MOSFET devices. This means we can utilize this new characteristic to construct an equivalent circuit for the SET. This equivalent circuit is depicted on Fig. 2.16, the circuit is derived from the active region of the $I_{\rm DS} - V_{\rm DS}$ of SET as shown on the Fig. 2.15. From this equivalent circuit, available power gain formula of SET can be derived as follows

- Available input power from the source is given by:

$$P_i = \frac{|V_{\rm S}|^2}{4Re(Z_{\rm S})}. \tag{2.54}$$

- Maximum output power delivered to the load Z_L is:

$$P_0 = \frac{I_{\rm D}^2 Re(Z_{\rm L})}{4} = g_{\rm m}^2 V_{\rm G}^2 \frac{Re(Z_{\rm L})}{4}. \tag{2.55}$$

- The expression for the MAG is then given as:

$$\text{MAG} = \frac{P_0}{P_i} = g_{\rm m}^2 \frac{Re(Z_{\rm L})Re(Z_{\rm S})}{[(\omega C_{\rm G} Re(Z_{\rm S}))^2 + 1]}. \tag{2.56}$$

where $\omega = 2\pi f$ is the operation frequency. Equation Eq. (2.56) implies that the power gain of the SET can be improved by increasing its transconductance through appropriately tuning the electrical parameters including tunnel capacitances ($C_{\mathrm{TD}}, C_{\mathrm{TS}}$), gate capacitance ($C_{\mathrm{G}}$) and tunnel resistances ($R_{\mathrm{TD}}, R_{\mathrm{TS}}$).

2.3.2 Power gain improvement for SET

From Eq. (2.56), MAG improvement of the SET is firstly investigated under the variation of SET's parameters ($C_{\mathrm{TD}}, C_{\mathrm{TS}}$, C_{G}, and $R_{\mathrm{TD}}, R_{\mathrm{TS}}$). However, the following assumptions must be taken into account:

- Co-tunneling effect is ignored during the investigation, or the source and drain resistances are always larger than the resistance quantum (25.8 $k\Omega$).
- Background charge effect is not dealt with.
- Only two major charging states are considered for drain current model.
- The SET model takes the "orthodox" theory and steady-state master equation method as frameworks for the study.

These assumptions are proposed to simplify the calculation yet still ensuring high accuracy. It is noted that in the calculation low error requirements including $V_{\mathrm{DS}} < e/C_{\Sigma}$ and $T < 0.1e^2/(2k_B C_{\Sigma})$ are always satisfied [50]. The RF signal used for power gain investigation of the SET is supposed to be a sinusoidal signal with an operation frequency of 10 MHz and small amplitude 0.035 V_{p-p}. Here the operation frequency of the SET is chosen at 10 MHz because it is low enough to ignore the parasitic components and close to the recent analyses of RF-SET in MHz bandwidth [41] [42]. The bias point of the SET is always established in the active region, or $V_{\mathrm{DS0}} = 0.25\,V$ and $V_{\mathrm{GS0}} = -0.035\,\mathrm{V}$. The fixed parameters are: $Re(Z_{\mathrm{L}}) = Re(Z_{\mathrm{S}}) = 50\,\Omega$; $T = 82\,\mathrm{K}$; $f = 10\,\mathrm{MHz}$ whereas the device's electrical parameters of the SET including $C_{\mathrm{TD}}, C_{\mathrm{TS}}$, C_{G}, and $R_{\mathrm{TD}}, R_{\mathrm{TS}}$ can take arbitrary values in order that the operation of SET is always kept in the active region. For a verification of this active region when electrical parameters of the SET vary, it is always verified using SIMON 2.0 simulator. Finally the calculated results for power gain improvement investigation are illustrated in Table 2.1. From this table, it can be seen that the power

Table 2.1: Calculated results.

Variation of parameters	G_{p}(dB)
R_{TS} (MΩ) $\downarrow$ 99.3	$\uparrow$ 39.45
R_{TD} (MΩ) $\downarrow$ 0.3	$\uparrow$ 1.55
C_{TD} (F) $\downarrow 4.99 \times 10^{-20}$	$\uparrow$ 0.98
C_{TS} (F) $\downarrow 8.99 \times 10^{-20}$	$\uparrow$ 1.26
C_{G} (F) $\uparrow 15 \times 10^{-20}$	$\uparrow$ 0.48

gain of the SET can be improved the most by tuning the source resistance R_{TS} compared to other parameters. In details, the power gain of the SET is enhanced by a significant amount of 39.45 dB if R_{TS} is decreased by 99.3 MΩ whereas the improved power gain when other parameters including R_{TD}, C_{TD}, C_{TS}, and C_{G} vary are just about 1.55 dB, 0.98 dB, 1.26 dB, and 0.48 dB respectively. It is noted that compared to the key parameters, says R_{TS}, other parameters values are changed within a small range because of two reasons. The first one is they have just a slight impact on power gain improvement and another important reason is beyond that range, the SET cannot be kept in the active region.

2.3.3 Frequency response of the SET

To investigate the frequency characteristic of our present SET model, it first needs discussing about the two key points. The first one is cutoff frequency of the SET since this frequency contributes to the intrinsic operation speed or the time between two successive tunneling events and the second one is tunneling rate which relates to the duration time of a tunneling event. In the case of our present SET model, SET with a set of electrical parameters $R_{\mathrm{TD}} = 0.1\,\mathrm{M\Omega}$, $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$, $C_{\mathrm{G}} = 0.5\,\mathrm{aF}$ exhibits a

maximum cutoff frequency of

$$f_c = \frac{1}{(2\pi R_{TD} C_{TD})} \simeq 1.6 \times 10^{16}\,\text{Hz}. \tag{2.57}$$

Whereas, if the SET has the following set of parameters: $R_{TD} = 0.1\,\text{M}\Omega$, $R_{TS} = 0.7\,\text{M}\Omega$, $C_{TD} = 10^{-3}\,aF$, $C_{TS} = 2 \times 10^{-4}\,\text{aF}$, $C_G = 0.5\,\text{aF}$ exhibits the maximum drain current of 0.16 μA leading to the maximum tunneling rate of

$$\Gamma_{max} = \frac{I_D}{e} \simeq 1\,\text{THz}. \tag{2.58}$$

where e is the elementary charge. This shows that in the operation frequency range from 1 to 10^4 THz, there exists SETs which exhibit the time interval between successive tunneling events smaller than the duration time of a single tunneling event. This causes the co-tunneling and undesired effect. Hence, in order that all SETs proposed can operate normally, operation frequency of the SET is limited to THz regime. Now frequency response of the SET is investigated using Eq. (2.56), or in other words, the plot of MAG of the SET vs the operation frequency. This characteristic is illustrated on Fig. 2.17 with operation frequency up to 1 THz. It is clearly seen on the figure that power gain of the SET shows the most improvement under the change of the source resistance R_{TS} compared to the other parameters as concluded before. Another important finding can be seen from the figure is the power gain remains constant within the frequency range up to 1 THz. This reveals the fact that our proposed SET model can still operate at extremely high frequency in THz regime and today's technology has been developed up to THz regime [59] [60]. In addition, the figure also shows that output power of the SET is very small due to its intrinsic extremely small transconductance. So far, we have used Eq. (2.56) to study power gain improvement and frequency characteristic of the SET under the variation of its electrical parameters and it was found that the source resistance is the key factor for power gain improvement. However, studying such features with considering the effect of just electrical parameters is not significant enough since relationship between these electrical parameters and the real device structure, or the physical parameters such as junction thickness, area, and so on can not be revealed. The following section goes

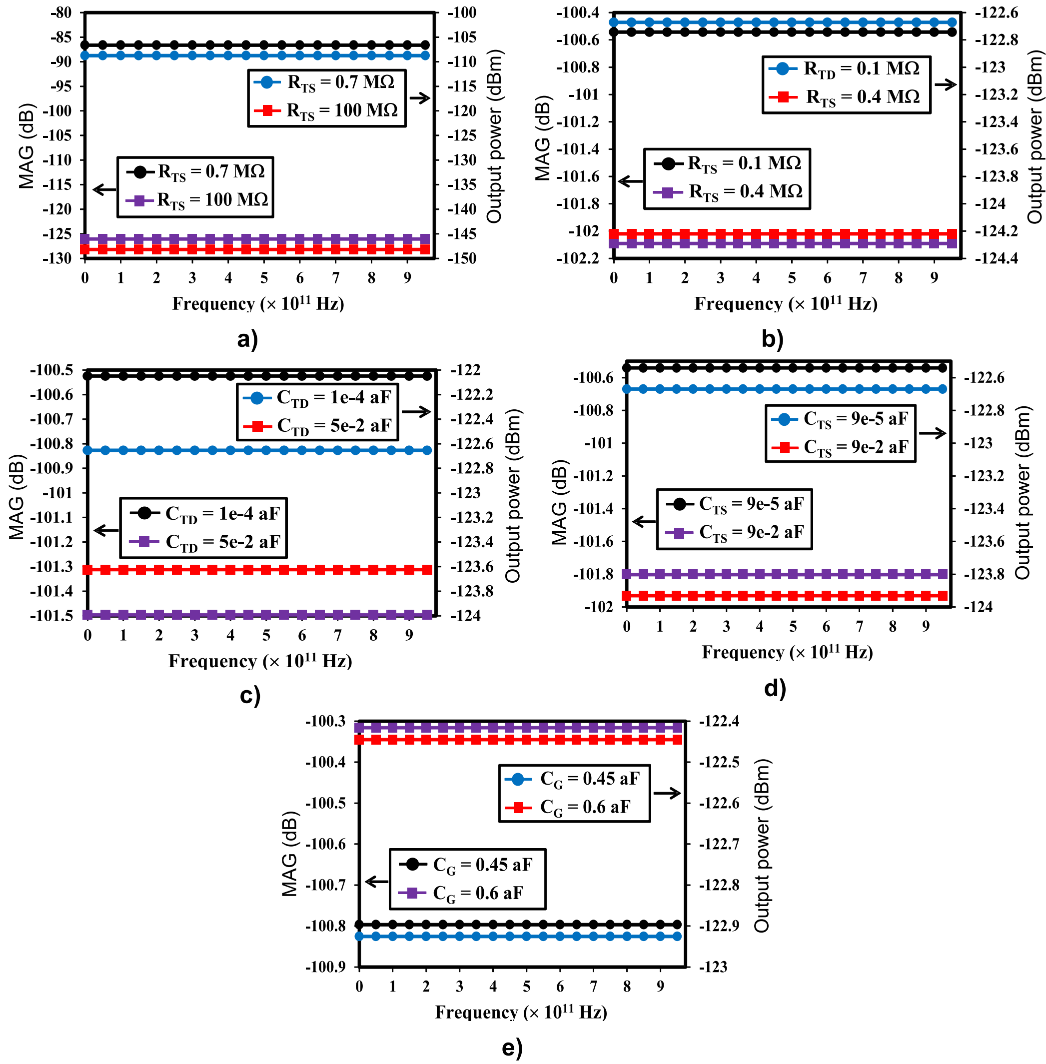


Figure 2.17: a) and b): Frequency characteristic with respect to the variation of the source and drain resistances (R_{TS} and R_{TD}); c), d), and e): frequency characteristic with respect to the variation of the drain, source and gate capacitances (C_{TD}, C_{TS}, and C_{G}) respectively. The SET parameters: a) $R_{\mathrm{TD}} = 0.1\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$, $C_{\mathrm{G}} = 0.5\,\mathrm{aF}$; b) $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$, $C_{\mathrm{G}} = 0.5\,\mathrm{aF}$; c) $R_{\mathrm{TD}} = 0.1\,\mathrm{M\Omega}$, $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$, $C_{\mathrm{G}} = 0.5\,\mathrm{aF}$; d) $R_{\mathrm{TD}} = 0.1\,M\Omega$, $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_G = 0.5\,\mathrm{aF}$; e) $R_{\mathrm{TD}} = 0.1\,\mathrm{M\Omega}$, $R_{\mathrm{TS}} = 5\,\mathrm{M\Omega}$, $C_{\mathrm{TD}} = 10^{-3}\,\mathrm{aF}$, $C_{\mathrm{TS}} = 2 \times 10^{-4}\,\mathrm{aF}$.

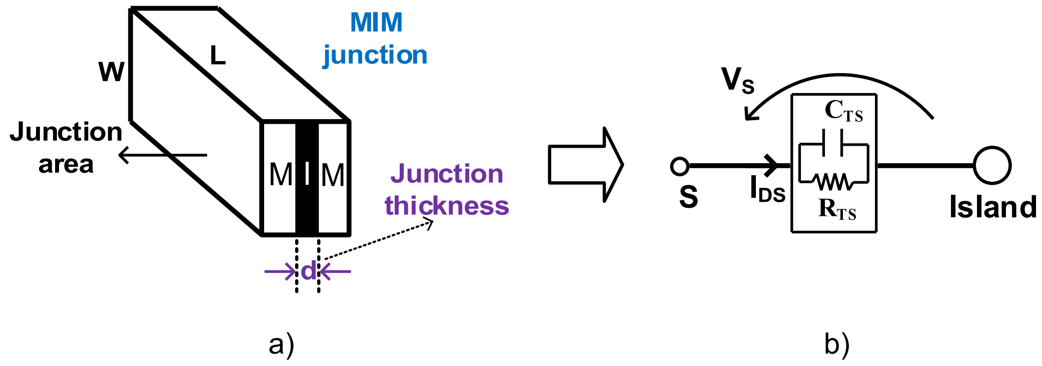


Figure 2.18: Source junction thickness of the SET: a) Draw of the structure and b) The equivalent circuit of the junction.

further by pointing out the relationship between the power gain improvement and the physical parameters of the tunnel junction of the SET.

2.3.4 Influence of the source junction thickness on power gain improvement

Although some articles reported on the analytical model of SET [57] [61] [62], most of them studied SET at the circuit level but not in the device structure level. Contrary to these researches, our SET model is studied not only in the circuit level but also in the device structure level. The purpose of this section is to investigate the dependence of SET power gain on its source junction thickness as the key factor for the power gain improvement. The method procedure is as follows:

- Firstly finding the physical parameters including junction material, junction dielectric, area, etc. of a fabricated SET.
- After that using a proper tunneling current model for a metal-insulator-metal (MIM) junction.
- Thirdly obtaining each set of current and voltage values of the source junction which corresponds to each set of source resistance and capacitance values from the SIMON simulator.
- Lastly substituting the obtained physical parameters and set of current and

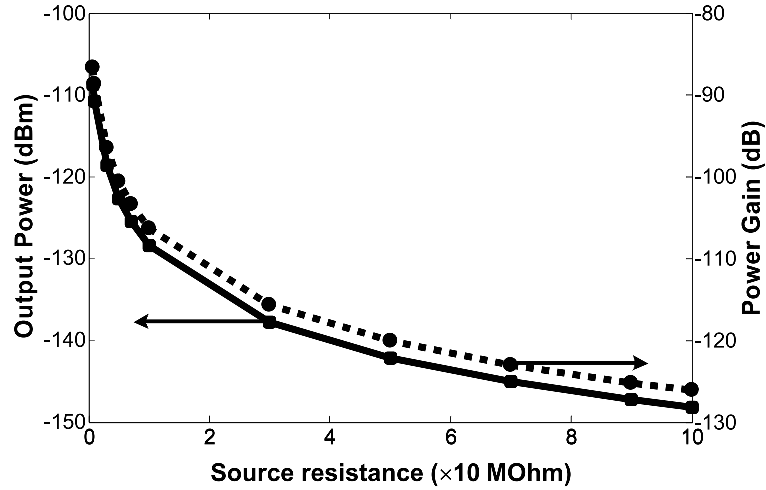


Figure 2.19: The dependence of SET output power and power gain on the source resistance. The SET parameters: $R_{\mathrm{TD}} = 0.1$ MΩ, $C_{\mathrm{TD}} = 10^{-3}$ aF, $C_{\mathrm{TS}} = 2 \times 10^{-4}$ aF, $C_{\mathrm{G}} = 0.5$ aF.

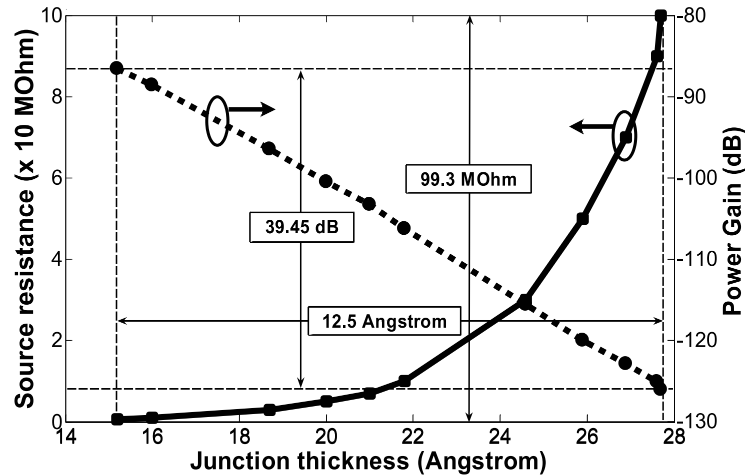


Figure 2.20: The dependence of SET power gain on the source junction thickness.

voltage into the tunnel current equation and solving this equation to find out the value for the source thickness.

The SET physical junction parameters for the first step are given in Table 2.2 [63]. We can image that the source junction made up with MIM material as depicted on Fig. 2.18. It can be seen on the Fig. 2.18b that in accordance with

Table 2.2: Physical parameters of the source tunnel junction.

Junction material	Ti
Junction dielectric	TiO_x
Junction area (nm^2)	10×2
Ti/TiO_x barrier height (eV)	0.35
Effective electron mass in Ti/TiO_x (m)	0.4
Ti/TiO_x dielectric constant	3.5

each set of (R_{TS}, C_{TS}), there is a corresponding set of current and voltage on the junction (I_{DS}, V_S). The following formula describes the zero-temperature tunnel current through an MIM junction which was proposed by Gibson [64]:

$$\begin{aligned} J(V) = \frac{6.16 \times 10^{10}}{s^2} \Bigg\{ & \left[\varphi_0 - \frac{eV}{2} + \frac{2.93}{s} \left(\frac{m}{m^*}\right)^{1/2} \left(\varphi_0 - \frac{eV}{2}\right)^{1/2} + \frac{2.86}{s^2} \left(\frac{m}{m^*}\right) \right] \\ & \times \left\{ \exp \left[-1.025 s \left(\frac{m^*}{m}\right)^{1/2} \left(\varphi_0 - \frac{eV}{2}\right)^{1/2} \right] \right\} \\ & - \left[\varphi_0 + \frac{eV}{2} + \frac{2.93}{s} \left(\frac{m}{m^*}\right)^{1/2} \left(\varphi_0 + \frac{eV}{2}\right)^{1/2} + \frac{2.86}{s^2} \left(\frac{m}{m^*}\right) \right] \\ & \times \left(\exp \left[-1.025 s \left(\frac{m^*}{m}\right)^{1/2} \left(\varphi_0 + \frac{eV}{2}\right)^{1/2} \right] \right) \Bigg\}. \end{aligned} \quad (2.59)$$

where V is a low bias voltage whereas s and φ_0 are the barrier thickness and height, respectively. It is noted here that $eV < \varphi_0$. Then the temperature-dependent current model in [63] is utilized as below:

$$J(V, T) = J(V, 0) \left[\frac{\pi BkT}{\sin(\pi BkT)} \right], \quad (2.60)$$

where

$$B = \frac{A}{2\varphi_0^{1/2}}; A = \left(\frac{4\pi S_{eff}}{h}\right) (2m^*)^{1/2}, \quad (2.61a)$$

$$S_{eff} = \frac{s(\alpha + \varepsilon_r/\gamma)}{(e/\varphi_0 + \varepsilon_r/\gamma)}; \alpha = 0.2V^{-1}; \gamma = 3.5V. \quad (2.61b)$$

here $J(V, 0)$, m, m^*, and ε_r are the zero-temperature current density, free electron mass, effective electron mass in the material and the relative dielectric

constant, respectively. Now we can see the dependence of the power gain and output power on the source resistance as illustrated on Fig. 2.19. This figure will be converted in to another figure in which the power gain of the SET is plotted vs the source junction thickness. This purpose is accomplished if it is successfully extracted the set of current and voltage on the junction ($I_{\rm DS}$, $V_{\rm S}$) according to each respective values of the junction resistance and capacitance ($R_{\rm TS}$, $C_{\rm TS}$) as shown on the Fig. 2.19. To to so, the SIMON 2.0 simulator is used for a precise extraction. In the SIMON simulator, the SET model and the simulation time step was optimized to ensure the simulation accuracy. After extracting these current and voltage values, these values along with the other physical parameters given in the Table Fig. 2.2 are substituted into Eq. (2.59), then solving this equation to find out the source thickness. Here, it is assumed that the junction thickness only affects tunnel resistance but not tunnel capacitance. This is a reasonable assumption since the tunnel capacitance is mainly affected by the island size [65]. Furthermore, for simplicity in calculation yet high accuracy, only low electrical field and low temperature current model of Eq. (2.59) and Eq. (2.60) are considered. Finally, the dependence of the power gain of SET on the source thickness as shown in Fig. 2.20 where it can be seen power gain of the SET is improved significantly by 39.45 dB if its source resistance is reduced by 99.3 MΩ which is equivalent to the reduction of 12.5 Å (1.25 nm) in the junction thickness.

2.4 Summary

In this chapter, by introducing a small-signal equivalent circuit, SETs power gain and output power, the crucial microwave features of active devices has been studied for the first time. It was found that by using the method of current transfer or transconductance improvement, SET's power gain can be enhanced by 39.45 dB if its source junction thickness is reduced by 1.25 nm. Moreover, the proposed SET was found to be suitable for using in applications at very high frequencies up to THz regime since its power gain remains almost

unchanged till THz region. In addition, it is important to note that although power gain of SET is very small compared to that of conventional devices, its improvement still plays a key role in order to increase the output current drive capability for not only SET but other quantum devices. Therefore, my present finding in optimizing SET device structure for power gain improvement contributes a very important role for a new promising research field of SET for its potential application in the future.

Chapter 3

Power gain performance enhancement of independently biased InGaP/GaAs heterojunction bipolar transistor (HBT) cascode chip

3.1 Introduction

In the last chapter, power gain improvement for the single-electron transistor (SET) has been investigated by using the method of current transfer method through the improvement of the SET's transconductance. This chapter, on the other hand, utilizes alternative power gain improvement method as mentioned in Chapter 1, the resistance transfer method, to investigate the power gain performance of a new proposed cascode configuration, that is so-called the independently biased configuration. As mentioned earlier in the Chapter 1 that a conventional cascode configuration (Conventional CC) is formed by connecting in cascade a first-stage common-emitter (CE) or common-source (CS) transistor and a second-stage common-base (CB) or common-gate (CG) transistor. This conventional configuration has been shown to have many ad-

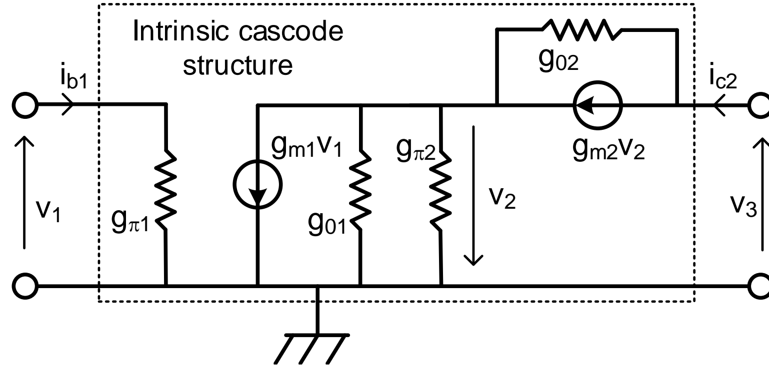


Figure 3.1: Simplified hybrid π model small-signal equivalent circuit of the cascode configuration.

vantages including high isolation, wide bandwidth, and capable of operating at high frequency range [66] [67] [68]. Moreover although there are several articles reporting on its superior RF characteristics [69] - [72], it encounters an inherent weakness of an unstable potential or a floating point between two transistors, this mechanism will be explained in the next section. This weakness makes it impossible to independently establish the bias condition for each transistor, thus the degree of freedom in bias setting of the Conventional CC becomes very low. To overcome this inherent weakness, a new novel cascode configuration, namely independently biased cascode configuration (Independently Biased CC) is proposed. The Independently Biased CC is realized by adding an additional bias terminal to the floating point of the Conventional CC [73] [74], as a result the bias condition of the Independently Biased CC can be established individually for each transistor of the configuration. This means the degree of freedom in bias setting becomes increased. In contrast to the Conventional CC, thanks to this technique, output resistance of the Independently Biased CC can be controlled. This is understood by considering Fig. 3.1 which shows the simplified small-signal equivalent circuit for the cascode configuration. From this figure, output resistance of the cascode configuration is derived as below:

$$r_0 \approx \frac{1}{g_{02}}\left(1+\frac{g_{\mathrm{m}2}}{g_{\pi 2}}\right) = (\beta+1)\frac{1}{g_{02}}. \tag{3.1}$$

where

$$g_{02} = \frac{I_{c2}}{V_A}. \tag{3.2}$$

here r_0 is the output resistance while g_{02}, g_{m2} and $g_{\pi 2}$ are the second stage transistor's conductance values; I_{c2} and V_A are the second stage collector bias voltage and Early voltage, respectively. The above equation means output resistance of the cascode configuration is only dependent on the second stage collector bias current I_{c2}. While conventional configuration is not able to control this bias parameters since it can not set bias condition independently for each transistor, the independently biased configuration, on the other hand, can control this bias parameter (or the output resistance) thanks to the independently biased feature, consequently its power gain is increased accordingly when compared with the conventional one. In addition to the power gain enhancement, the Independently Biased CC can also deliver high power efficiency yet ensuring high linearity [75] compared to the Conventional CC. This chapter investigates and validates the above discussion on the power gain improvement of the Independently Biased CC in comparison to that of the Conventional CC using the resistance transfer method by considering its bias conditions at an operation frequency of 1.9 GHz.

3.2 DC power analysis

This section investigates the DC power distribution of both the Conventional CC and Independently Biased CC to give a raw prediction on if power gain of the Independently Biased CC is better than that of the Conventional CC. This step is necessary because power gain and DC power supply have a direct relationship, thus that is the reason why DC power distribution needs to be investigated before the power gain investigation. Firstly, let's look at the Fig. 3.2 where shows the constructions of the Conventional CC and Independently Biased CC. We can see the floating point or stuck potential between the CE and CB transistors of the Conventional CC in Fig. 3.2a whereas in the Independently Biased CC it is replaced with an additional bias terminal

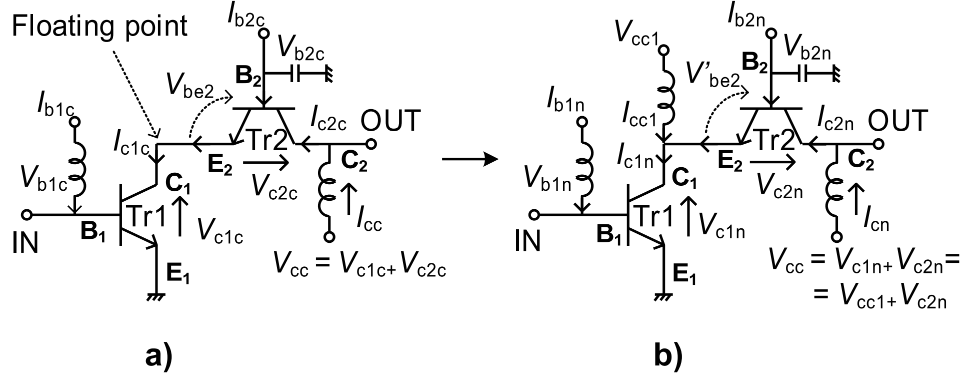


Figure 3.2: a) Conventional cascode configuration (Conventional CC) and b) Independently biased cascode configuration (Independently Biased CC). Here I_{b1c} and I_{b2c} represent the base bias currents of the CE and CB of the Conventional CC; I_{b1n} and I_{b2n} denote the base bias currents of the CE and CB of the Independently Biased CC, respectively. Furthermore, V_{c1c} and V_{c2c} are the collector bias voltages of the CE and CB transistors of the Conventional CC, respectively; V_{c1n} and V_{c2n} are the collector bias voltages of the CE and CB transistors of the Independently Biased CC, respectively. I_{c1c}, I_{c2c} and I_{c1n}, I_{c2n} represent the DC collector currents for the CE and CB transistors of the Conventional CC and Independently Biased CC respectively whereas V_{c1c}, V_{c2c} and V_{c1n}, V_{c2n} represent their DC collector voltages.

as illustrated on Fig. 3.2b. This technique makes the bias degree of freedom of the Independently Biased CC higher than that of the Conventional CC. To make a fair comparison between the two configurations, it is necessary to follow below assumptions:

- Two transistors of the Conventional CC and Independently Biased CC are biased under the same base bias currents for ordinary operation since they have the same size or we have: $I_{\mathrm{b1c}} = I_{\mathrm{b2c}} = I_{\mathrm{b1n}} = I_{\mathrm{b2n}} = I_{\mathrm{b}}$.
- The total collector voltage or the CB transistor's collector voltage V_{cc} is kept the same for both the Conventional CC and Independently Biased CC during the comparison or: $V_{\mathrm{cc}} = V_{\mathrm{c1c}} + V_{\mathrm{c2c}} = V_{\mathrm{c1n}} + V_{\mathrm{c2n}}$.

According to the Fig. 3.2, the expressions of DC power supply for the Con-

ventional CC and Independently Biased CC have the following forms

$$\begin{aligned} P_{\mathrm{DCc}} &= I_{\mathrm{b1c}}V_{\mathrm{b1c}} + I_{\mathrm{b2c}}V_{\mathrm{b2c}} + I_{\mathrm{c2c}}V_{\mathrm{cc}} \\ &= I_{\mathrm{b1c}}V_{\mathrm{b1c}} + I_{\mathrm{b2c}}(V_{\mathrm{b2e}} + V_{\mathrm{c1c}}) + I_{\mathrm{c2c}}(V_{\mathrm{c1c}} + V_{\mathrm{c2c}}). \end{aligned} \tag{3.3}$$

$$\begin{aligned} P_{\mathrm{DCn}} &= I_{\mathrm{b1n}}V_{\mathrm{b1n}} + I_{\mathrm{b2n}}V_{\mathrm{b2n}} + I_{\mathrm{c2n}}V_{\mathrm{cc}} + I_{\mathrm{cc1}}V_{\mathrm{cc1}} \\ &= I_{\mathrm{b1n}}V_{\mathrm{b1n}} + I_{\mathrm{b2n}}(V'_{\mathrm{b2e}} + V_{\mathrm{c1c}}) + I_{\mathrm{c2n}}(V_{\mathrm{c1n}} + V_{\mathrm{c2n}}) + I_{\mathrm{cc1}}V_{\mathrm{cc1}}. \end{aligned} \tag{3.4}$$

V_{b1c} and V_{b2c} denote the base DC voltages of the CE and CB of the Conventional CC, respectively. I_{cc1} and V_{cc1} represent the mid-point current and voltage, respectively whereas V_{be2} and V'_{be2} denote the base-emitter DC voltages of the CB transistor of the Conventional CC and Independently Biased CC.

The currents condition at the floating point according to the Kirchhoffs law gives

$$I_{\mathrm{c1c}} = I_{\mathrm{c2c}} + I_{\mathrm{b2}} \approx I_{\mathrm{c2c}}. \tag{3.5}$$

$$I_{\mathrm{c1n}} = I_{\mathrm{c2n}} + I_{\mathrm{b2n}} + I_{\mathrm{cc1}} \approx I_{\mathrm{c2n}} + I_{\mathrm{cc1}}. \tag{3.6}$$

The above approximation can be used based on the fact that in the Conventional CC the base current is much smaller compared to the collector current. Taking the subtraction of the P_{DCn} and the P_{DCc} we have

$$\Delta P_{\mathrm{DC}} = P_{\mathrm{DCn}} - P_{\mathrm{DCc}} \approx V_{\mathrm{cc}}(I_{\mathrm{c2n}} - I_{\mathrm{c2c}}) + I_{\mathrm{cc1}}V_{\mathrm{cc1}}. \tag{3.7}$$

So far we have mentioned that in the Conventional CC, collector current flows through the CE and CB transistors have the same value, consequently the mid-point current I_{cc1} becomes much smaller than I_{c2n} and I_{c2c}. Therefore the Eq. (3.7) then can be reduced to

$$\Delta P_{\mathrm{DC}} \approx V_{\mathrm{cc}}(I_{\mathrm{c2n}} - I_{\mathrm{c2c}}). \tag{3.8}$$

The above formula means the difference in DC power supply between the Conventional CC and Independently Biased CC are mainly contributed by the difference in their CB transistor collector currents. This leads to that fact that under the same bias condition, the Independently Biased CC can deliver higher

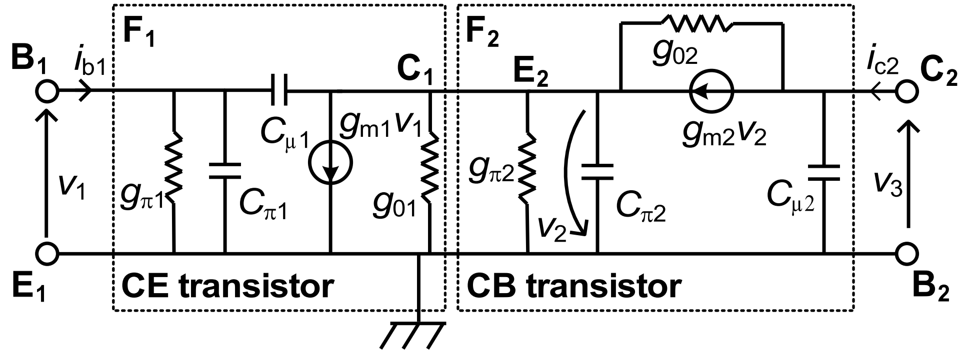


Figure 3.3: Simplified small-signal equivalent circuit for the Conventional CC and Independently Biased CC as a two-port network of a cascode connection of CE and CB transistors. Here g_{m}, g_0, and g_π represent the conductances at a specific bias point; C_μ and C_π denote the base-collector and base-emitter capacitances, respectively; i_{b1} and i_{c2} are the AC currents of the CE and CB transistors, respectively whereas v_1 and v_2 represent the AC base-emitter voltages of the CE and CB transistors, and v_3 is the AC CB transistor collector voltage.

DC power supply than that of the Conventional CC if its I_{c2n} is adjusted to be higher than I_{c2c} of the Conventional CC. It is also expected that this will result in the higher power gain of the Independently Biased CC compared to that of the Conventional CC. This expectation will be investigated in the next section.

3.3 Power gain investigation

In this section, it is pointed out that the difference in CB transistor collector currents $I_{\mathrm{c2n}} - I_{\mathrm{c2c}}$ between the Conventional CC and Independently Biased CC is also the key factor affecting the difference in their power gain. To investigate the power gain of the Conventional CC and Independently Biased CC, it first needs to derive the power gain expressions based on their simplified small-signal equivalent circuit as a two-port network which is given on Fig. 3.3. For

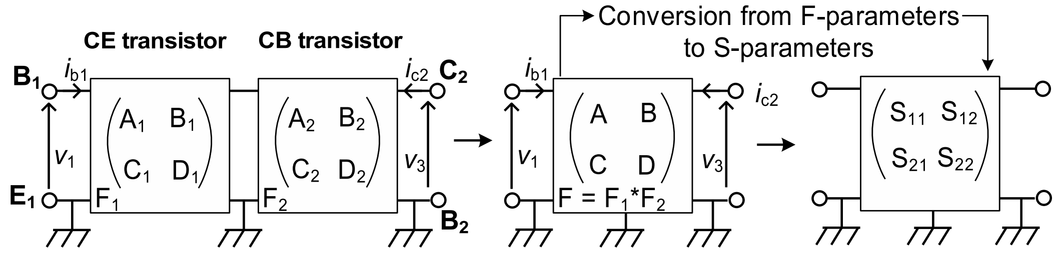


Figure 3.4: Conventional CC and Independently Biased CC as a two-port network which is formed by the combination in cascade of two two-port networks, the CE and CB transistors. S-parameters of the Conventional CC and Independently Biased CC are derived by converting their F-parameters.

small-signal power gain analysis of two-port networks, the most common power gain definitions used are maximum available gain (MAG) and maximum stable gain (MSG) [76] [77] [78]. Now we will derive the MAG/MSG expressions of the Conventional CC and Independently Biased CC and compare their power gain from the derived MAG/MSG.

MAG/MSG of a two-port network is computed from its S-parameters by the following formulas

$$\text{MAG} = (K - \sqrt{K^2 - 1}) \left| \frac{S_{21}}{S_{12}} \right|. \tag{3.9}$$

if $K > 1$, otherwise if $K < 1$ power gain is expressed through MSG as below formula

$$\text{MSG} = \left| \frac{S_{21}}{S_{12}} \right|. \tag{3.10}$$

where K is Rollet stability factor and it is given as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|}. \tag{3.11}$$

Here,

$$S = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \tag{3.12}$$

are the S-parameters of the Conventional CC and Independently Biased CC as a cascade combination of two two-port networks, CE and CB transistors.

Since in analysis of two-port networks in cascade connection the most common way is using the F-parameters, the S-parameters of the cascode configurations is derived by transforming their the F-parameters as illustrated on Fig. 3.4. The transformation is conducted through the following relationship

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D}. \tag{3.13}$$

$$S_{12} = \frac{2(AD - BC)}{A + B/Z_0 + CZ_0 + D}. \tag{3.14}$$

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D}. \tag{3.15}$$

$$S_{22} = \frac{-A + B/Z_0 - CZ_0 + D}{A + B/Z_0 + CZ_0 + D}. \tag{3.16}$$

where Z_0 is reference impedance whereas A, B, C, D are the components of the final F-parameters of the cascode configuration which are formed from two component F-parameters, F_1 and F_2, or

$$F = \begin{pmatrix} A & B \\ C & D \end{pmatrix} = F_1 \times F_2 = \begin{pmatrix} A_1 & B_1 \\ C_1 & D_1 \end{pmatrix} \begin{pmatrix} A_2 & B_2 \\ C_2 & D_2 \end{pmatrix} \tag{3.17}$$

here A_1, B_1, C_1, D_1 and A_2, B_2, C_2, D_2 can be calculated from Fig. 3.3 and they are given as below

$$\begin{pmatrix} A_1 & B_1 \\ C_1 & D_1 \end{pmatrix} = \begin{pmatrix} \frac{-(sC_{\mu 1})^2 + sC_{\mu 1} g_{\mathrm{m1}}}{g_{\mathrm{m1}}} & \frac{1}{sC_{\mu 1}} \\ \frac{-s^2 C_{\mu 1} g_{\mathrm{m1}} + sC_{\mu 1} g_{\pi 1} g_{\mathrm{m1}}}{g_{\mathrm{m1}}^2} & \frac{g_{\pi 1} + sC_{\pi 1}}{sC_{\mu 1}} \end{pmatrix} \tag{3.18}$$

$$\begin{pmatrix} A_2 & B_2 \\ C_2 & D_2 \end{pmatrix} = \begin{pmatrix} \frac{g_{02} + sC_{\mu 2}}{g_{\mathrm{m2}}} & \frac{1}{g_{\mathrm{m2}}} \\ \frac{s^2 C_{\mu 2} C_{\pi 2} - sC_{\mu 2} g_{\mathrm{m2}}}{g_{\mathrm{m2}}} & \frac{-g_{\mathrm{m2}} + sC_{\pi 2}}{g_{\mathrm{m2}}} \end{pmatrix} \tag{3.19}$$

with $s = j\omega$ the complex angular frequency and ω, the operation frequency. g_{m}, g_0, and g_π in (3.18) and (3.19) can be calculated using below typical equations of a bipolar junction transistor (BJT) [79] [80] [81]

$$I_{\mathrm{c}} = I_{\mathrm{S}} \exp\left(\frac{V_{\mathrm{be}}}{V_{\mathrm{T}}}\right)\left(1 + \frac{V_{\mathrm{ce}}}{V_{\mathrm{A}}}\right) \rightarrow g_0 = \frac{\partial i_{\mathrm{c}}}{\partial v_{\mathrm{ce}}} \approx \frac{I_{\mathrm{c}}}{V_{\mathrm{A}}}. \tag{3.20}$$

$$I_{\mathrm{c}} = I_{\mathrm{S}} \exp\left(\frac{V_{\mathrm{be}}}{V_{\mathrm{T}}}\right)\left(1 + \frac{V_{\mathrm{ce}}}{V_{\mathrm{A}}}\right) \rightarrow g_m = \frac{\partial i_{\mathrm{c}}}{\partial v_{\mathrm{be}}} \approx \frac{I_{\mathrm{c}}}{V_{\mathrm{T}}}. \tag{3.21}$$

$$I_{\mathrm{b}} = I_{\mathrm{B0}} \exp\left(\frac{V_{\mathrm{be}}}{V_{\mathrm{T}}}\right) \rightarrow g_\pi = \frac{\partial i_{\mathrm{b}}}{\partial v_{\mathrm{be}}} \approx \frac{I_{\mathrm{b}}}{V_{\mathrm{T}}}. \tag{3.22}$$

here

$$V_{\mathrm{T}} = \frac{kT}{q}; I_{\mathrm{c}} = \beta I_{\mathrm{b}}. \tag{3.23}$$

with β the beta current gain of the BJT. V_{T} and V_{A} represent the thermal and Early voltages, respectively whereas V_{be} and V_{ce} denote the base-emitter and collector-emitter DC voltages; v_{be} and v_{ce} are their AC values; I_{b} and I_{c} represent the base and collector DC currents while i_{be} and i_{ce} are their AC values, respectively. I_{S} and I_{B0} are the base and collector saturation currents. $k = 1.38 \times 10^{23}\,\mathrm{m}^2.\mathrm{kg.s}^2.\mathrm{K}^1$ is the Boltzmann constant and $q = 1.6 \times 10^{19}\,\mathrm{C}$ is the elementary charge.

Since it is difficult to derive explicit expressions of MSG/MAG in (3.9) and (3.10), we should find an alternative way by using a set of typical sample parameters for an HBT: $\beta = 50$; $V_{\mathrm{A}} = 250\,\mathrm{V}$; $V_{\mathrm{T}} = 0.026\,\mathrm{V}$; $I_{\mathrm{S}} = 10^{15}\,\mathrm{A}$; $Z_0 = 50\,\Omega$; $f = 1.9\,\mathrm{GHz}$; $C_{\mu 1} = 1\,\mathrm{pF}$; $C_{\mu 2} = 0.01\,\mathrm{pF}$; $C_{\pi 1} = C_{\pi 2} = 5.95\,\mathrm{pF}$. Here $\beta = 50$ is a reasonable value for GaAs-based HBT [82] [83] [84] [85]. In addition, the Early voltage is chosen at a fixed value $V_{\mathrm{A}} = 250\,\mathrm{V}$ although complicated model for the Early voltage can be found in [86] [87] [88]. Now substituting these parameters into Eq. (3.10) with taking into account Eq. (3.18)-Eq. (3.23), we have a new form of MSG as follows

$$\mathrm{MSG} = \frac{I_{\mathrm{c2}}}{\sqrt{a - bI_{\mathrm{c2}}^2 + cI_{\mathrm{c2}}^4 + dI_{\mathrm{c2}}^6}}. \tag{3.24}$$

where $a = 6.94 \times 10^{-16}\mathrm{A}^2$, $b = 2.85 \times 10^{-10}$, $c = 3.09 \times 10^{-5}\mathrm{A}^{-2}$, and $d = 3.47\mathrm{A}^{-4}$.

Eq. (3.24) indicates that MSG of the Conventional CC and Independently Biased CC is only dependent on I_{c2}, as a result the difference in MSG between them is also dependent only on the difference in I_{c2} or the subtraction $I_{\mathrm{c2n}} - I_{\mathrm{c2c}}$. Since the expression for MAG using Eq. (3.23) and the sample parameters is still complicated, we use a graphical technique to analyze the dependence of MAG on I_{c2}. This method is described on Fig. 3.5 where we can see that when the base bias current I_{b} varies from 0.1 mA to 0.3 mA, the angles α_i [$\alpha_i = \arctan(\Delta\mathrm{MAG}_i/\Delta I_{\mathrm{c2}i})$ where $\Delta\mathrm{MAG}_i = \mathrm{MAG}_{\mathrm{n}i} - \mathrm{MAG}_{\mathrm{c}i}$ and $\Delta I_{\mathrm{c2}i} =$

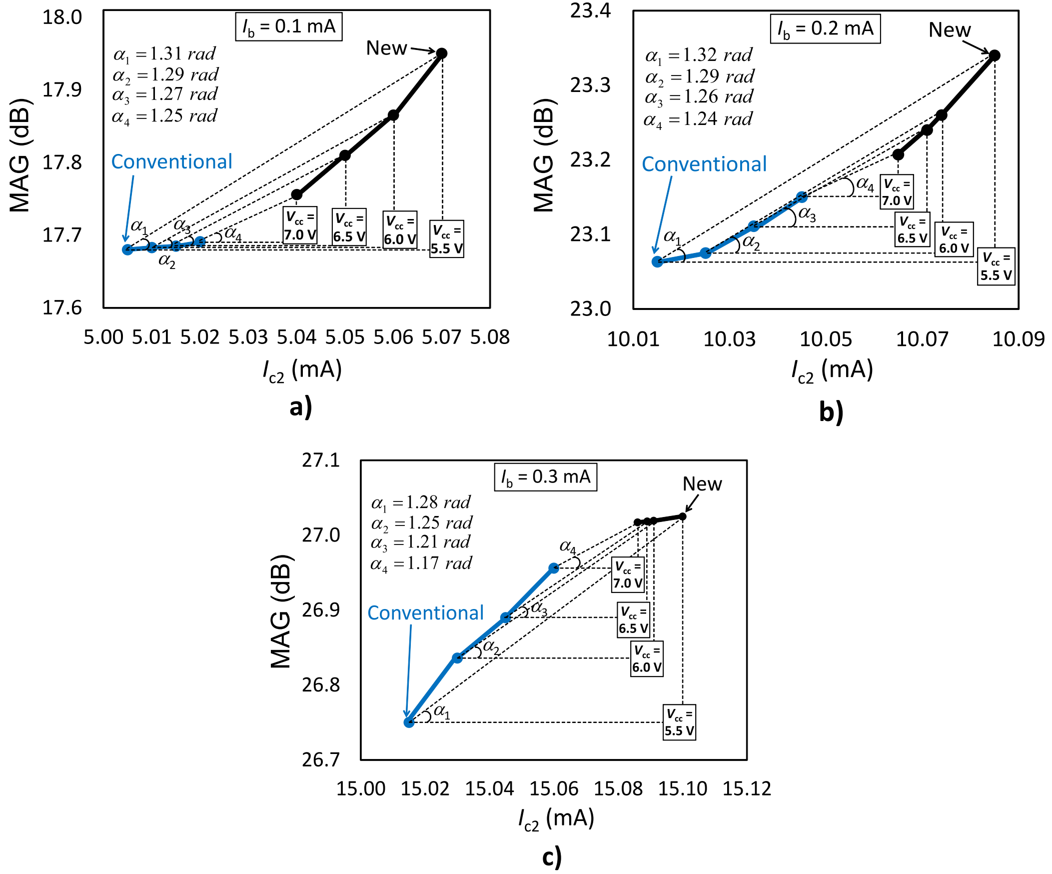


Figure 3.5: The dependence of MAG difference between the Conventional CC and Independently Biased CC employing the graphical method. The relationship between the difference in MAG or $\mathrm{MAG}_n - \mathrm{MAG}_c$ and difference in I_{c2} or $I_{\mathrm{c2n}} - I_{\mathrm{c2c}}$) is expressed through the angles α_1, α_2, α_3, and α_4. Here, I_{c2} denotes both I_{c2n} and I_{c2c}.

$I_{\mathrm{c2n}i}I_{\mathrm{c2c}i}$] with $i = 1, 2, 3$, and 4 correspondence with $V_{\mathrm{cc}} = 5.5, 6.0, 6.5$, and 7.0 V, respectively, which represent the dependence of the difference in MAG or ΔMAG on the difference in I_{c2} or ΔI_{c2} remain nearly unchanged. This means ΔMAG is only affected by ΔI_{c2} but not the I_{b}. The bias conditions for calculating MAG of the Conventional CC and Independently Biased CC are described in Table 3.1. Here, V_{c1c} and V_{c2c} are computed through the following constraint equations:

$$V_{\mathrm{c2c}} = \frac{1}{2}\left(V_{\mathrm{cc}} - \frac{V_{\mathrm{A}}}{\beta}\right). \tag{3.25}$$

Table 3.1: Bias conditions for the calculation of I_{c2} and MAG of the Conventional CC and Independently Biased CC.

I_b (mA)	V_{cc} (V)	Independently Biased CC		Conventional CC	
		V_{c1n} (V)	V_{c2n} (V)	V_{c1c} (V)	V_{c2c} (V)
0.1	5.5	2.1	3.4	5.25	0.25
	6.0	3.1	2.9	5.50	0.50
	6.5	4.3	2.2	5.75	0.75
	7.0	5.0	2.0	6.00	1.00
0.2	5.5	3.5	2.0	5.25	0.25
	6.0	4.2	1.8	5.50	0.50
	6.5	4.7	1.8	5.75	0.75
	7.0	5.5	1.5	6.00	1.00
0.3	5.5	3.8	1.7	5.25	0.25
	6.0	4.5	1.5	5.50	0.50
	6.5	5.0	1.5	5.75	0.75
	7.0	5.5	1.5	6.00	1.00

$$V_{c1c} = V_{cc} - V_{c2c}. \tag{3.26}$$

From the above discussed points about the dependence of ΔMAG and ΔMSG on ΔI_{c2} we can conclude that ΔMAG and ΔMSG are only affected by ΔI_{c2}. In other words, I_{c2} is the main factor making the difference in power gain between the Conventional CC and Independently Biased CC and thus by appropriately controlling the I_{c2}, Independently Biased CC can exhibit superior power gain compared to that of the Conventional CC. Next section will examine in which bias conditions relating to the I_{c2}, the Independently Biased CC can deliver this superior power gain performance.

3.4 Bias conditions investigation

In this seciton, the degree of freedom in bias setting of the Conventional CC and Independently Biased CC can be explained based on Fig. 3.6 and Fig. 3.7. In Fig. 3.6 which describes the possible bias regions of the Conventional CC, it can be seen that since in the Conventional CC the same collector current travels through CE and CB transistors ($I_{\mathrm{c1c}} = I_{\mathrm{c2c}}$) there are just two possible bias points, says Q_{1c} and Q_{2c} which can be established to keep that requirement for the collector current. This means the bias degree of freedom of the Conventional CC is very low. In addition, one issue arising here is if the Conventional CC is biased at these two points, one of the two transistors (CE or CB transistor) must operate in saturation region while the other one operates in the active region. On the other hand, in the case of the Independently Biased CC which is shown on Fig. 3.7, as the collector current is not necessary to be the same for CE and CB transistors, or $I_{\mathrm{c1c}} \neq I_{\mathrm{c2c}}$, the possible bias points can be set freely and independently for CE and CB transistors which are represented by bias points $\mathrm{Q}_{1n} - \mathrm{Q}_{4n}$, resulting in the higher bias degree of freedom compared to that of the Conventional CC.
Moreover, as analyzed in previous sections, I_{c2} is the key factor affecting the difference in DC power distribution as well as in power gain performance between the Independently Biased CC and Conventional CC, this section will analyze two typical bias cases to examine in which bias conditions I_{c2} of the Independently Biased CC can be higher than I_{c2} of the Conventional CC.

3.4.1 First bias case

The first bias case for the Independently Biased CC and Conventional CC is shown on Fig. 3.8. This bias condition means two transistors of the Independently Biased CC operate in the active region while one of two transistors of the Conventional CC operates in the saturation region and the other operates in the active region. As can be seen on the figure, when V_{cc} varies from $V_{\mathrm{c1cmin}} + V_{\mathrm{c2cmax}} (= V_{\mathrm{c1nmin}} + V_{\mathrm{c2n}})$ to $V_{\mathrm{c1cmax}} + V_{\mathrm{c2cmin}} (= V_{\mathrm{c1nmax}} + V_{\mathrm{c2n}})$, I_{c2} of

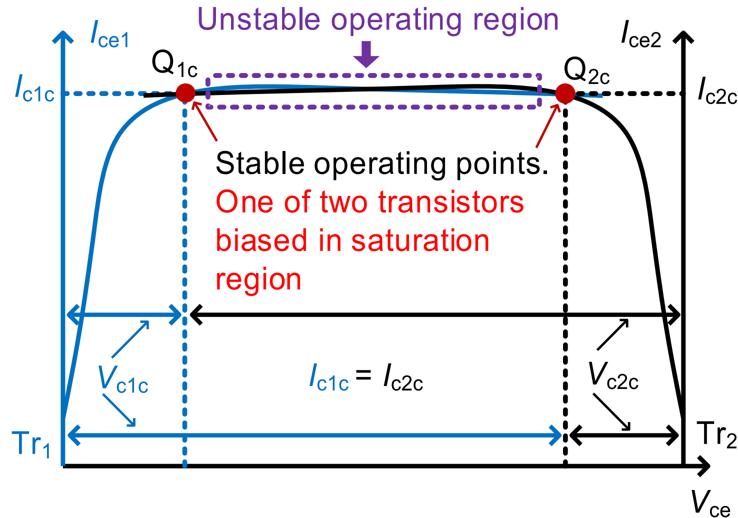


Figure 3.6: A typical load-line of the Conventional CC. Tr2 or the CB transistor is treated as a load terminal of the Tr1 or the CE transistor. Q_{1c} and Q_{2c} represent two possible or stable bias points which is contrary to the unstable bias region lying between these two points. It is noted that the total collector voltage V_{cc} remains the same at both Q_{1c} and Q_{2c} or $V_{cc} = V_{c1c} + V_{c2c}$. Moreover, in the case of the Conventional CC, $I_{c1c} = I_{c2c}$.

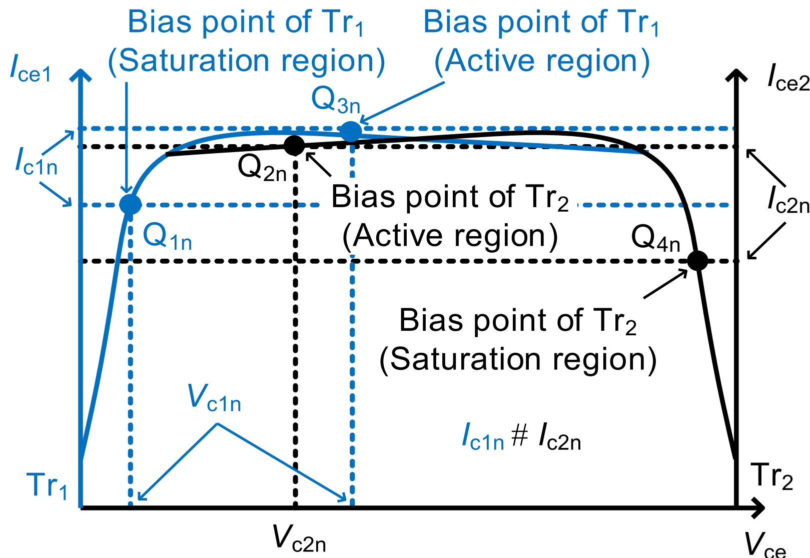


Figure 3.7: A typical load-line of the Independently Biased CC. Here Q_{1n} – Q_{4n} are sample possible bias points of the Independently Biased CC. In the Independently Biased CC V_{cc} are the same with that of the Conventional CC or $V_{cc} = V_{c1c} + V_{c2c} = V_{c1n} + V_{c2n}$.

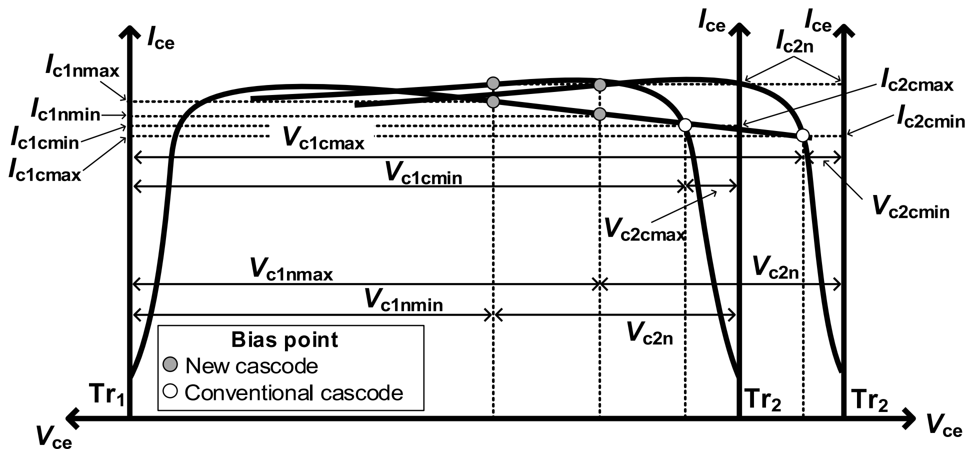


Figure 3.8: Illustration of the first bias case in which it can be seen that for the Conventional CC, at its two bias points, one of the two transistors has to be biased in the saturation region. On the other hand, in the case of the Independently Biased CC, its two transistors can be biased in the active region. With this bias condition, Independently Biased CC shows higher I_{c2} compared to that of the Conventional CC.

the Independently Biased CC or I_{c2n} is always higher than I_{c2} of the Conventional CC or I_{c2c} which varies from I_{c2cmin} to I_{c2cmax}. Hence, as analyzed in the section of DC power distribution and small-signal power gain, if this bias condition is established, the Independently Biased CC is expected to deliver higher DC power supply as well as power gain than the Conventional CC.

3.4.2 Second bias case

This bias case is illustrated on Fig. 3.9 where we can see that bias points of the Independently Biased CC are the same as that of the Conventional CC, that is, one of the two transistors is biased in the saturation while the other operates in the active region. In this bias condition, I_{c2} of the Independently Biased CC or I_{c2n} can exhibit higher or lower than I_{c2} of the Conventional CC or I_{c2c} when V_{cc} varies from $V_{\mathrm{c1cmin}} + V_{\mathrm{c2cmax}} (= V_{\mathrm{c1nmin}} + V_{\mathrm{c2n}})$ to $V_{\mathrm{c1cmax}} + V_{\mathrm{c2cmin}} (= V_{\mathrm{c1nmax}} + V_{\mathrm{c2n}})$. As a result, contrary to the first bias case, DC power as well as

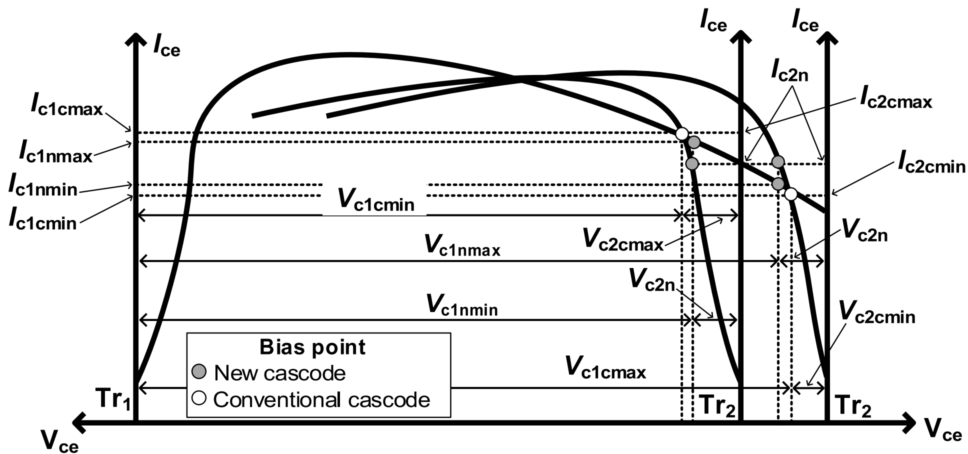


Figure 3.9: Illustration of the second bias case. In this case, bias condition of the Independently Biased CC is set the same as that of the Conventional CC, this makes the I_{c2n} to fall between I_{c2cmin} and I_{c2cmax}

.

power gain of the Independently Biased CC exhibit higher or lower than the Conventional CC. However as will be shown in experimental section, under this bias setting the circuit becomes more stable or the K-factor greater than 1.

3.5 Experimental setup

Figure 3.10 describes the experimental setup for measuring the DC parameters, DC power supply as well as MAG/MSG of the Conventional CC and Independently Biased CC. Here, K-factor and MAG/MSG are calculated by measuring the S-parameters of the Conventional CC and Independently Biased CC as two-port networks. The instruments used for experiment includes an Agilent E5270A 8-Slot Parametric Measurement Mainframe (DC power supply), an Agilent N5242A PNA-X Network Analyzer with a frequency range from 10 MHz to 26.5 GHz (Network analyzer), the bias-T is from Aeroflex/Inmet with maximum current of 2.5 A. In addition, I_{b1} and V_{cc} are implemented via bias-T whereas V_{cc1} and I_{b2} are implemented through gold wires. A 29.18 pF

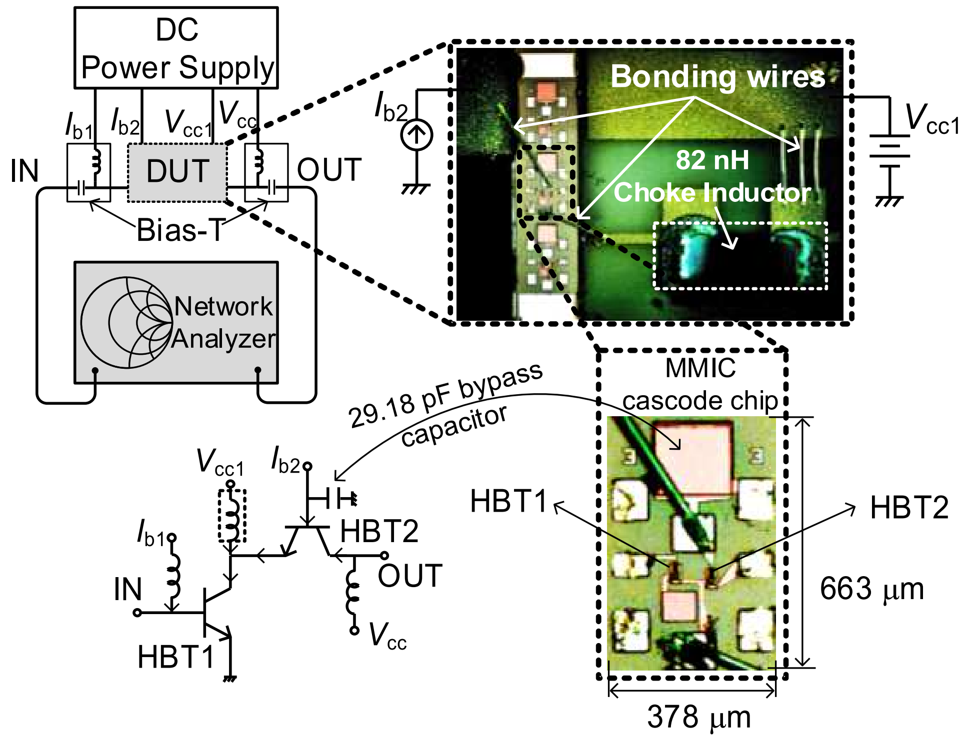


Figure 3.10: Experimental setup for DC power supply and power gain investigation between the Independently Biased CC and Conventional CC.

bypass capacitor is embedded at the base terminal of the CB transistor in the MMIC chip for RF short at a frequency of 1.9 GHz; a 82 nH choke inductor is inserted in the mid-point bias line. The cascode MMIC chip of the Independently Biased CC and Conventional CC consists of two InGaP/GaAs HBTs connecting in cascade. The chip was fabricated using foundry service by the WIN Semiconductor Corp. with substrate thickness of 75 μm.

3.6 Measured results

This section shows the experimental results together with simulated results from Agilent ADS 2011.01 simulator to confirm the DC power supply and small-signal power gain comparison investigations between the Independently Biased CC and Conventional CC in Sec. 3.2 - Sec. 3.4. Bias conditions for

Table 3.2: Bias conditions in the investigations (Exp.: experiment; Sim.: simulation).

Bias	Unit	First investigation		Second investigation	
		Exp.	Sim.	Exp.	Sim.
I_{b}	mA	0.12	0.11	0.30	0.28
V_{c1n}	V	1.0-3.0	1.3-3.3	1.5-5.5	1.58-5.58
V_{c2n}	V	4.0	3.7	0.44	0.36

simulation and measurement are described in Table 3.2. These bias conditions are established from the bias investigation as discussed in Sec. 3.3. It is noted that bias condition of the simulation is set slightly different from that of the measurement for the best agreement between their results.

3.6.1 First bias case results

3.6.1.1 DC power supply

In the DC power supply analytical investigation, we have mentioned that I_{c2} is the only factor affecting the DC power supply of the Independently Biased CC and Conventional CC and in the first bias case, DC power of the Independently Biased CC is always higher than that of the Conventional CC since I_{c2n} is always higher than I_{c2c}. This conclusion is demonstrated with both the simulated and measured results as shown on Fig. 3.11 and Fig. 3.12. In Fig. 3.11, when V_{c2n} is kept at a fixed value of 4.0 V for experiment or 3.7 V for simulation and V_{cc} varies from 5.0 V to 7.0 V which is equivalent to the variation of the V_{c1n} from 1.0 V to 3.0 V for experiment and from 1.3 V to 3.3 V for simulation, I_{c2n} which is 9.4 mA for experiment or 8.3 mA for simulation is always higher than I_{c2c} which varies from 9.05 mA to 9.26 mA for experiment or from 7.94 mA to 8.11 mA for simulation. Consequently DC power supply of the Independently Biased CC (P_{DCn}) which changes from 51.53 mW

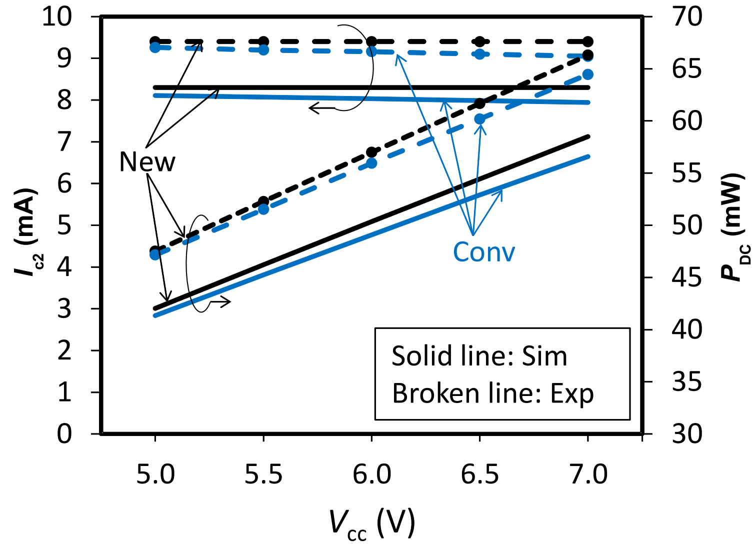


Figure 3.11: Results for the investigation of the relationship between I_{c2} and DC power supply P_{DC} of the Independently Biased CC and Conventional CC for the first bias case. Here, *New* means the Independently Biased CC and *Conv* is the Conventional CC whereas *Sim* is simulation and *Exp* is experiment.

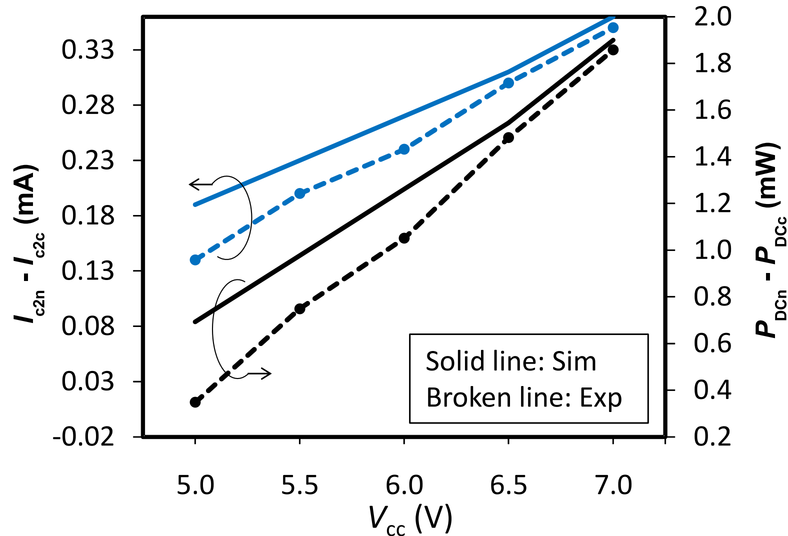


Figure 3.12: The dependence of the difference in DC power supply or $P_{DCn} - P_{DCc}$ on the difference in I_{c2} or $I_{c2n} - I_{c2c}$ for the first bias case.

to 66.31 mW for experiment or from 42.04 mW to 58.5 mW for simulation exhibits higher than that of the Conventional CC (P_{DCc}) which changes from 47.17 mW to 64.45 mW for experiment or from 45.24 mW to 56.6 mW for

simulation within the variation range of the V_{cc}. More specific illustration for this behavior can be seen on Fig. 3.12 where it shows that I_{c2n} higher than I_{c2c} from 0.14 mA to 0.35 mA for experiment or from 0.19 mA to 0.36 mA for simulation results in the higher DC power supply of the Independently Biased CC (P_{DCn}) than the Conventional CC (P_{DCc}) from 0.35 mW to 1.86 mW for experiment or from 0.69 mW to 1.86 mW for simulation.

3.6.1.2 Small-signal power gain

It was found that if the first bias case was established or both two transistors of the Independently Biased CC operate in the active region, the circuit is in stable state or the K-factor less than 1. This means the small-signal power gain is expressed in term of MSG. As shown on Fig. 3.13, when V_{cc} varies from 5.0 V to 7.0 V, with respect to the variation of the I_{c2}, MSG of the Independently Biased CC ($\mathrm{MSG_n}$) which goes from 43.59 dB to 43.82 dB for experiment or from 48.31 dB to 49.84 dB for simulation always exhibits higher than MSG of the Conventional CC ($\mathrm{MSG_c}$) that goes from 39.24 dB to 38.45 dB for experiment or from 44.83 dB to 44.53 dB for simulation. In addition, on Fig. 3.14 we can see that if I_{c2n} is higher than I_{c2c} from 0.14 mA to 0.35 mA for experiment or from 0.19 mA to 0.36 mA for simulation, $\mathrm{MSG_n}$ accordingly becomes better than $\mathrm{MSG_c}$ from 4.53 dB to 5.37 dB for experiment or from 3.48 dB to 5.37 dB for simulation.

It is obvious that in the first bias case, simulated and measured results have confirmed the fact I_{c2} is the main factor affecting the DC power as well as power gain between the Independently Biased CC and Conventional CC.

3.6.2 Second bias case results

3.6.2.1 DC power supply

The results for DC power supply investigation of the second bias case are illustrated on Fig. 3.15 and Fig. 3.16. On the Fig. 3.15, when V_{cc} varies from 1.94 V to 5.94 V which is correspondence with the variation of the V_{c1n} from 1.5

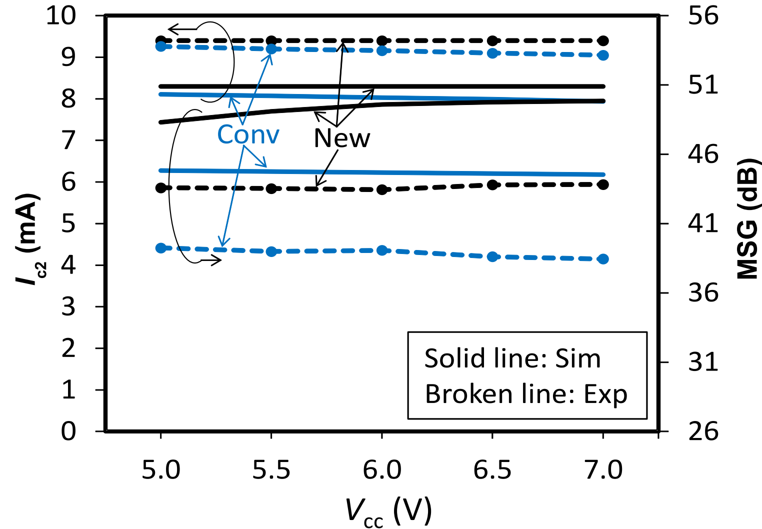


Figure 3.13: Results for the investigation of the relationship between I_{c2} and small-signal power gain (MSG) of the Independently Biased CC and Conventional CC for the first bias case.

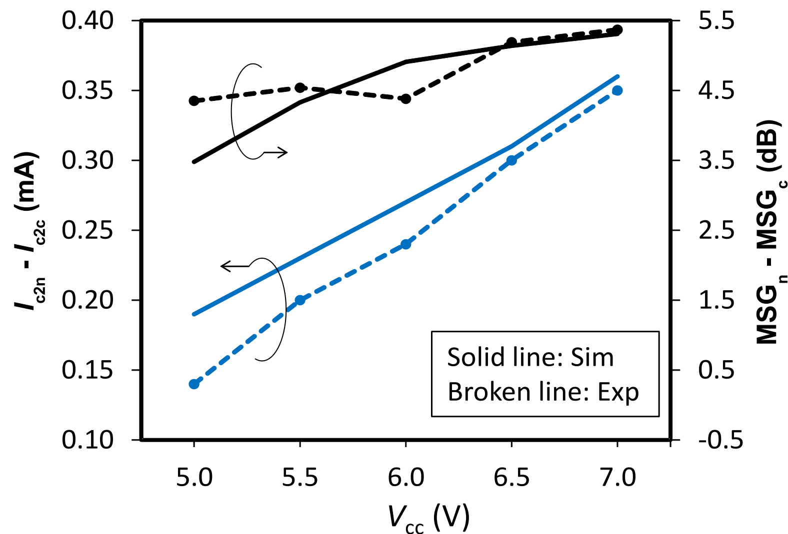


Figure 3.14: Results for the investigation of the dependence of the difference in power gain or $\mathrm{MSG_n} - \mathrm{MSG_c}$ on the difference in I_{c2} or $I_{c2n} - I_{c2c}$ for the first bias case.

V to 5.5 V for experiment and from 1.58 V to 5.58 V for simulation while V_{c2n} is kept at a constant value of 0.44 V for experiment or 0.36 V for simulation, there exists balanced points where $I_{c2n} = I_{c2c}$ and $P_{\mathrm{DCn}} = P_{\mathrm{DCc}}$. The balanced point for I_{c2c} occurs at $V_{cc} = 2.89$ V for simulation and 3.75 V for experiment whereas the balanced point for P_{DC} occurs at $V_{cc} = 2.8$ V for simulation and

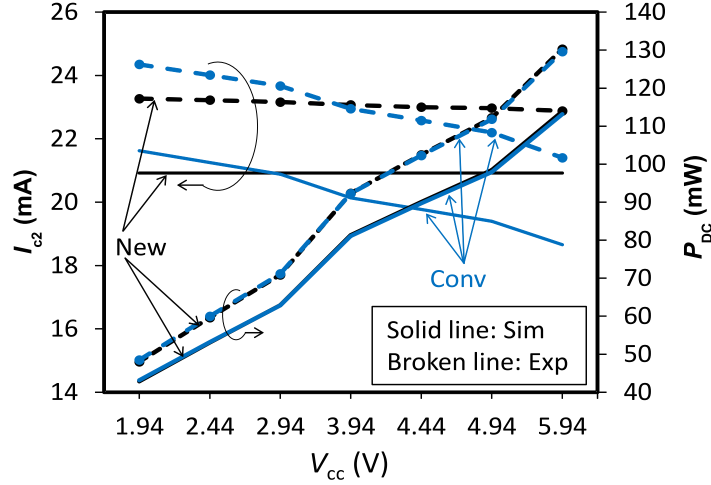


Figure 3.15: Results for the investigation of the relationship between I_{c2} and DC power supply P_{DC} of the Independently Biased CC and Conventional CC for the second bias case. Here I_{c2} represent both I_{c2n} and I_{c2c}.

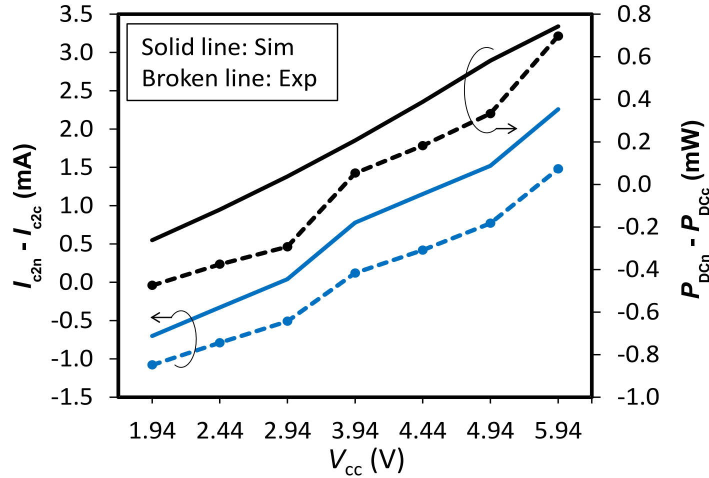


Figure 3.16: The dependence of the difference in DC power supply or $P_{DCn} - P_{DCc}$ on the difference in I_{c2} or $I_{c2n} - I_{c2c}$ for the second bias case. Both the difference in I_{c2} and difference in P_{DC} curves cross the zero-line, or the balanced point of DC power and power between the Independently Biased CC and Conventional CC.

3.87 V for experiment. This means DC power of the Independently Biased CC (P_{DCn}) can be higher or lower than that of the Conventional CC (P_{DCc}) due to the variation of the V_{cc}. Figure 3.15 demonstrates the behavior of the relationship between the difference in I_{c2} or $I_{c2n} - I_{c2c}$ and the difference in

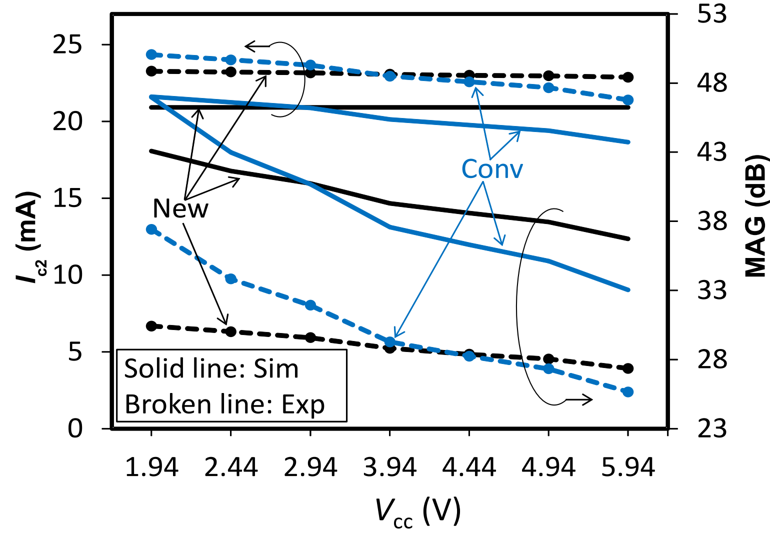


Figure 3.17: Results for the investigation of the relationship between I_{c2} and small-signal power gain (MAG) of the Independently Biased CC and Conventional CC for the second bias case.

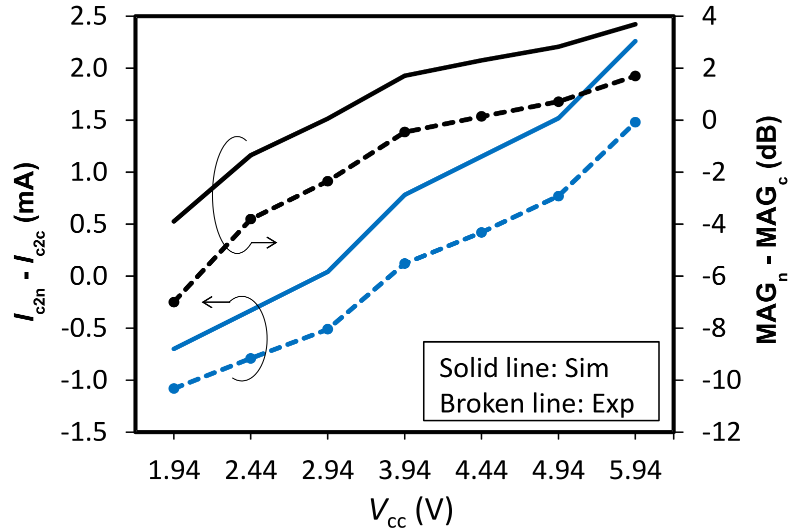


Figure 3.18: Results for the investigation of the dependence of the difference in power gain or $\mathrm{MSG_n} - \mathrm{MSG_c}$ on the difference in I_{c2} or $I_{c2n} - I_{c2c}$ for the second bias case.

P_{DC} or $P_{\mathrm{DCn}} - P_{\mathrm{DCc}}$, it can be observed in the figure that the difference in I_{c2} is directly proportional to the the difference in P_{DC}, or in other words, the higher the I_{c2} the higher the P_{DC}. In more detail, when I_{c2n} varies from a value lower than I_{c2c} 1.08 mA for experiment or 0.33 mA for simulation to a value higher than I_{c2c} 1.48 mA for experiment or 2.26 mA for simulation, P_{DCn}

consequently goes from a value lower than P_{DCc} 0.48 mW for experiment or 0.12 mW for simulation to a value higher than P_{DCc} 0.7 mW for experiment or 0.74 mW for simulation.

3.6.2.2 Small-signal power gain

In contrast to the first bias case, in the second bias case within the variation range of the V_{cc} both the Independently Biased CC and Conventional CC was found to in stable state (K-factor greater than 1), this means their small-signal power gain is expressed in term of MAG. The simulated and measured results for the investigation of the power gain dependence on I_{c2} are given on Fig. 3.17 and Fig. 3.18. On Fig. 3.17, we can also observe a balanced point for MAG where $\mathrm{MSG_n} = \mathrm{MSG_c}$. This point occur at $V_{\mathrm{cc}} = 2.91$ V for simulation and 4.31 V for experiment. Furthermore, Fig. 3.18 once again confirms the fact difference in I_{c2} varies in direct proportion to the difference in P_{DC}.
In conclusion, all the above results for the second bias case reveals that I_{c2} is the main factor not only for DC power supply but also for power gain improvement of the Independently Biased CC.

3.7 Summary

In this study, the power gain difference between a new cascode structure (Independently Biased CC) and a conventional cascode structure (Conventional CC) was investigated by examining two important bias conditions that relate to the main factor, namely, the bias current (I_{c2}) or the output resistance. It was concluded, under a conditional stable state, that the Independently Biased CC can deliver better power gain (MSG) performance than that of the Conventional CC by more than 5 dB at an operation frequency of 1.9 GHz if the bias conditions are set appropriately, thanks to its higher (I_{c2}) or higher output resistance. In spire of being unstable under some specific bias conditions, the Independently Biased CC can still offer superior power gain performance over the Conventional CC more than 2 dB at the same operation frequency

of 1.9 GHz. This is an important finding for circuit designers in considering the appropriate bias conditions for achieving a trade off between the power gain and stability of a Independently Biased CC for their specific circuit design purposes. Moreover, the research also shows that the proposed cascode structure, if acting as a power amplifier, can deliver not only high efficiency and low distortion but also better power gain performance compared with the conventional one.

Chapter 4

Microwave performances investigation of independently biased 3-stack InGaP/GaAs HBT and GaN HEMT configurations

4.1 Introduction

In the last chapter, a new circuit configuration called independently biased configuration was proposed for power gain improvement study. It was found that although the conventional cascode structure exhibits better power gain compared to a single-stage transistor thanks to the advantage of the CB transistor, our new configuration has been proved that it can deliver even better power gain and other superior features such as high linearity, low distortion when compared to the conventional cascode configuration. These superior features of the new structure are obtained by setting appropriate bias conditions independently for each individual transistor and the CB transistor's collector current (I_{c2}) was found to be the key factor of how much the difference in power gain between the new and conventional structures.

This chapter continues the study of power gain and other RF characteristics of conventional active devices (HBT and HEMT) by the investigation of bias conditions of stack devices configuration. To take the advantage of the superior high frequency power gain behavior of the CB (or CG) configuration compared to CE (or CS) configuration [92] [93] [94] as well as of the independently biased functionality, other novel circuit configurations are proposed once again. The new configurations are realized by combining the connection of CE (CS), CB (CG), CB (CG) transistors as illustrated in Fig. 4.1. Figure 4.1a and Fig. 4.1c show the conventional 3-stack structures whereas Fig. 4.1b and Fig. 4.1d show the independently biased 3-stack structures. In both conventional configurations, bias condition for each transistor cannot be adjusted independently, on the other hand by using the new configurations, thanks to the two additional mid-bias terminals, bias condition for each individual transistors is able to set independently and flexibly. This novel functionality makes it possible to improve microwave performances such as power gain, efficiency and linearity simultaneously for the proposed configurations. Firstly let's consider these advantages of this independently biased feature applied to the HBT.

4.2 Microwave performance investigation of independently biased 3-stack InGaP/GaAs HBT configuration

4.2.1 Small-signal analysis

In this section, small-signal characteristics including stability, power gain, and isolation of the independently biased 3-stack HBT structures will be studied in comparison to that of the conventional 3-stack as well as of the conventional and new cascode structures under experimental investigation.

Figure 4.2 shows the experimental procedure for on-wafer measurement of the S-parameters of the independently biased 3-stack configuration which is realistically illustrated in Figure 4.3. The configuration is implemented using a

4.2. Microwave performance investigation of independently biased 3-stack InGaP/GaAs HBT configuration

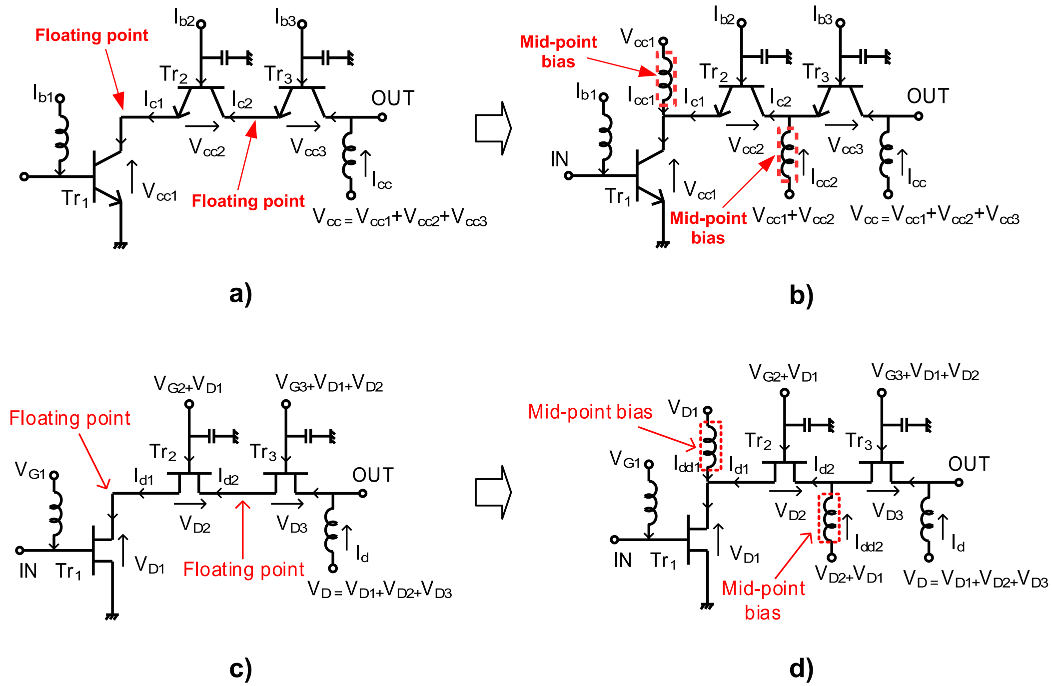


Figure 4.1: Independently biased 3-stack configurations which are the connection of one common-emitter (CE) or common-source (CS) transistor and two common-base (CB) or common-gate (CG) transistors: a) conventional 3-stack HBT configuration; b) independently biased 3-stack HBT configuration consisting two mid-bias points; c) conventional 3-stack HEMT configuration; b) independently biased 3-stack HEMT configuration consisting two mid-bias points.

Monolithic Microwave Integrated Circuit (MMIC) 3-stack HBT chip as shown in the figure. The MMIC chip consists of three InGaP/GaAs HBTs with the same size of $2 \times 20\,\mu\text{m}^2 \times 2$ which was fabricated using foundry service by the WIN Semiconductor Corp. with a substrate thickness of 75 μm. The base terminals of the three transistors are biased through current sources (I_{b1} and I_{b2}), while the last CB transistor collector terminal is biased using a voltage source (V_{cc}) through Bias-T. The base terminal of the two CB transistors and the two added bias terminal (V_{cc1} and V_{cc2}) are biased through bonding wires with negligible internal inductances. The DC power supply are Agilent E5270A

4.2. Microwave performance investigation of independently biased 3-stack InGaP/GaAs HBT configuration

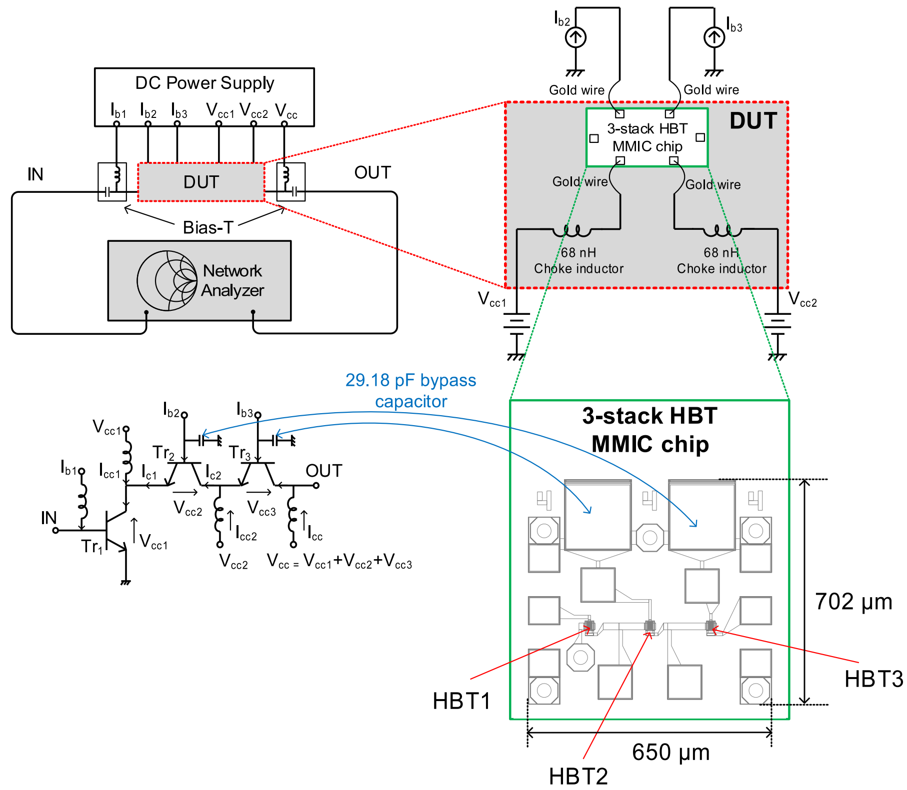


Figure 4.2: Experimental setup for measuring the S-parameters of the independently biased 3-stack HBT MMIC chip. Three transistors have the same emitter size of $2 \times 20\,\mu\text{m}^2 \times 2$ fingers

whereas the S-parameters for calculating the K-factor, MAG, and MSG, are measured using an Agilent N5242A PNA-X with a frequency range of 10 MHz to 26.5 GHz.

The small-signal analysis is conducted as follows. Firstly let us analyze the stability, power gain, and isolation characteristics of the independently biased 3-stack HBT structure under the investigation of bias conditions for each transistor to obtain the optimum bias scenario. After that comparing these optimum characteristics obtained from the optimum bias scenario of the independently biased 3-stack HBT structure with that of the conventional and independently biased cascode structures as well as the conventional 3-stack structure to demonstrate the advantages of our new 3-stack structure.

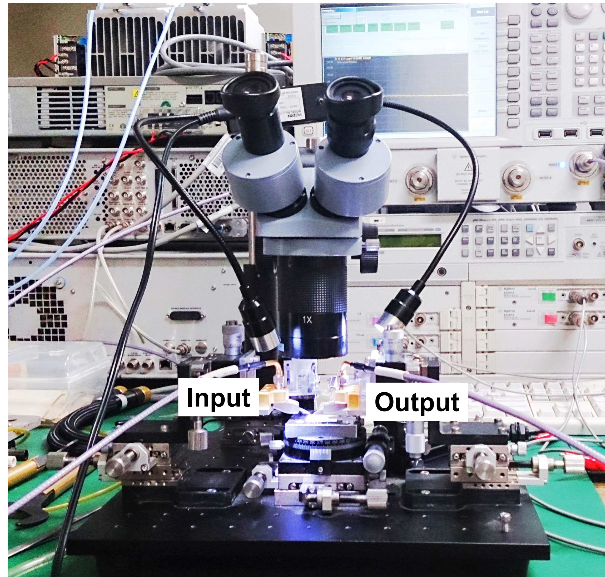


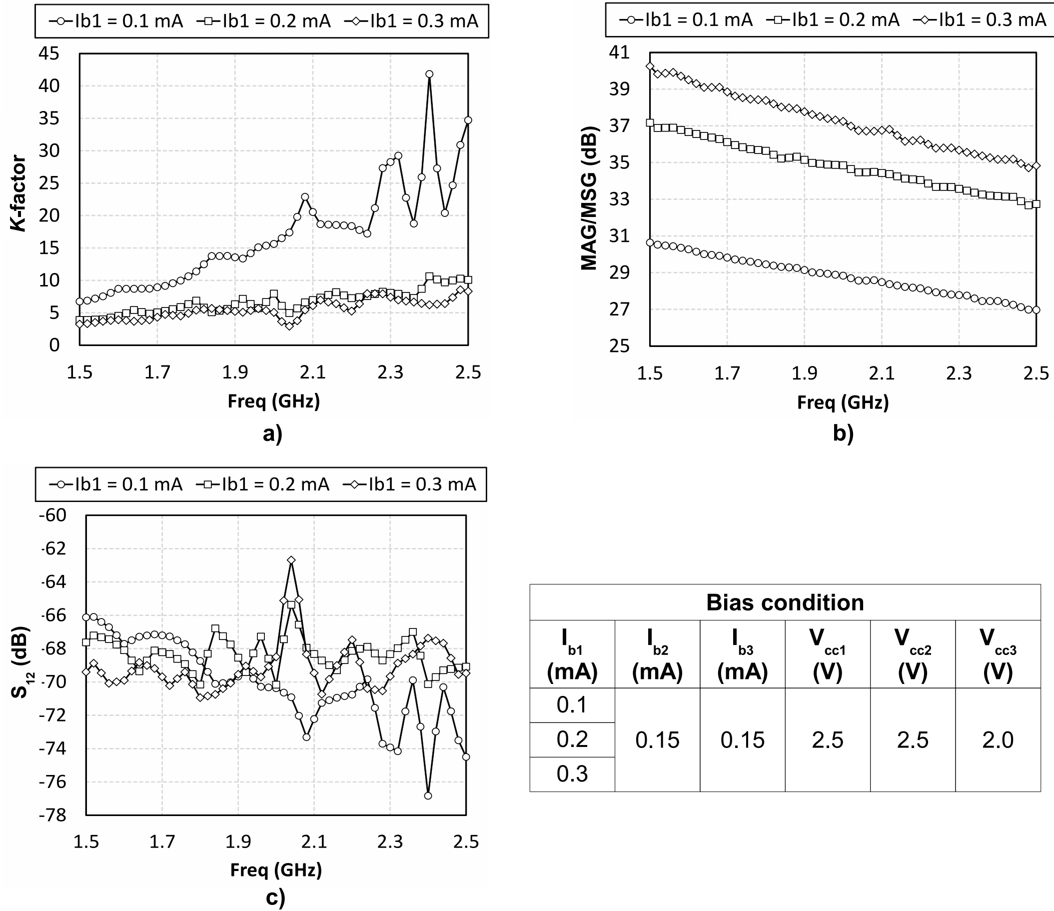
Figure 4.3: Realistic experimental setup for on-wafer S-parameters measurement of the MMIC chip.

4.2.1.1 Investigation of the first transistor's base bias current (I_{b1})

This section investigates the new 3-stack HBT configuration under the variation of I_{b1}. The bias condition for this analysis as well as the measured results are illustrated on Fig. 4.4. As can be seen on the figure, I_{b1} has a little effect to the isolation. On the other hand, it affects rather significantly the stability as well as the power gain (MAG/MSG) of the circuit. Fig. 4.4a and Fig. 4.4b show that lower I_{b1} results in higher stability but lower maximum gain (MAG). However even with higher I_{b1} ($I_{b1} = 0.2\,\text{mA}$ and $I_{b1} = 0.3\,\text{mA}$), the stability with K-factor greater than 1 is still archived yet ensuring higher MAG.

4.2.1.2 Investigation of the second transistor's base bias current (I_{b2})

The bias condition and measured results for this investigation are shown on Fig. 4.5. It is found that the circuit tends to be stable at lower I_{b2} but the power gain (MAG/MSG) must be reduced. In addition at lower I_{b2} the isolation is also poorer than that at higher I_{b2} which is illustrated on Fig. 4.5c. Finally



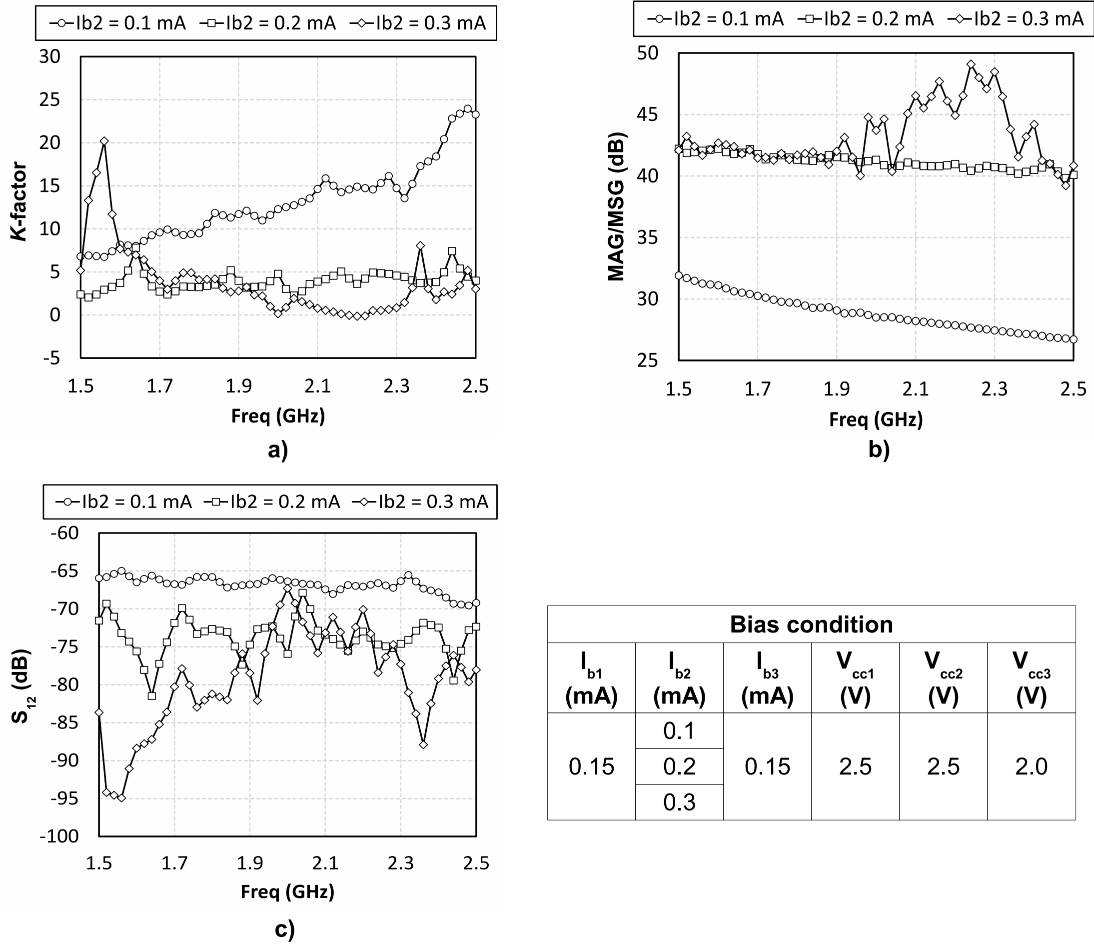
Bias condition					
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.1					
0.2	0.15	0.15	2.5	2.5	2.0
0.3					

Figure 4.4: Effect of I_{b1} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic.

the difference in characteristics between $I_{\text{b2}} = 0.2\,\text{mA}$ and $I_{\text{b2}} = 0.3\,\text{mA}$ is not so clear.

4.2.1.3 Investigation of the third transistor's base bias current (I_{b3})

Figure 4.6 illustrates the bias condition and measured results for the analysis of the proposed 3-stack characteristics under investigation of I_{b3} variation. We can see on the figure that when I_{b3} changes from 0.1 mA to 0.3 mA, the stability slightly varies whereas a remarkable change in power gain (MAG/MSG) and isolation is clearly visible. Nevertheless, the most important conclusion of this



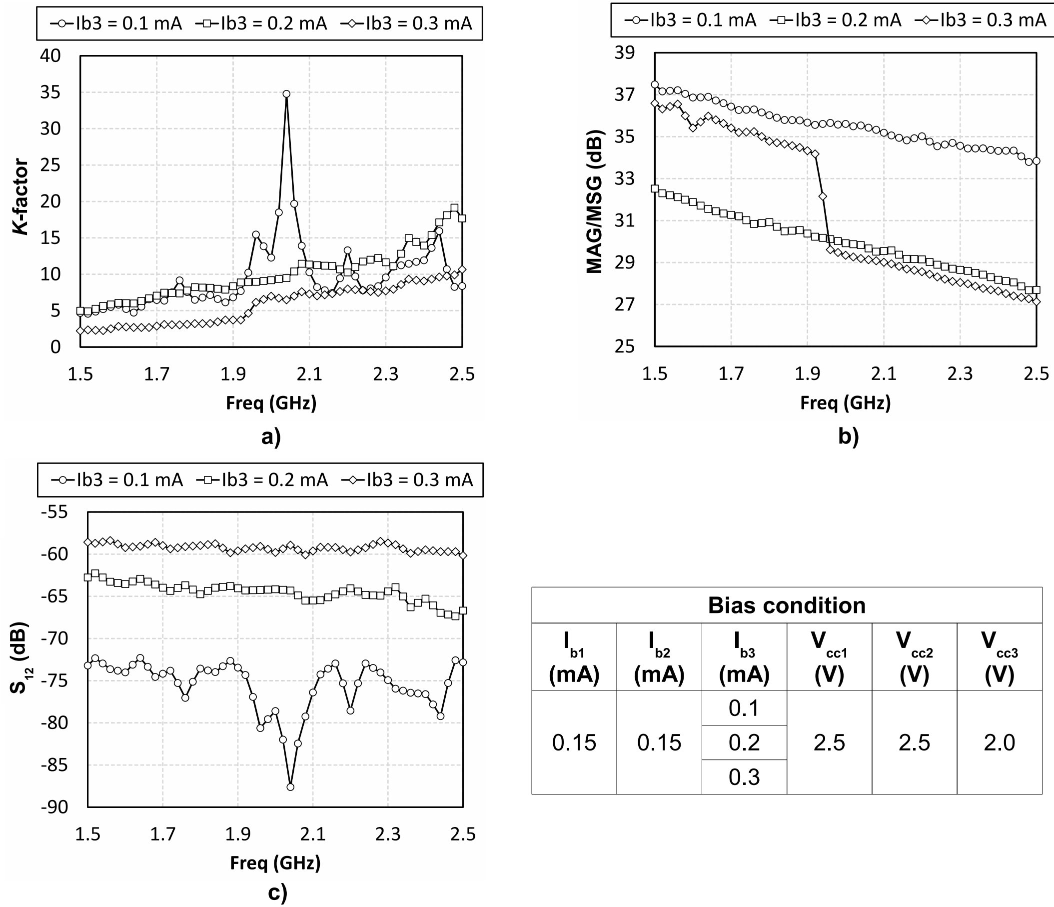
Bias condition					
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.15	0.1	0.15	2.5	2.5	2.0
	0.2				
	0.3				

Figure 4.5: Effect of I_{b2} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic.

investigation which can be drawn from the figure is lower I_{b3} can result in better performances for all characteristics including the stability, power gain and isolation. This means I_{b3} should be set at low bias values for optimum performances.

4.2.1.4 Investigation of the first mid-point bias voltage (V_{cc1})

We can see the bias condition and the measured results for this investigation on Fig. 4.7. When V_{cc1} varies from 1.0 V to 4.0 V, the investigation characteristics such as stability, power gain and isolation are not affected significantly.



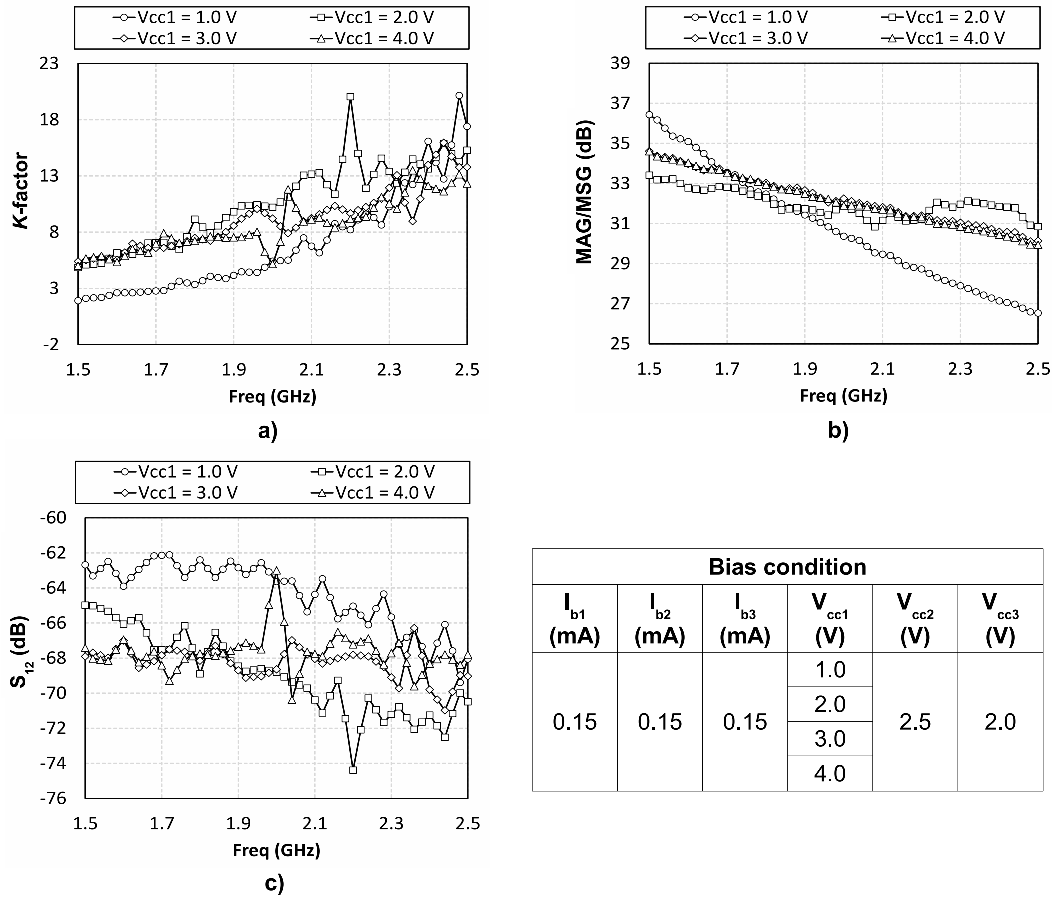
Bias condition					
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.15	0.15	0.1	2.5	2.5	2.0
		0.2			
		0.3			

Figure 4.6: Effect of I_{b3} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic.

Hence V_{cc1} seems not to be the important factor contributing to the 3-stack configuration's performance.

4.2.1.5 Investigation of the second mid-point bias voltage (V_{cc2})

In this investigation as shown on Fig. 4.8, it can be seen that V_{cc2} influences considerably on the power gain (MAG/MSG) but a little on the stability as well as the isolation characteristics. However, generally it can conclude that the the proposed 3-stack exhibits better performance for power gain and stability at $V_{cc2} = 2.0\,\text{V}$ and better isolation at $V_{cc2} = 4.0\,\text{V}$.

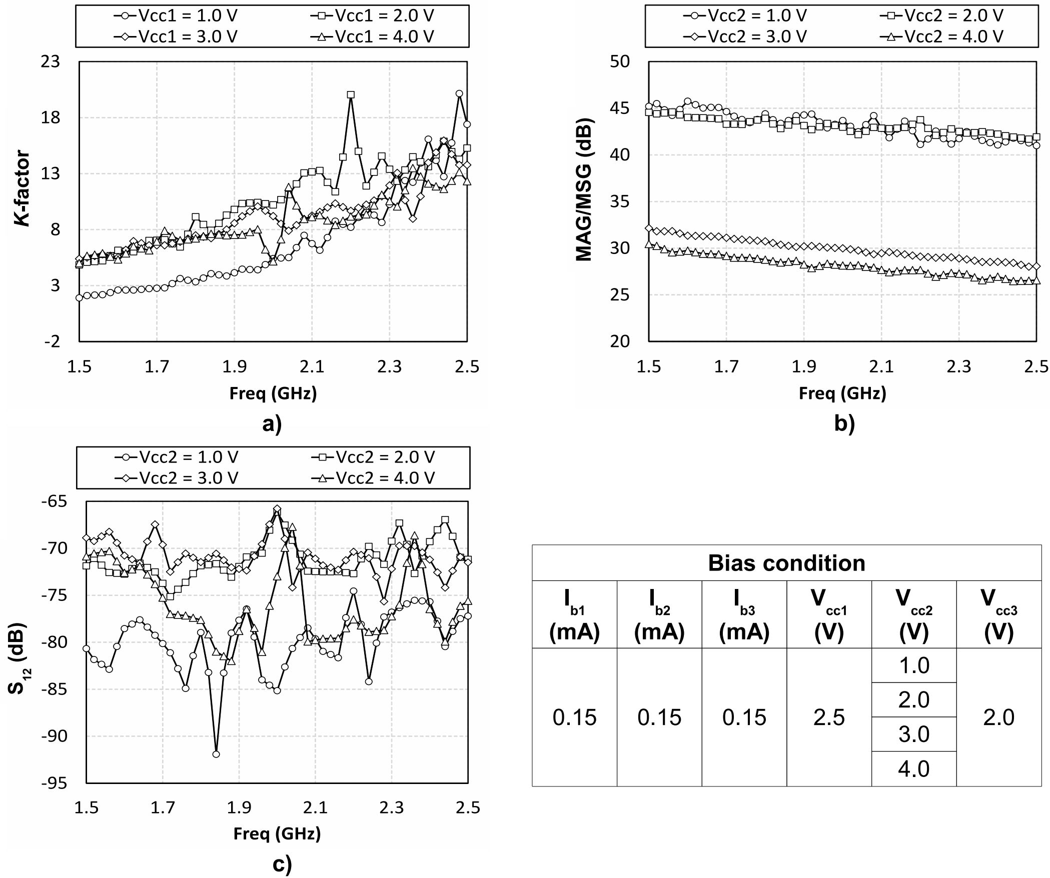


Bias condition					
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.15	0.15	0.15	1.0	2.5	2.0
			2.0		
			3.0		
			4.0		

Figure 4.7: Effect of V_{cc1} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic.

4.2.1.6 Investigation of the third collector bias voltage (V_{cc3})

Contrary to the contribution of V_{cc1} and V_{cc2}, the influence of V_{cc3} on the proposed configuration is rather remarkable as can be seen on the Fig. 4.9. When V_{cc3} varies from 1.0 V to 4.0 V, the investigated characteristics including stability, power gain, and isolation can be improved considerably, especially for the power gain and isolation. Figure 4.9a shows that we can stabilize the configuration from an unstable state (K-factor less than 1 at $V_{\mathrm{cc3}} = 3.0\,\mathrm{V}$ and $V_{\mathrm{cc3}} = 4.0\,\mathrm{V}$) by lowering V_{cc3} (at $V_{\mathrm{cc3}} = 1.0\,\mathrm{V}$ and $V_{\mathrm{cc3}} = 2.0\,\mathrm{V}$) but this causes the power gain as well as isolation poorer. In power amplifier fabrication, we



<table>
<tr><th colspan="6">Bias condition</th></tr>
<tr><th>I_{b1} (mA)</th><th>I_{b2} (mA)</th><th>I_{b3} (mA)</th><th>V_{cc1} (V)</th><th>V_{cc2} (V)</th><th>V_{cc3} (V)</th></tr>
<tr><td rowspan="4">0.15</td><td rowspan="4">0.15</td><td rowspan="4">0.15</td><td rowspan="4">2.5</td><td>1.0</td><td rowspan="4">2.0</td></tr>
<tr><td>2.0</td></tr>
<tr><td>3.0</td></tr>
<tr><td>4.0</td></tr>
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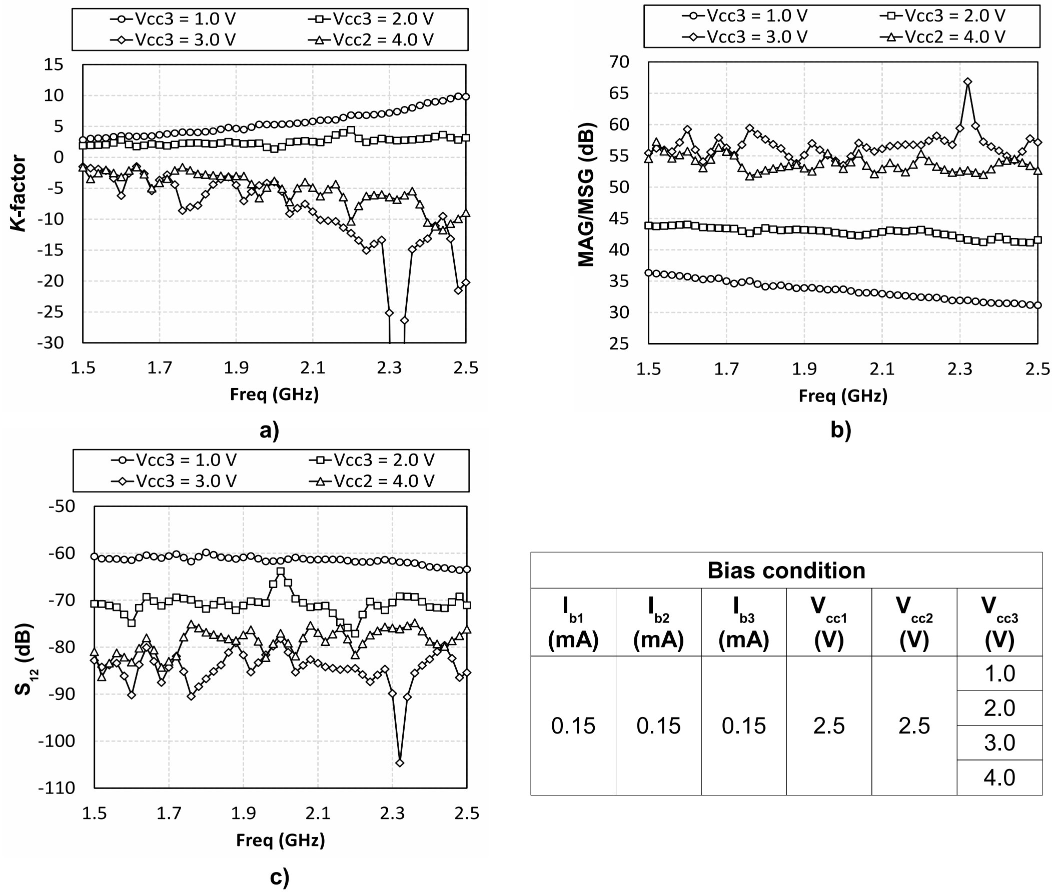
Figure 4.8: Effect of V_{cc2} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic.

have to take this behavior into account to have a trade-off between the large-signal characteristics such as power gain, efficiency, linearity and the stability of the circuit. For instant, although if setting $V_{cc3} = 4.0\,\text{V}$ we can obtain very good isolation and power gain, the circuit then becomes unstable, hence it is necessary to use stabilization techniques for this situation.

Finally, all the above investigation of bias conditions for improvement of the performance can be summarized in Table 4.1. The table shows that V_{cc1} does not contribute to the performance improvement whereas I_{b3} seems to be the most important factor contributing to the performance improvement, that is, decreasing I_{b3} improves the circuit performance. Moreover, to obtain the



Bias condition					
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.15	0.15	0.15	2.5	2.5	1.0
					2.0
					3.0
					4.0

Figure 4.9: Effect of V_{cc3} on the new 3-stack HBT configuration's characteristics. Here: a) stability characteristic; b) maximum power gain (MAG/MSG) characteristic; c) isolation (S_{12}) characteristic.

Table 4.1: Summary of the measured small-signal performance investigation.

Improved characteristics	**Bias parameters** (↑: increase; ↓: decrease; ◯: no effect)					
	I_{b1}	I_{b2}	I_{b3}	V_{cc1}	V_{cc2}	V_{cc3}
Stability (K-factor)	↓	↓	↓	◯	◯	↓
Power gain (MAG/MSG)	↑	↑	↓	◯	↓	↑
Isolation (S_{12})	◯	↑	↓	◯	◯	↑

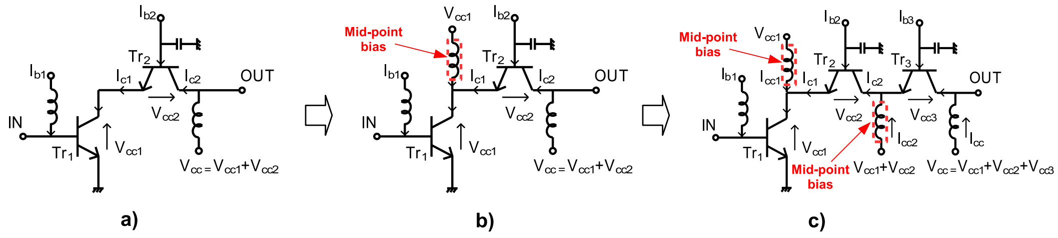


Figure 4.10: The conventional, proposed cascode and 3-stack configurations: a) conventional cascode configuration; b) proposed cascode configuration or independently biased cascode configuration; c) 3-stack configuration.

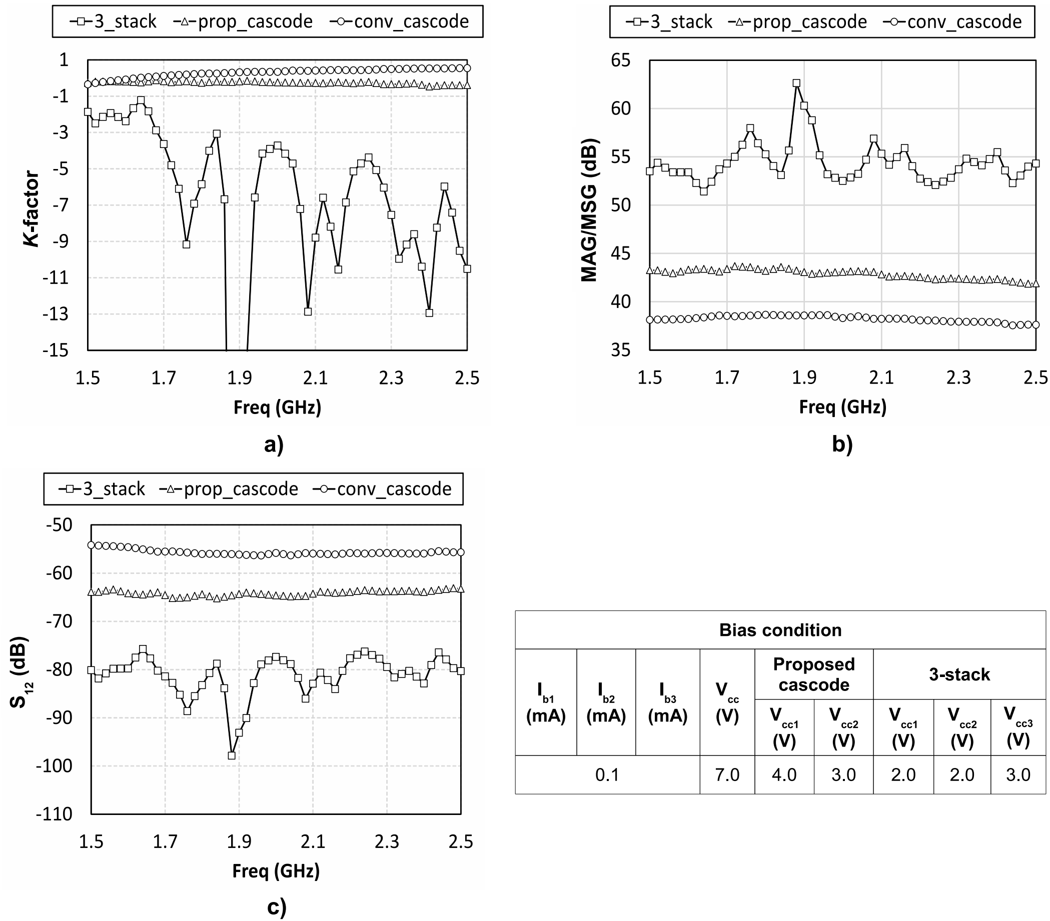
best stability for the circuit, all the biases should be set at low level, however the power gain and isolation then become degraded. This implies we can set appropriate bias values so that the stability of the circuit should be sacrificed to improve other performance including power gain and isolation.

4.2.1.7 Comparison of performances between the independently biased 3-tack HBT structure and the conventional, independently biased HBT cascode structures

This section demonstrates the superior performances of the independently biased 3-stack HBT by making a comparison of the performance between it and conventional, independently biased cascode (or proposed cascode) configurations. These configurations are depicted on Fig. 4.10 where the conventional cascode structure has no additional bias point whereas the proposed cascode and 3-stack structures have one and two additional bias terminals respectively. Now in order to make a logical comparison in performance among these configurations, following assumptions must be considered:

- All HBTs have the same size of $2 \times 20\,\mu\text{m}^2 \times 2$ fingers.
- The base terminals of the three structures should be biased under the same current values ($I_{\text{b1}} = I_{\text{b2}} = I_{\text{b3}} = I_{\text{b}}$) to avoid any adverse impact since the HBTs have the same emitter size.
- The total collector bias voltage (V_{cc}) is set the same for all the three struc-

4.2. Microwave performance investigation of independently biased 3-stack InGaP/GaAs HBT configuration



Bias condition								
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc} (V)	Proposed cascode		3-stack		
				V_{cc1} (V)	V_{cc2} (V)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.1			7.0	4.0	3.0	2.0	2.0	3.0

Figure 4.11: Performances comparison between three types of configurations at $I_{\mathrm{b}} = 0.1$mA: independently biased 3-tack HBT, the conventional and proposed cascodes; the bias conditions are also shown. Here: a) stability characteristic; b) power gain characteristic; c) isolation characteristic.

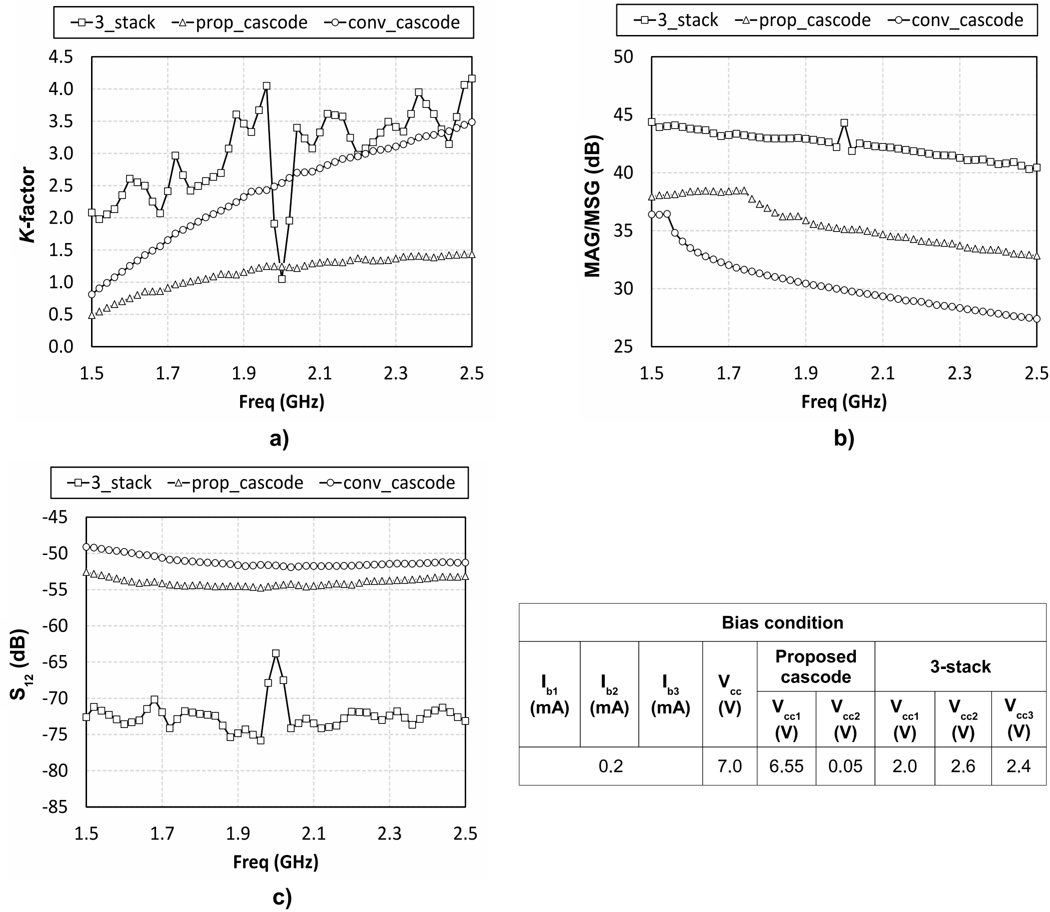
tures.

In the next section, the performances under both unstable and stable conditions (K-factor less than 1 and greater than 1) are compared to each other to obtain the maximum power gain in MSG and MAG respectively.

- **First investigation under unstable condition at $I_{\mathrm{b}} = 0.1\,\mathrm{mA}$.**

Figure 4.11 shows the performance comparison between the three structures: proposed 3-stack, conventional cascode and proposed cascode structures, in addition the bias conditions for all the structures are also given in the figure.

4.2. Microwave performance investigation of independently biased 3-stack InGaP/GaAs HBT configuration



Bias condition								
				Proposed cascode		3-stack		
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc} (V)	V_{cc1} (V)	V_{cc2} (V)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.2			7.0	6.55	0.05	2.0	2.6	2.4

Figure 4.12: Performances comparison between three types of configurations at $I_{\mathrm{b}} = 0.2\,\mathrm{mA}$: independently biased 3-tack HBT, the conventional and proposed cascodes; the bias conditions are also shown. Here: a) stability characteristic; b) power gain characteristic; c) isolation characteristic.

In this investigation, the total collector bias voltage (V_{cc}) is set to 7.0 V. The bias condition for each transistor of the proposed cascode and 3-stack structures are established in order to obtain the optimum power gain (MAG/MSG). Under such bias conditions establishment, we can see in the Fig. 4.11b that the 3-stack structure can deliver significantly higher power gain (MSG) than the other two structures. Moreover, its isolation characteristic also exhibits better than the conventional and proposed cascode structures. However Fig. 4.11a points out that the stability of the proposed 3-stack structure must be sacrificed to obtain these superior power gain as well as isolation.

- Second investigation under stable condition at $I_b = 0.2\,\mathbf{mA}$.

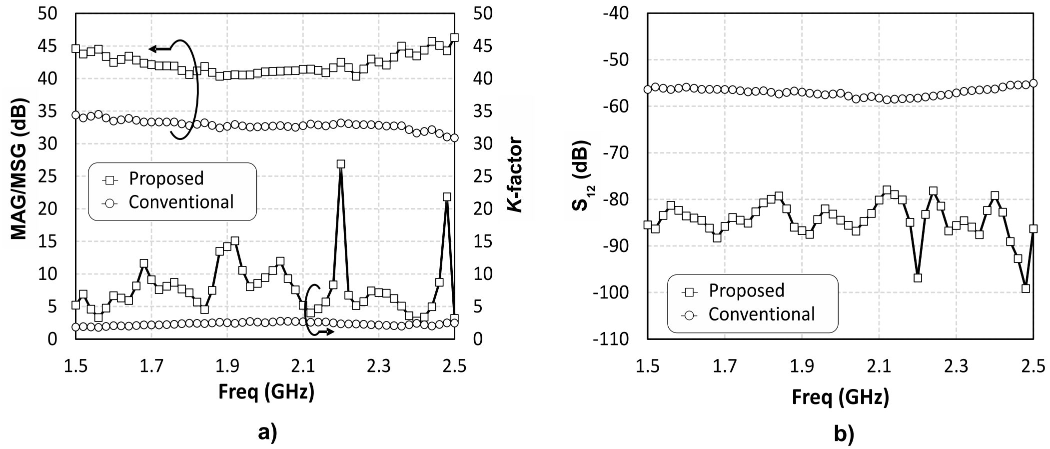
This investigation results are given on Fig. 4.12 where the bias conditions as well as performance comparison among the structures are shown. In this case, to obtain the stable state or the K-factor greater than 1, the bias condition for each transistor has been changed at the base bias current of 0.2 mA. It can be clearly observed on Fig. 4.12 the superior performances of the 3-stack structure over the conventional and proposed cascode structures. The 3-stack structure deliver remarkably better isolation compared to the remaining two structures which is illustrated in Fig. 4.12c. In addition to this advantage, it also exhibits not only the better power gain, but stability than the conventional and proposed cascode configurations which is given on Fig. 4.12a and Fig. 4.12b.

4.2.1.8 Performance comparison between the independently biased 3-tack HBT structure and the conventional 3-stack HBT structure

In the last sections it has been proved that our proposed 3-stack HBT structure which owing to the two added bias terminals can exhibit better performances compared to the conventional and independently biased cascode structures. This section continues to demonstrate the advantages in performance of the new 3-stack structure by comparing its performance with the conventional 3-stack structure.

- First investigation at $I_b = 0.1\,\mathbf{mA}$.

This investigation results are illustrated on Fig. 4.13 where it is clearly seen the better performances including both stability, power gain and isolation of the independently biased 3-stack compared to the conventional one. In Fig. 4.13a power gain of the proposed configuration shows better power gain with an maximum amount of 15 dB at 2.5 GHz whereas in Fig. 4.13c, a better isolation with a maximum amount of 39 dB for the proposed structure can be observed. Here both the conventional and proposed structures are compared under the stable condition, or their K-factor is greater than 1.



Bias condition									
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc} (V)	Conv 3-stack			Proposed 3-stack		
				V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.1			7.0	5.36	0.88	0.76	0.50	5.80	0.70

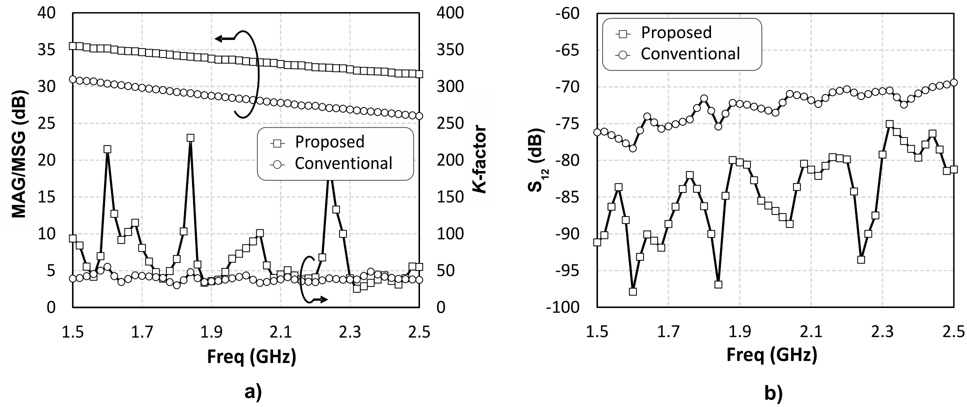
Figure 4.13: Performances comparison between independently biased 3-stack HBT configuration and the conventional one at $I_{\mathrm{b}} = 0.1$mA; the bias conditions are also given. Here: a) power gain characteristic; b) isolation characteristic.

- **Second investigation at $I_{\mathbf{b}} = 0.2\,\mathbf{mA}$.**

When base bias currents increase to $I_{\mathrm{b}} = 0.2\,\mathrm{mA}$, we still can observe the better stability, power gain as well as isolation for the proposed 3-stack structure as illustrated in Fig. 4.14. In Fig. 4.14a, power gain (MAG) of the proposed structure exhibits superior over the conventional one with a maximum amount of about 5.67 dB at 2.5 GHz while it can also deliver a better isolation than the conventional one with a maximum amount of 20 dB at 1.6 GHz as can be seen on Fig. 4.14b.

4.2.2 Large-signal analysis

From the previous small-signal investigations regarding the bias conditions analysis, this section studies the large-signal behavior of our proposed 3-stack



Bias condition									
I_{b1} (mA)	I_{b2} (mA)	I_{b3} (mA)	V_{cc} (V)	Conv 3-stack			Proposed 3-stack		
				V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)	V_{cc1} (V)	V_{cc2} (V)	V_{cc3} (V)
0.2			7.0	6.33	0.35	0.32	0.50	6.09	0.41

Figure 4.14: Performances comparison between independently biased 3-stack HBT configuration and the conventional one at $I_{\text{b}} = 0.2$mA; the bias conditions are also given. Here: a) power gain characteristic; b) isolation characteristic.

HBT MMIC chip by fabricating an RF power amplifier using the chip and testing its large-signal performances such as power gain, output power and linearity at the frequency of 1.6 GHz. However, firstly let me investigate its large-signal behavior under the simulation.

4.2.2.1 Simulation investigation

The 3-stack HBT MMIC chip based amplifier circuit is depicted on Fig. 4.15 where we can see the amplifier includes the 3-stack HBT MMIC chip, the input and output matching networks which are composed of lumped components (inductors L_{i}, L_{o} and capacitors C_{i}, C_{o}). Here the capacitors C_1-C_6 are RF bypass ones whereas the resistor R is used as a dissipated component to prevent the amplifier from a spurious oscillation. The amplifier operates under six bias terminals which are three current sources (I_{b1}, I_{b2}, and I_{b3}) and three voltage sources (V_{cc1}, V_{cc2}, and V_{cc}).

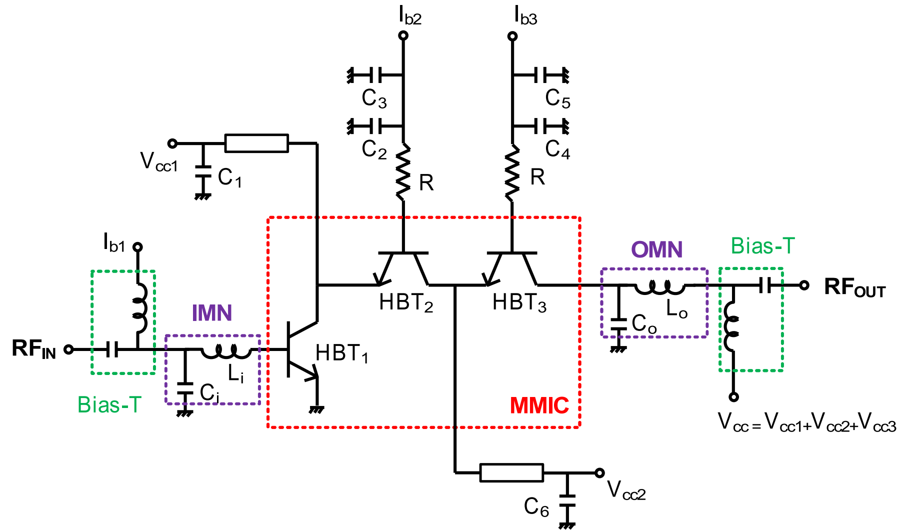


Figure 4.15: The 3-stack HBT MMIC chip based amplifier circuit.

To simulate the amplifier's large-signal characteristics, an Agilent ADS 2011.01 simulator is used with the circuit schematic as shown on Fig. 4.16. The HBT model used for simulation is from WIN Semiconductor Corp. that is based on the VBIC model for bipolar junction transistor. The lumped components model which is composed of the input and output matching networks is from the Murata with LQW18AN, LQW15AN and GRM1555C series. The RF bypass capacitors models are GRM1555C and GRM15XR series. The design frequency is at 1.6 GHz.

- Gain and efficiency investigation under the effect of various bias conditions.

The simulated results for the investigation of effect of the base bias currents are demonstrated on Fig. 4.17. The figure clearly shows that when the base bias current varies from 0.15 mA to 0.17 mA there is no considerable influence of the base bias current on the amplifier's performance including gain and efficiency (PAE) are observed. In addition to the investigation of the base bias current effect, Fig. 4.18 illustrates the results for the investigation of collector bias voltages effect. When the second and third-stage collector bias voltages V_{cc2}, V_{cc2} varies from 0.5 V to 1.5 V and from 3.5 V to 4.5 V respectively,

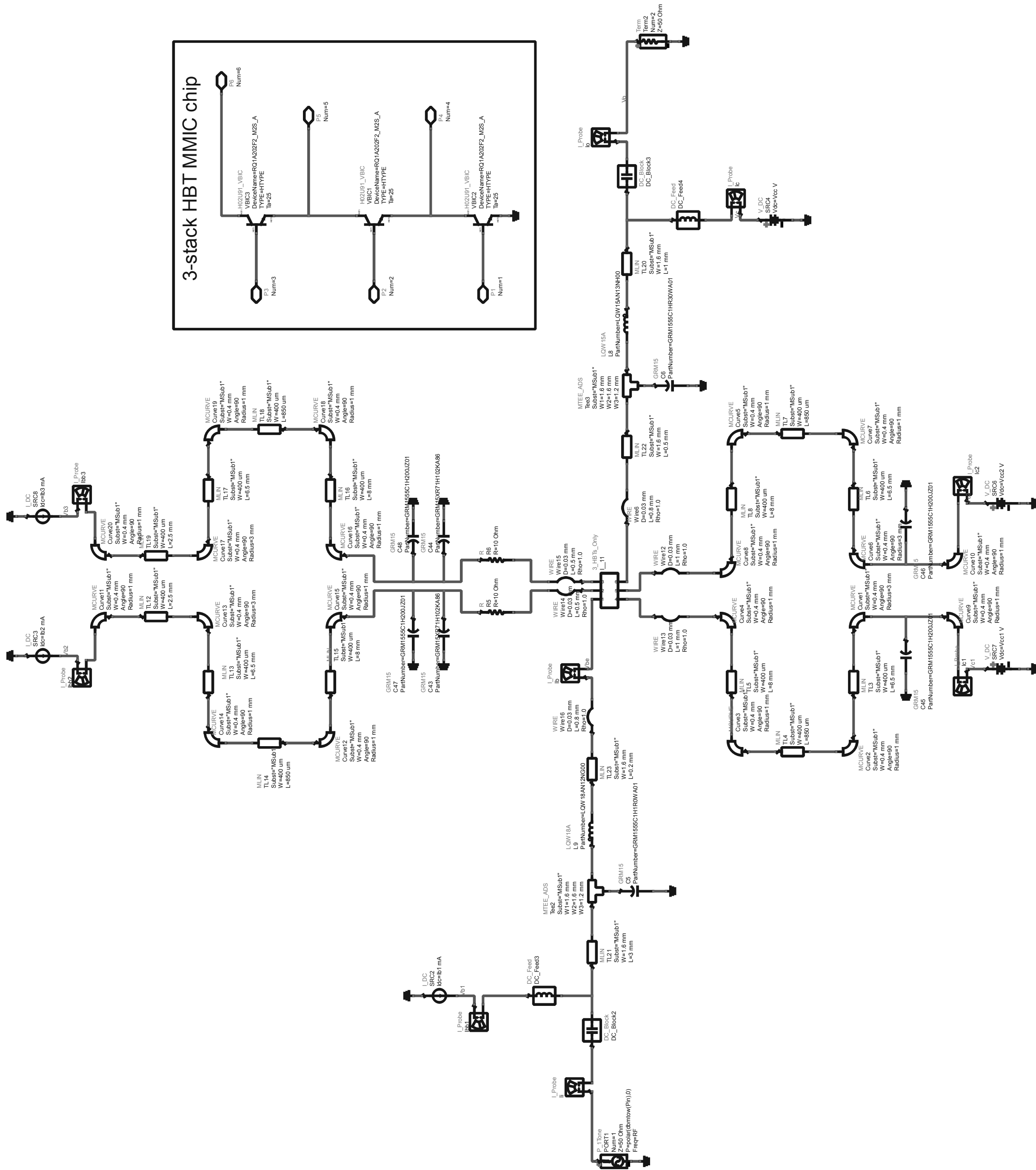


Figure 4.16: The ADS schematic of the 3-stack HBT MMIC chip based amplifier for simulation.

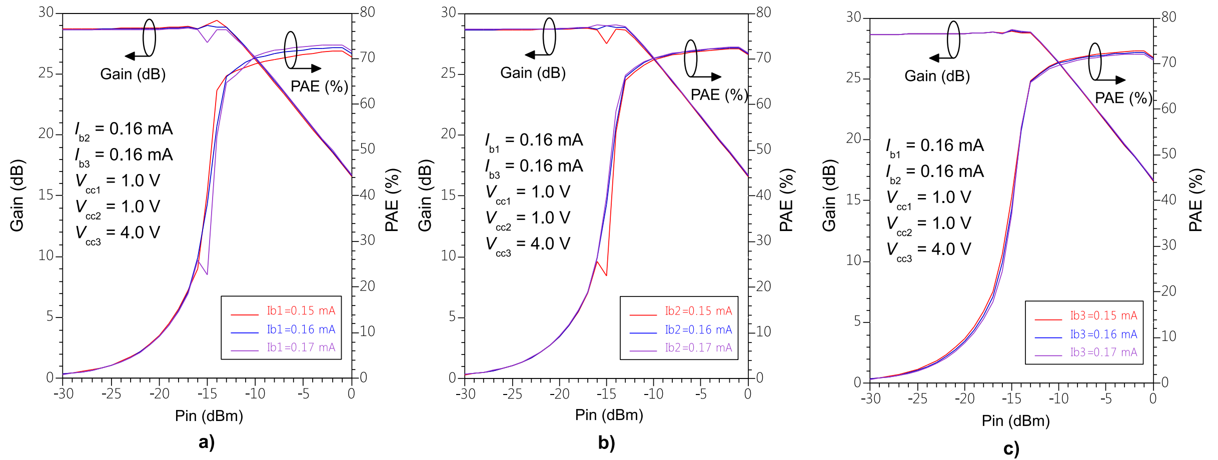


Figure 4.17: One-tone gain and PAE characteristics of the amplifier under the influence of the base bias current I_b at f = 1.6 GHz: a) I_{b1} variation; b) I_{b2} variation; c) I_{b3} variation.

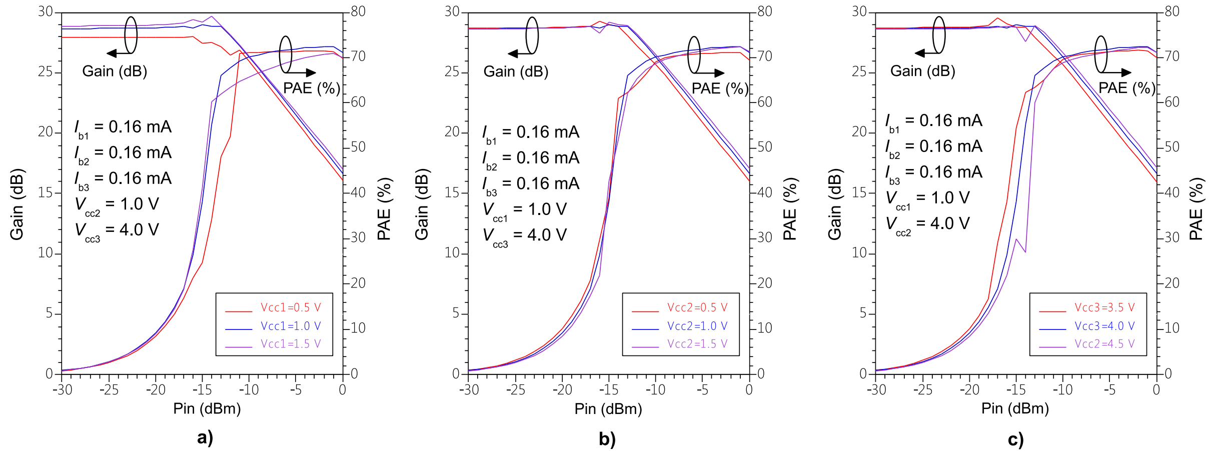


Figure 4.18: One-tone gain and PAE characteristics of the amplifier under the influence of the collector bias voltages at f = 1.6 GHz: a) V_{cc1} variation; b) V_{cc2} variation; c) V_{cc3} variation.

gain and PAE of the amplifier seems not to be affected remarkably as shown in Fig. 4.18b and Fig. 4.18c. This means V_{cc2} and V_{cc2} are not the important factor contributing to the performance improvement. On the other hand, in Fig. 4.18a, it can observed improvement of gain and efficiency if the first-stage collector bias voltage is increased. Hence V_{cc1} is the only factor among the bias parameters affects the gain and efficiency characteristics.

- Distortion (IMD3) characteristic investigation under the effect of

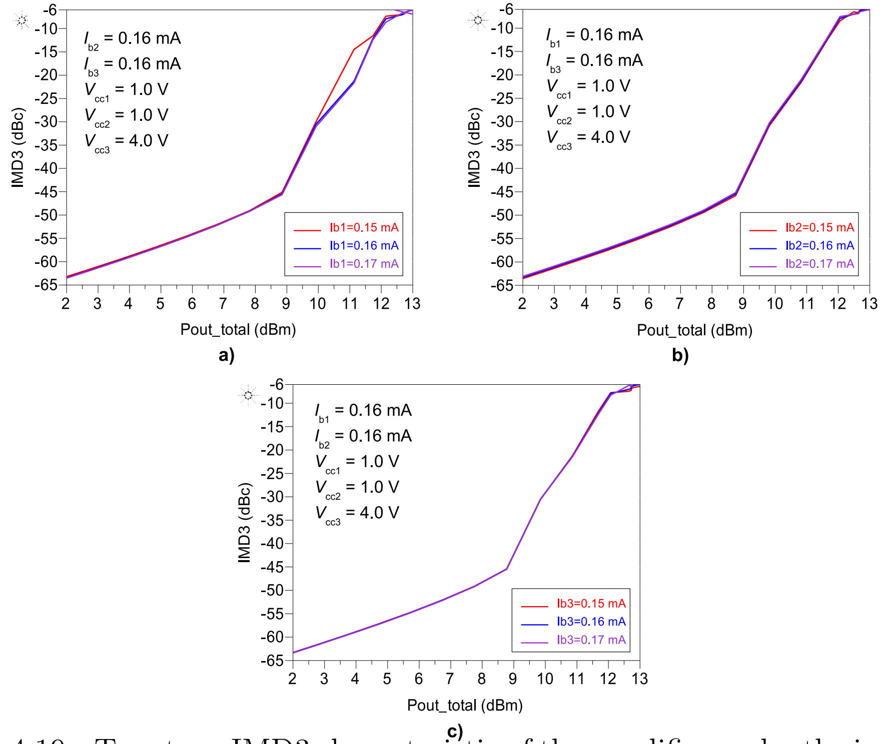


Figure 4.19: Two-tone IMD3 characteristic of the amplifier under the influence of the base bias current I_b at f = 1.6 GHz and frequency spacing Δf = 4 MHz: a) I_{b1} variation; b) I_{b2} variation; c) I_{b3} variation.

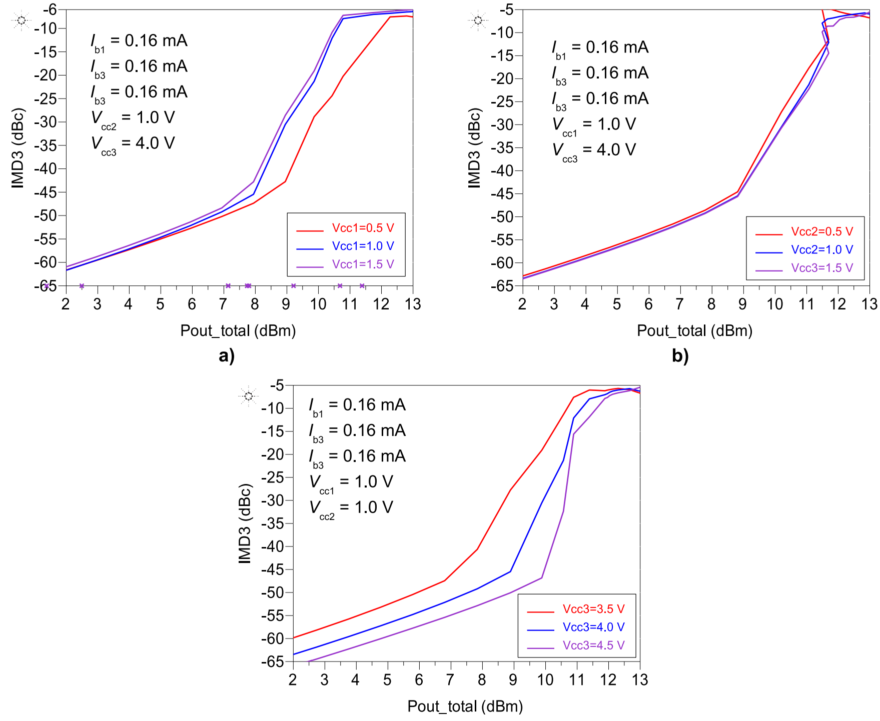


Figure 4.20: Two-tone IMD3 characteristic of the amplifier under the influence of the collector bias voltage V_{cc} at f = 1.6 GHz and frequency spacing Δf = 4 MHz: a) V_{cc1} variation; b) V_{cc2} variation; c) V_{cc3} variation.

Table 4.2: Summary of the simulated large-signal performance investigation.

Improved characteristics	Bias parameters (↑: increase; ↓: decrease; ◯: no effect)					
	I_{b1}	I_{b2}	I_{b3}	V_{cc1}	V_{cc2}	V_{cc3}
Gain	◯	◯	◯	◯	◯	◯
Efficiency (PAE)	◯	◯	◯	◯	◯	◯
Distortion (IMD3)	◯	◯	◯	↓	◯	↑

various bias conditions.

Figure 4.19 presents the simulated results for the investigation of IMD3 characteristic under the influence the base bias current. It is figured out on the figure that base bias current doesn't contribute to the improvement of the amplifier's linearity, it cannot observe a significant variation of IMD3 under the change of base bias current. This trend is the same as the investigation of gain and PAE characteristics. Consequently, the base bias current doesn't play an important role in performance enhancement. In contrast to to the influence of the base bias current on the performance, Fig. 4.20 shows a remarkable improvement of the IMD3 with respect to the change of collector bias voltages. Figure 4.20a and Fig. 4.20c illustrates the fact that the IMD3 of the amplifier can be improved by lowering the first-stage collector bias voltage V_{cc1} and increasing the last stage one V_{cc3}.

Finally, the above investigation results are summarized in table 4.2 where it shows that we should decrease V_{cc1} and increase V_{cc3} for performance improvement whereas the other bias parameters don't have a significant influence on the performance. Moreover, Fig. 4.21 summarizes the measured small-signal and simulated large-signal performances of the proposed configuration with respect to the variation of the bias parameters. As can be seen in the figure, various amplifier's important small-signal and large-signal performances like stability, isolation, linearity, efficiency and especially power gain can be traded

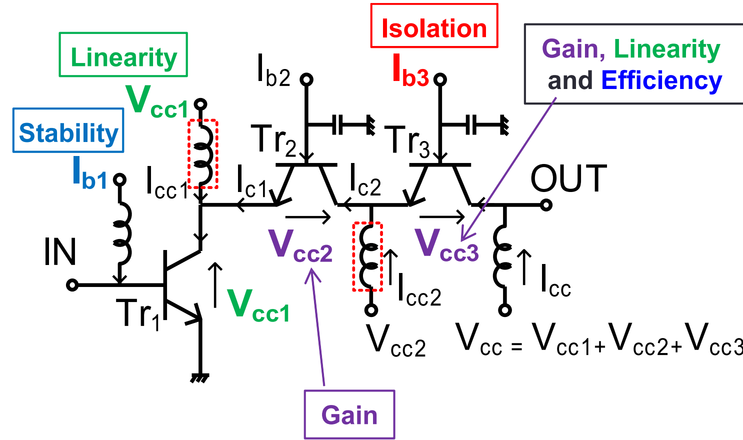


Figure 4.21: Summary of small-signal and large-signal performances improvement under bias parameters variation.

Table 4.3: Megtron6 substrate information.

Substrate thickness	**Conductor thickness**	**Dielectric constant**	**Dielectric loss tangent**
0.75 mm	35 μm	3.7	0.002

off to realize an optimum performance by setting appropriate bias condition independently for each transistor thanks to the advantage of independently biased feature. In details, stability and isolation can be improved mainly by changing the first stage base bias current (I_{b1}) and the third stage base bias current (I_{b1}), respectively whereas power gain and linearity can be improved by adjusting the first stage collector bias voltage (V_{cc1}) and the second stage collector bias voltage (V_{cc2}), respectively. The third stage collector bias voltage is the most important bias parameter since it contributes to the improvement of the power gain, linearity and efficiency. With this taken into account, an optimum performance of both small-signal and large-signal for the fabricated amplifier can be archived and shown in the next section.

4.2. Microwave performance investigation of independently biased 3-stack InGaP/GaAs HBT configuration

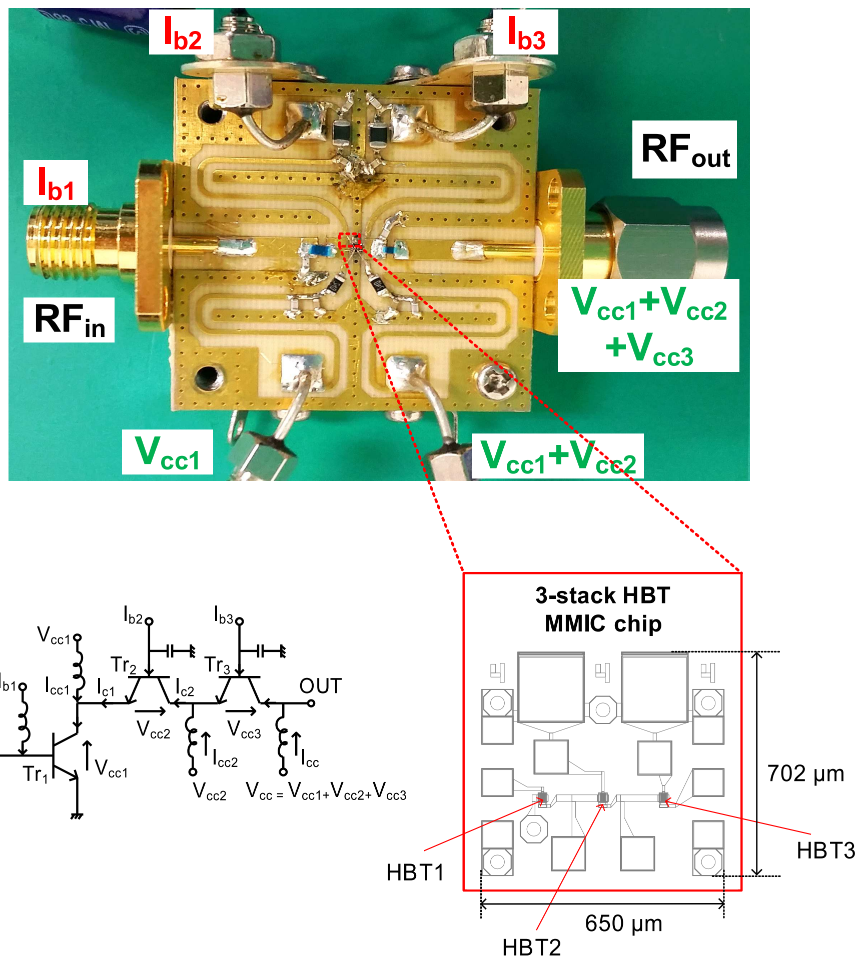


Figure 4.22: Fabricated 3-stack HBT MMIC chip based amplifier.

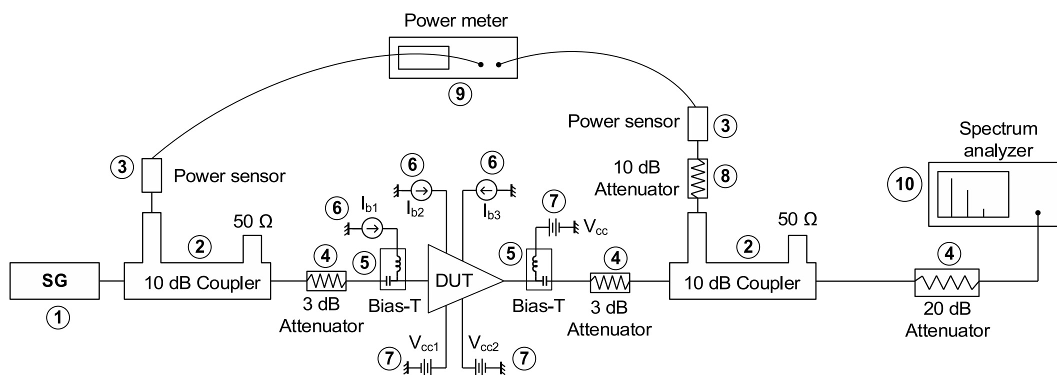


Figure 4.23: Experimental setup for one-tone signal measurement (gain and efficiency).

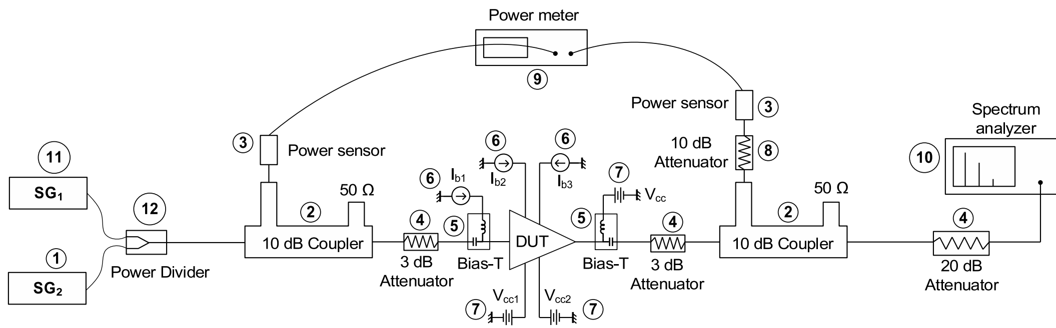


Figure 4.24: Experimental setup for two-tone signal or distortion (IMD3) measurement.

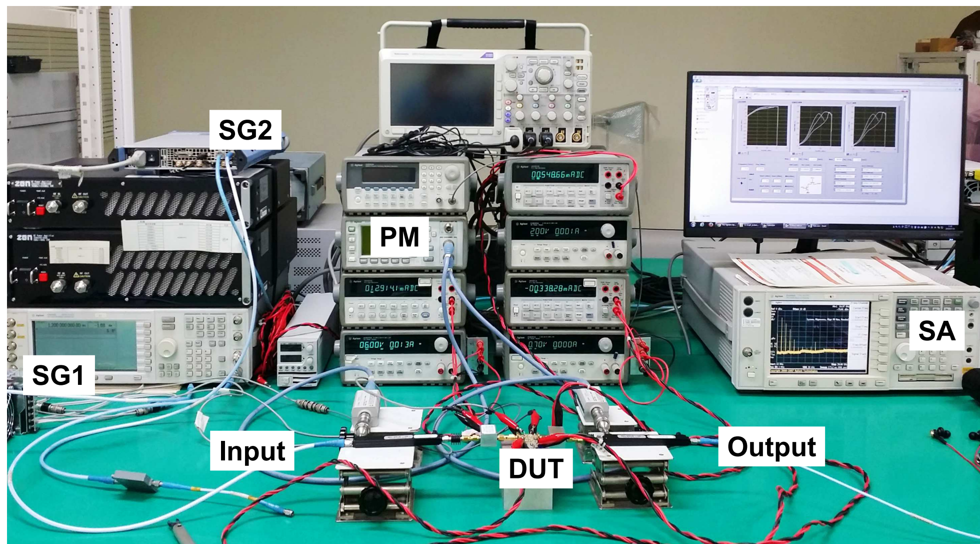


Figure 4.25: Realistic experimental setup for measurement of the fabricated amplifier.

4.2.2.2 Measured results

The fabricated 3-stack HBT MMIC chip based amplifier are shown on Fig. 4.22. It was fabricated on a Megtron6 substrate from Panasonic with the information is given in table 4.3 and the MMIC chip was made using foundry service from the WIN Semiconductor Corp. In the experiment, the large-signal characteristics including power gain, efficiency (PAE) and distortion (IMD3) are measured based on the bias investigation from measured small-signal characteristics as well as from simulated large-signal performances.

Table 4.4: List of instruments used for measurement of the fabricated amplifier.

Symbol	Instrument company	Instrument name
1	Agilent Technologies	E4438C ESG Vector Signal Generator
2	Fairview Microwave	MC0512-10 10 dB Directional Coupler
3	Agilent Technologies	E9300A E-Series Avg Power Sensor
4	Aeroflex/Inmet	18B5W-03 (5W, DC-18 GHz, 3dB ATT)
5	Aeroflex/Inmet	88008FF1-12 (2.5A Max. Bias-T)
6	Agilent Technologies	E5270A 8 Slot Parametric Measurement Mainframe
7	Agilent Technologies	E3645A 0-35V, 2.2A DC Power Supply
8	Aeroflex/Inmet	18B5W-10 (5W, DC-18 GHz, 10dB ATT)
9	Agilent Technologies	E4417A EPM-P Series Dual Channel Power Meter
10	Agilent Technologies	E4440A PSA Series Spectrum Analyzer
11	Rohde & Schwarz	R&S SGS 100A 6 GHz CW RF Source
12	MCLI	PS2-4 1836 (0.5-2.5 GHz) Power divider

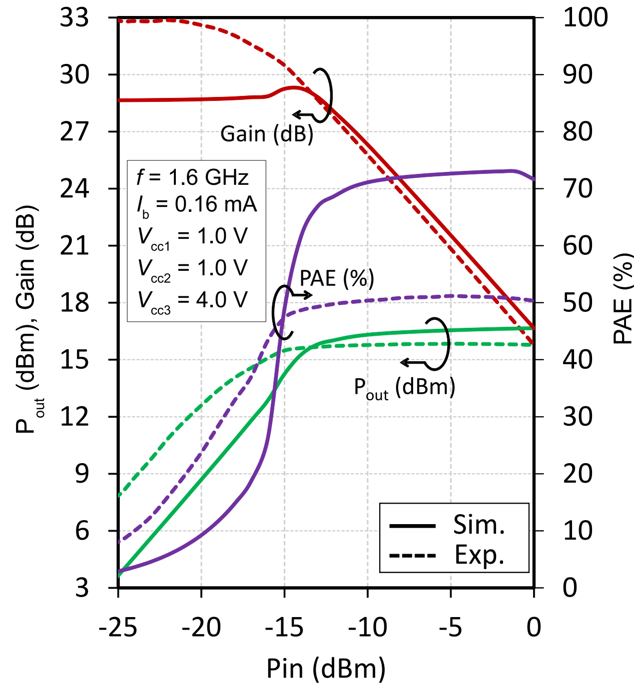


Figure 4.26: Measured results for the one-tone signal of gain and efficiency of the amplifier. Simulated results are also shown for comparison.

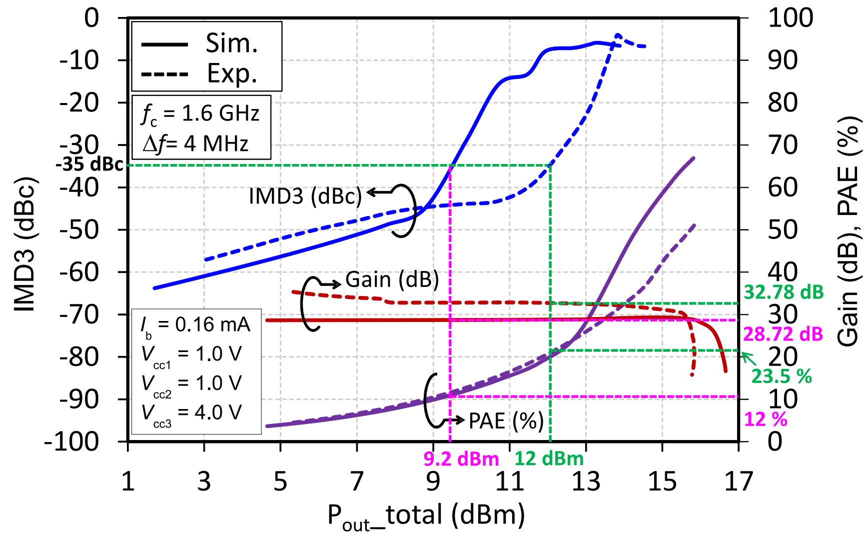


Figure 4.27: Measured results for two-tone signal (distortion) and one-tone signal (gain and efficiency) of the fabricated amplifier. The simulated results are also shown.

Table 4.5: Summary of the simulated and measured optimum performance for comparison.

Simulation				Measurement			
IMD3 (dBc)	PAE (%)	P_{out} (dBm)	Gain (dB)	IMD3 (dBc)	PAE (%)	P_{out} (dBm)	Gain (dB)
-35.0	12.0	9.2	28.7	-35.0	23.5	12.0	32.8

Figures 4.23 and Fig. 4.24 show the experimental setup for one-tone signal (gain and PAE) and two-tone signal (distortion or IMD3) measurement at operating frequency of 1.6 GHz, respectively whereas the realistic experimental setup is illustrated in Fig. 4.25. Here the instruments used for the measurement are described in details in table 4.4. Now it is necessary to consider the bias conditions investigation as shown in table 4.1 and table 4.2 to obtain the optimum bias conditions for the amplifier. The base bias currents for the three transistors are set to be the same and at a low value of 0.16 mA to make the

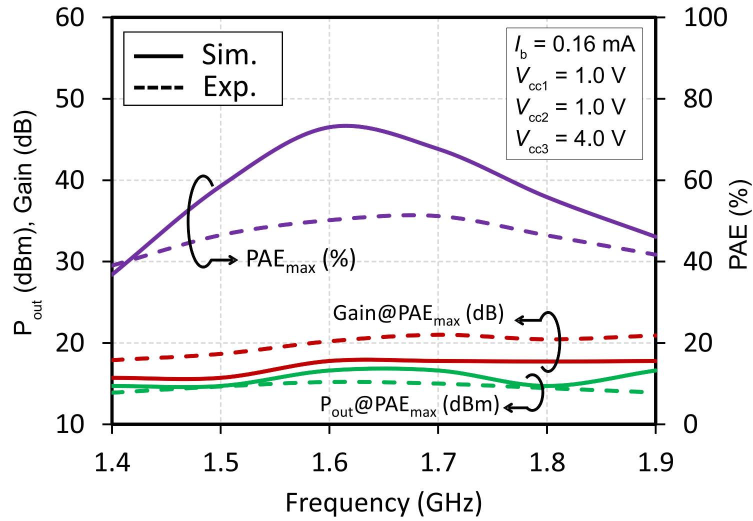


Figure 4.28: Frequency characteristic of the fabricated amplifier. Simulated results are also shown.

amplifier more stable as demonstrated in table 4.1. Moreover, from table 4.2 since V_{cc1} contributes to IMD3 improvement whereas it has no influence on the small-signal performance as can be seen in table 4.1, V_{cc1} is also set at a low value of 1.0 V for better IMD3 performance. According to the table 4.2, although V_{cc2} doesn't contribute to the large-signal performance enhancement, it should be also set at a low value for a better small-signal power gain as shown in table 4.1. Finally, according to both table 4.1 and table 4.2, V_{cc3} should be set at a high value in order to get better IMD3 as well as isolation and small-signal gain. In conclusion, by setting such a bias condition, the fabricated amplifier is expected to deliver high stability, high gain, high isolation and especially high linearity (or low IMD3).

The measured results for one-tone signal performance of the fabricated amplifier with the optimum bias condition are shown in Fig. 4.26. We can see on the figure that when input power varies from -25 dBm to 0 dBm, the amplifier can deliver a maximum efficiency of 51.2 % at output power of 15.84 dBm and power gain of 20.84 dB. It is also indicated on the figure that in the back-off region, power gain of the amplifier is still very high. These results

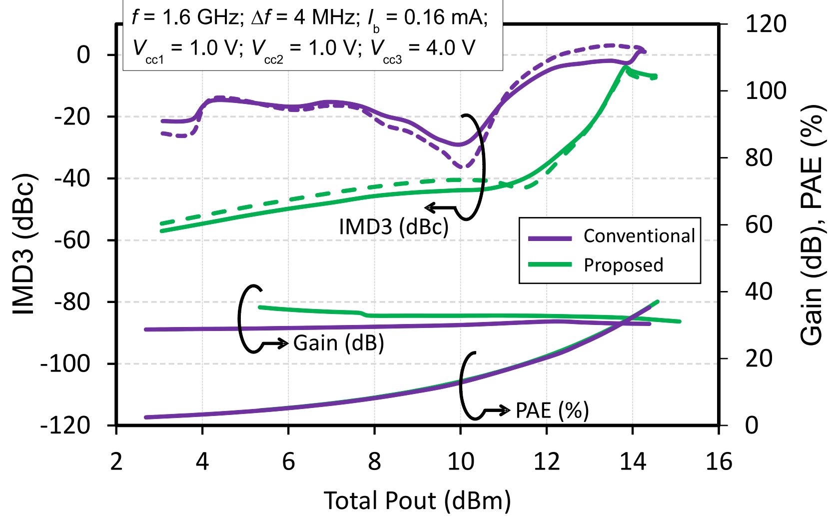


Figure 4.29: Comparison in distortion, power gain and efficiency performances between independently biased 3-stack amplifier and a conventional one.

have demonstrated for our above conclusion about the optimum bias condition on power gain. In addition to the one-tone signal results, the two-tone signal performance (IMD3) was also measured as indicated on Fig. 4.27. Here the center frequency is 1.6 GHz and the frequency spacing is 4 MHz. The bias condition for the amplifier is established the same as that of one-tone signal measurement. We can see that the amplifier exhibits a better IMD3 below -35 dBc at output power of 12 dBm and the efficiency of 23.5 %. This proves the fact that the amplifier exhibits low distortion or high linearity characteristic as expected. The optimum performances at optimum bias condition for both simulation and measurement are summarized in table 4.5 for comparison. From the table it can be seen that the measured results are slightly better than that of the simulated results.

Finally, the frequency characteristic of the fabricated amplifier is given in Fig. 4.28 along with the simulated result. The figure shows that within the bandwidth of 500 MHz (from 1.4 GHz to 1.9 GHz) and at the maximum efficiency (PAE), the amplifier exhibits a high power gain from 17.89 dB to 21.01 dB. This means high gain is one of the dominant advantages of the fabricated amplifier.

- Comparison with a conventional 3-stack HBT amplifier.

To validate the superior performance of the proposed configuration, its performance is compared with that of a conventional 3-stack amplifier as shown in Fig. 4.29. The so-called conventional amplifier is realized from the independently biased 3-stack (proposed) amplifier by disconnecting its two added bias terminals. Here, for a logical comparison, the frequency and bias condition are set the same for both the amplifiers as also given in the figure. As can be seen in the figure that the proposed amplifier exhibits significantly better IMD3 and power gain at the same efficiency. This means the proposed 3-stack configuration can deliver better performances not only in small-signal level but also in large-signal level compared to that of the conventional one.

4.2.3 Conclusion

In this section, a new novel circuit construction is proposed namely independently biased 3-stack HBT configuration and this new construction has been investigated for the small-signal and large-signal characteristics including stability, isolation, power gain and linearity by both the simulation and experiment. Furthermore its small-signal and large-signal performances were compared with that of a conventional configuration. For small-signal characteristic investigation, an MMIC chip was measured whereas for the large-signal characteristic investigation, a fabricated amplifier which is based on the MMIC chip was measured. All the simulated as well as measured results show that thanks to the advantage of the two added bias terminals, the proposed construction can deliver not only high stability, high isolation but also good power gain and linearity if the bias condition is established appropriately. An optimum performance at operation frequency of 1.6 GHz for both superior power gain and low distortion of this type of configuration was archived as: PAE = 23.5 %, P_{out} = 12 dBm; Gain = 32.6 dB at IMD3 = -35 dBc. Both small-signal and large-signal of the proposed configuration has been also shown better than that of a conventional configuration.

4.3 Microwave performance investigation of independently biased 3-stack GaN HEMT configuration

4.3.1 Introduction

If the previous section studies power gain and other RF characteristics such as linearity of the independently bias 3-stack InGaAs/GaAs HBT, in this section microwave performances of a power amplifier which is based on an independently biased 3-stack GaN HEMT MMIC chip at an operation frequency of 2.1 GHz is studied. Taking the advantage of the independently biased feature, the proposed amplifier is expected to deliver a good trade off of high output power, high gain and high efficiency at low distortion level. The schematic circuit for the amplifier is illustrated in Fig. 4.30. As can be seen in the figure, the independently biased 3-stack GaN HEMT structure has two additional bias terminals which are inserted into the mid-point between the drain of the first HEMT and the source of the second HEMT, and between the drain of the second HEMT and the source of the third HEMT. This method is the same one used in the independently biased 3-stack HBT structure. This also makes the 3-stack HEMT to be able to adjust bias condition for each transistor, resulting in superior performance.

4.3.2 Investigation of large-signal characteristics

In this section, large-signal characteristics of the 3-stack GaN HEMT amplifier including power gain, output power, efficiency and distortion will be investigated by considering the variation of bias parameters.

The circuit of the amplifier in Fig. 4.30 which is realized for simulation using Agilent ADS simulator is shown in Fig. 4.31. Here the input matching network (IMN) is treated up to second harmonic for obtaining high efficiency. Both IMN and output matching network (OMN) are formed from lumped chip components of Murata series. The component values of IMN used for simula-

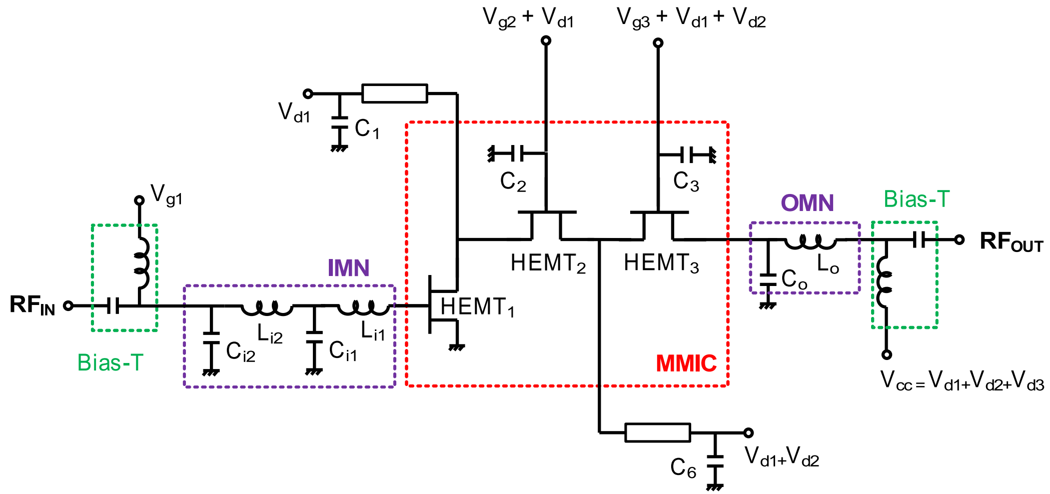


Figure 4.30: The independently biased 3-stack GaN HEMT amplifier circuit with incorporating input and output matching networks for realization of high efficiency.

tion are:

$L_{\mathrm{i1}} = 4.3$ nH.

$C_{\mathrm{i1}} = 0.9$ pF.

$L_{\mathrm{i2}} = 7.5$ nH.

$C_{\mathrm{i2}} = 2.4$ pF.

The component values of OMN are:

$L_{\mathrm{o}} = 12$ nH.

$C_{\mathrm{o}} = 0.3$ pF.

4.3.2.1 Effect of the gate bias voltage

The effect of the gate bias parameters V_{g1}, V_{g2}, and V_{g3} on output power, power gain and efficiency (PAE) are shown in Fig. 4.32. It can be seen in the figure that when the gate bias varies from −2.8 V to −2.4 V, the gate bias of the first transistor was found to the the most effective one contributing to the improvement of the power gain as well as PAE at low input power level. Gate bias of the second and third transistor seems not to affect to power gain efficiency performance of the amplifier.

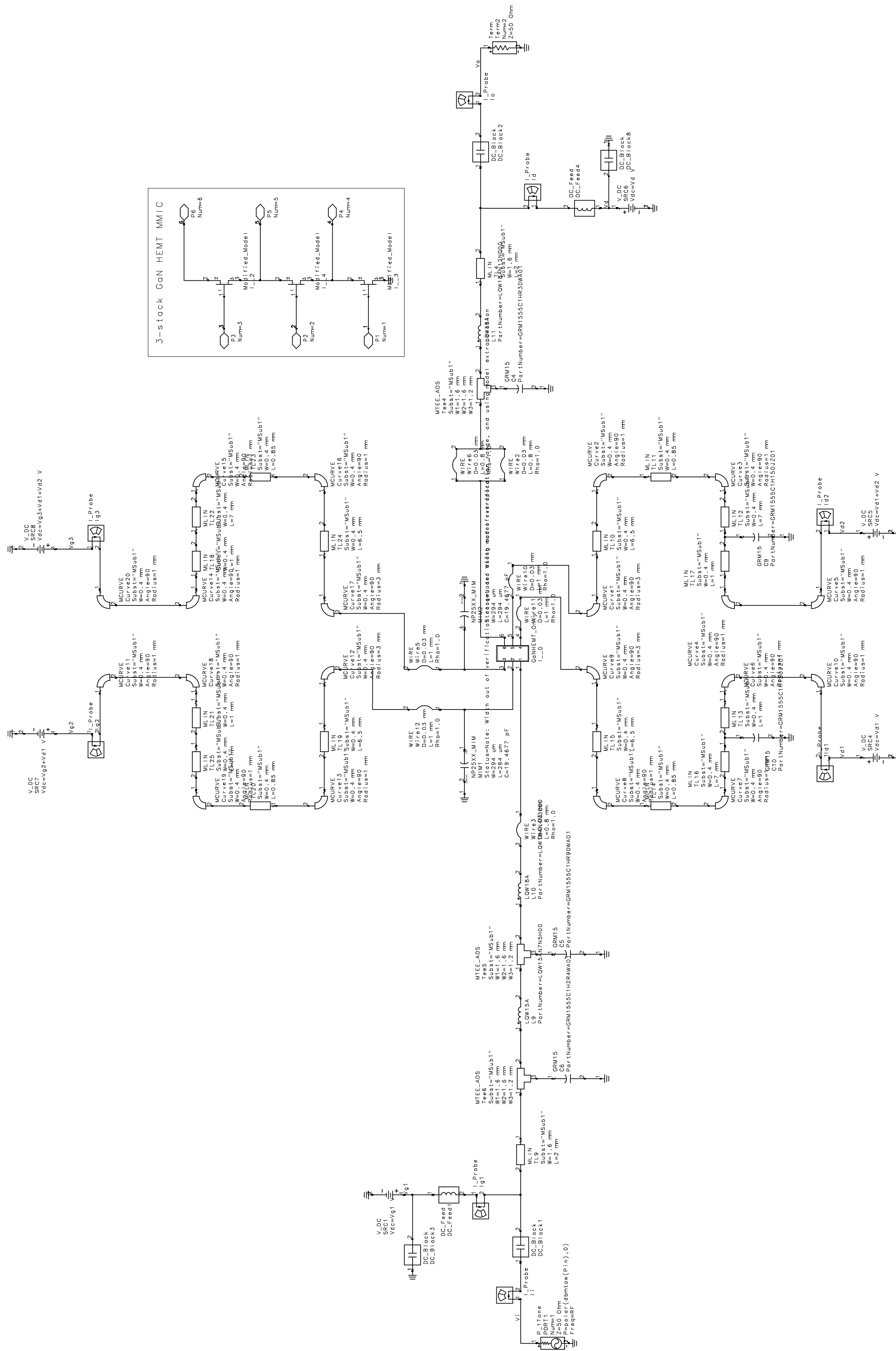


Figure 4.31: The ADS schematic of the independently biased 3-stack GaN HEMT MMIC chip based amplifier for simulation.

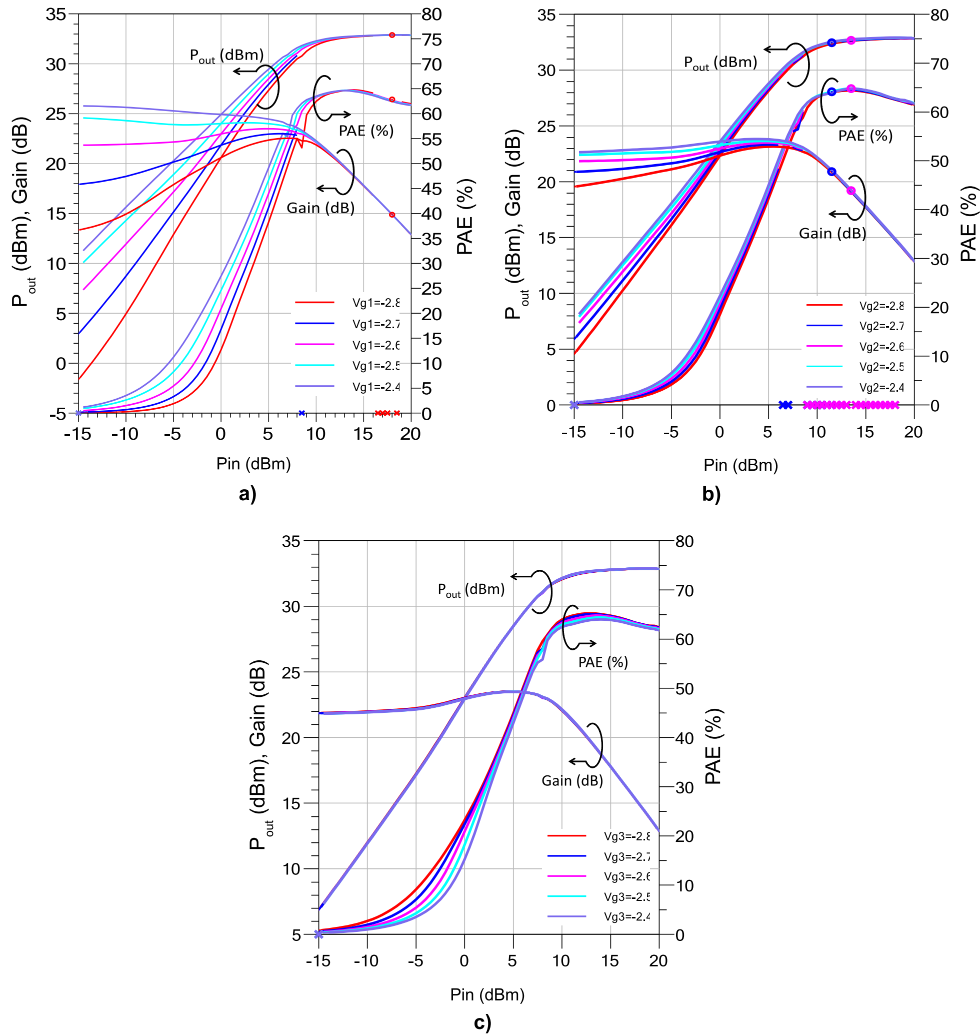


Figure 4.32: Dependence of output power, power gain and PAE for one-tone signal on the variation of the gate bias. Other bias values are: V_{g}= -2.6 V; V_{d1}= 5.0 V; V_{d2} = 4.0 V; V_{d} = 44.0 V

In addition to the power and efficiency performance, the distortion characteristic (IMD3) has been also investigated under the effect of gate bias. The simulated results are given in Fig. 4.33. In this investigation, V_{g1} and V_{g2} are the two effective factors contributing to the improvement of IMD3. In more detailed, V_{g1} and V_{g2} should be set at a high value of -2.5 V to realize better dynamic range, suppression of sweet point as well as lower IMD3. V_{g3} doesn't affect the improvement of IMD3.

Figure 4.34 describes the simultaneous dependence of IMD3 and PAE perfor-

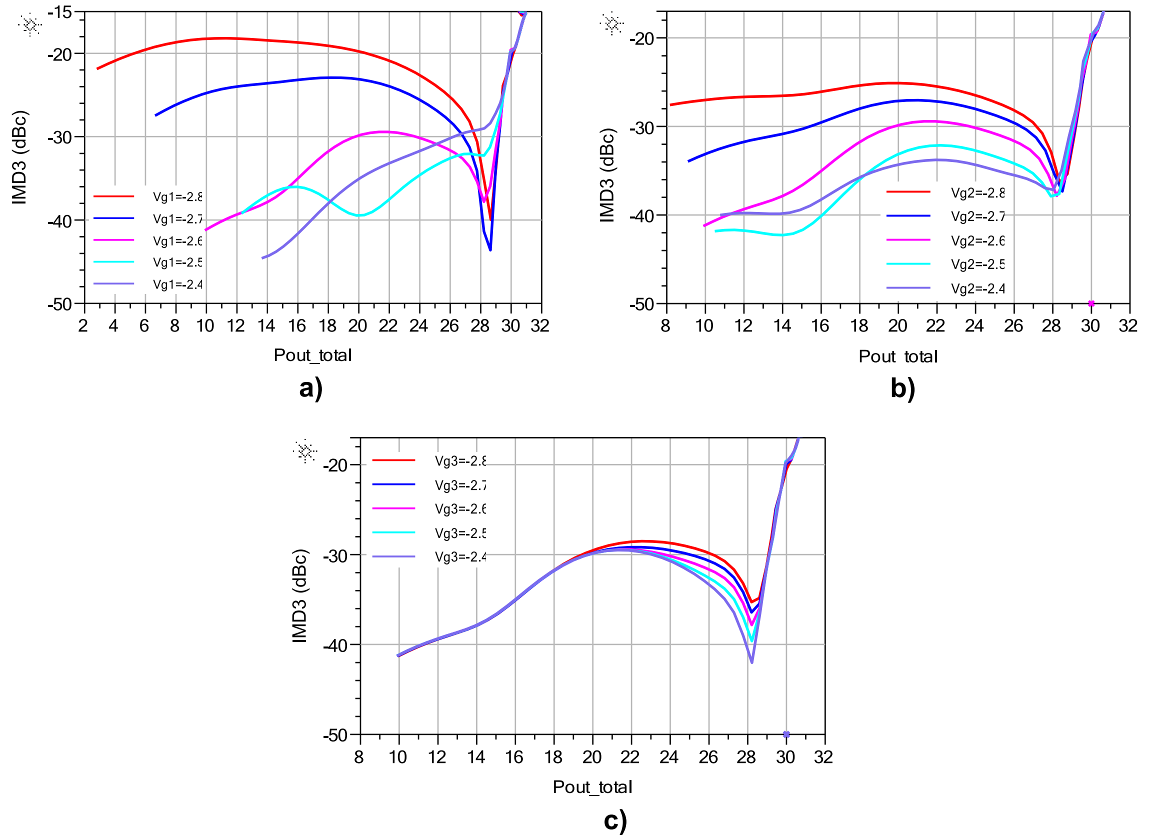


Figure 4.33: Dependence of IMD3 characteristic for two-tone signal on the variation of the gate bias. Other bias values are: V_g= -2.6 V; V_{d1}= 5.0 V; V_{d2} = 4.0 V; V_d = 44.0 V

mance of the amplifier on the gate bias variation. From this figure, we can make a trade off in the improvement of both IMD3 and PAE with respect to the gate bias change. V_{g1} and V_{g2} are two important bias parameters to be consider for this trade off and V_{g1} seems to be the most effective one for performance improvement. It was found that the best performance for both PAE and IMD3 can be obtained if V_{g1} is set at a value of -2.5 V. Finally by setting the optimum bias conditions for the gate bias, best performance of the amplifier is: at IMD3 = -32.22 dBc; PAE = 41.48 %, P_{out} = 27.85 dBm; Gain = 22.43 dB.

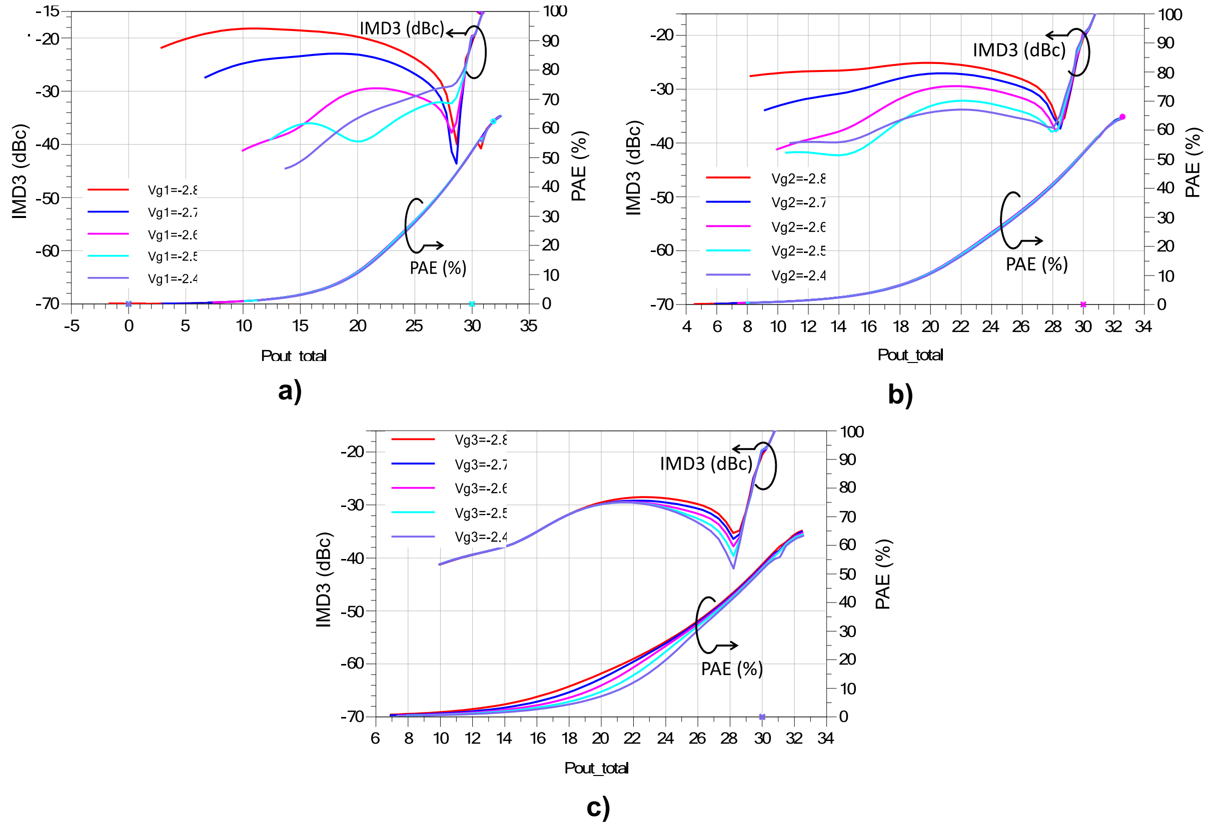


Figure 4.34: Dependence of simultaneous PAE and IMD3 characteristics on the variation of the gate bias. Other bias values are: V_{g}= -2.6 V; V_{d1}= 5.0 V; V_{d2} = 4.0 V; V_{d} = 44.0 V

4.3.2.2 Effect of the drain bias voltage

Effect of the drain bias voltages V_{d1}, V_{d2} and V_{d3} on the amplifier's power and efficiency performance is given in Fig. 4.35. The Fig. 4.35a shows that drain bias voltage of the first transistor V_{d1} slightly contributes to PAE and power performance and it should increase to enhance these performances. In contrast to the contribution of V_{d1}, V_{d2} and V_{d3} don't show any effect in the performance improvement as illustrated in Fig. 4.35b and Fig. 4.35c.

In Fig. 4.36a which shows the effect of the drain bias on IMD3 performance, we can once again see that V_{d1} is still the main factor of IMD3 improvement and its optimum value is 6.0 V. At this optimum value, IMD3 can be reduced and the sweet point can be suppressed. In Fig. 4.36b and Fig. 4.36c, no

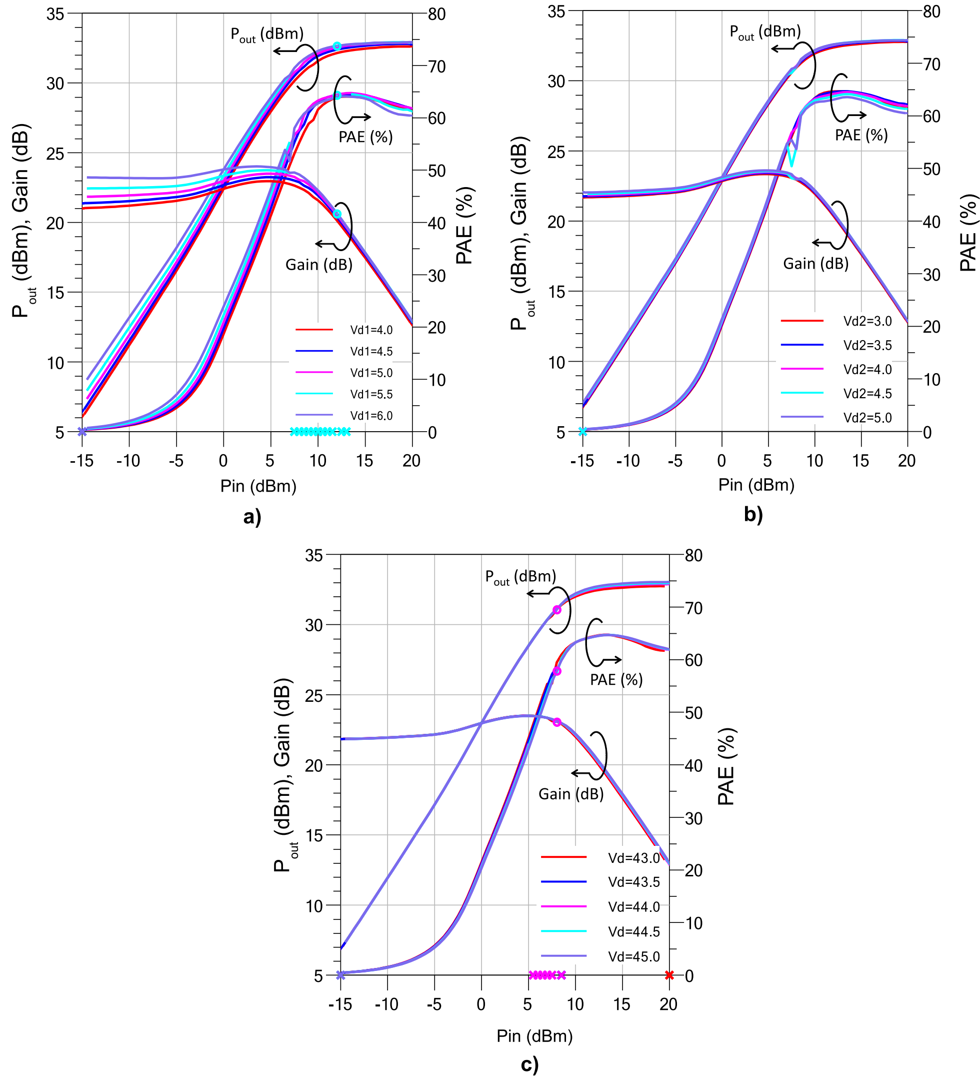


Figure 4.35: Dependence of output power, power gain and PAE for one-tone signal on the variation of the drain bias. Other bias values are: V_g= -2.6 V; V_{d1}= 5.0 V; V_{d2} = 4.0 V; V_d = 44.0 V

effective contribution of V_{d2} and V_{d3} to IMD3 performance can be observed. Finally the simultaneous dependence of PAE and IMD3 on the drain bias is given in Fig. 4.37. It is observed that optimum PAE and IMD3 can be obtained by adjusting V_{d1} since it affects significantly IMD3 characteristic and a little the PAE. The optimum value for V_{d1} to realize a good trade off of PAE and IMD3 is 6.0 V. At this optimum value, performance of the amplifier is: at IMD3 = -32.34 dBc; PAE = 46.45 %, P_{out} = 28.82 dBm; Gain =

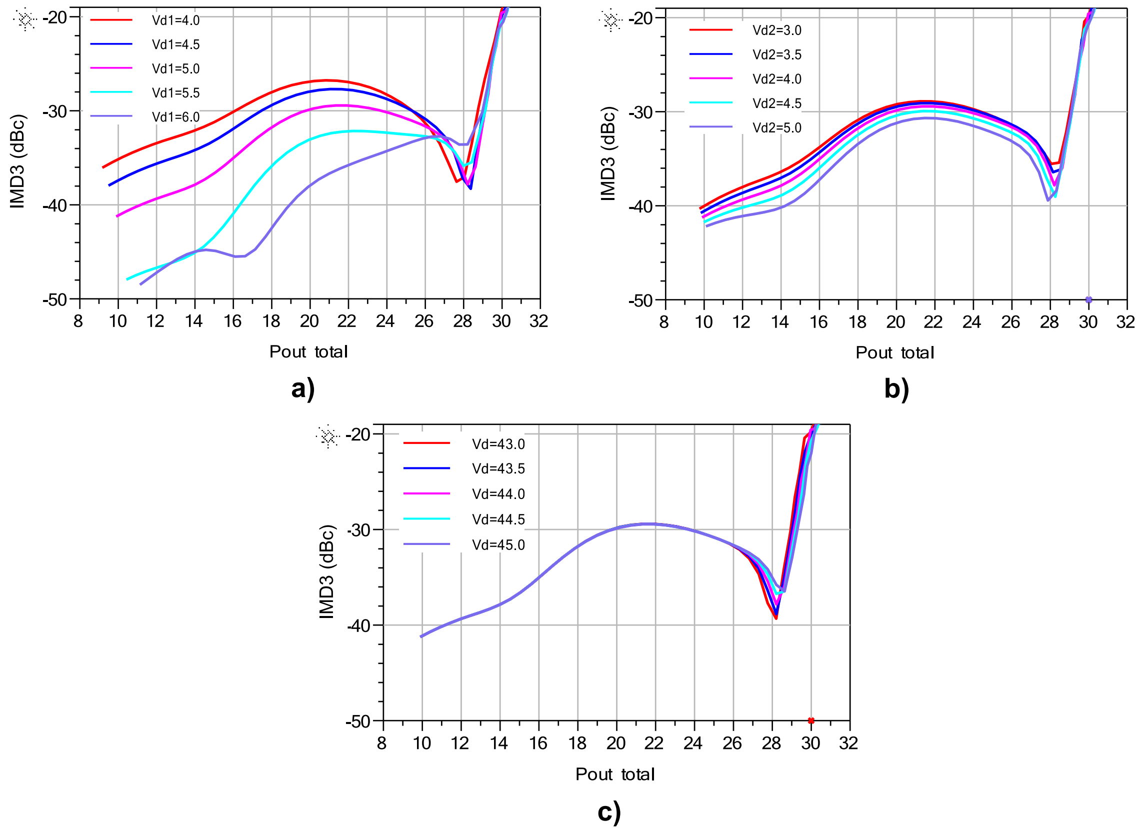


Figure 4.36: Dependence of IMD3 characteristic for two-tone signal on the variation of the drain bias. Other bias values are: V_{g} = -2.6 V; V_{d1} = 5.0 V; V_{d2} = 4.0 V; V_{d} = 44.0 V

23.96 dB. It is obvious that compared with the optimum V_{g1}, optimum V_{g1} contributes a better performance improvement for PAE, output power, power gain as well as IMD3. Consequently V_{d1} may be considered as the key factor for the performance enhancement of the independently biased 3-stack GaN HEMT amplifier.

Up to the time of finishing this thesis, performance of the amplifier has just been investigated by simulation. In the very near future the above simulated results will be soon confirmed by the measured results of a fabricated amplifier as shown in Fig. 4.38. In the figure, 3-stack GaN HEMT MMIC chip was fabricated using foundry service by the WIN Semiconductor Inc.. Moreover, IMN and OMN was realized using chip inductors and capacitors from Murata.

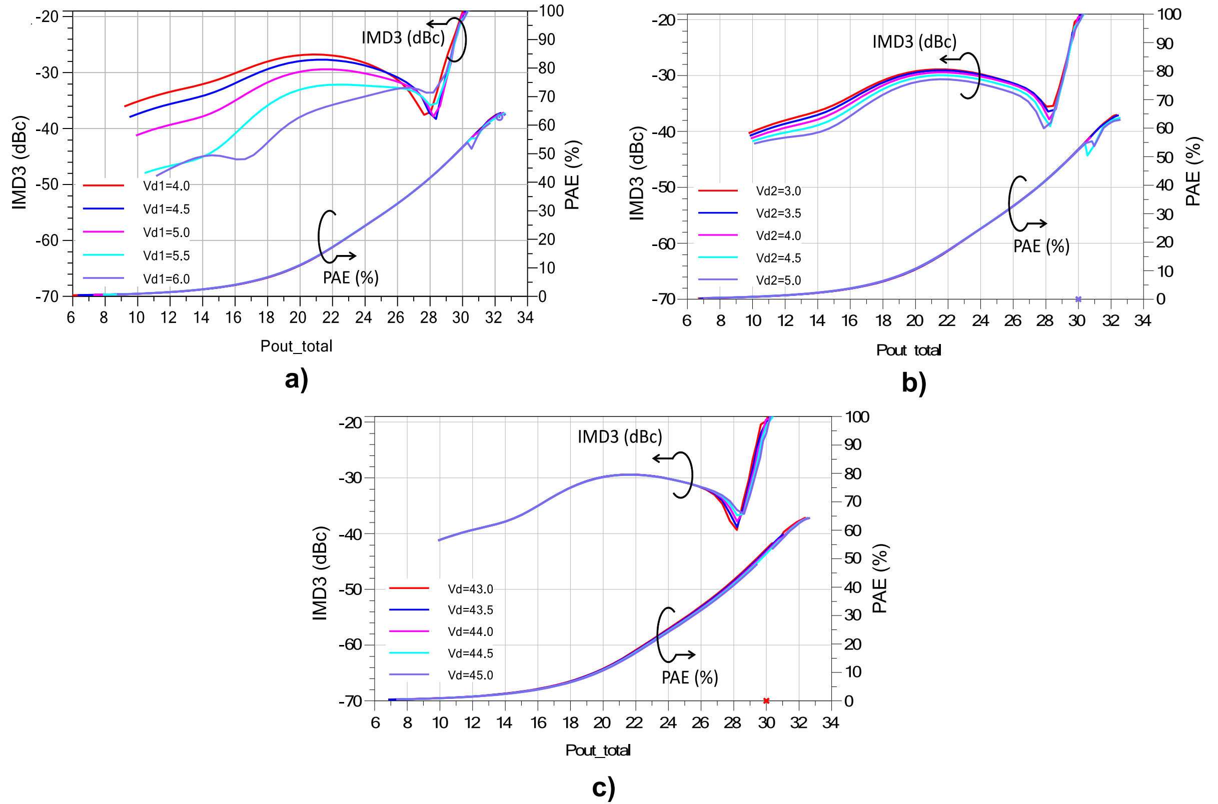


Figure 4.37: Dependence of simultaneous PAE and IMD3 characteristics on the variation of the drain bias voltages. Other bias values are: V_{g} = -2.6 V; V_{d1} = 5.0 V; V_{d2} = 4.0 V; V_{d} = 44.0 V

4.3.3 Conclusion

In this section, performances of independently biased 3-stack GaN HEMT amplifier has been investigated by simulation using the Agilent ADS simulator. It was found that the gate bias of the first transistor V_{g1} and its drain bias V_{d1} are the main factors affecting the amplifier performances including power gain, output power, efficiency and linearity. Compared with V_{g1}, the contribution of V_{d1} to performance improvement is more effective at its optimum value is of 6.0 V. If this optimum bias value is set, the amplifier can deliver a superior optimum performance as: PAE = 46.45 %, $\mathrm{P_{out}}$ = 28.82 dBm; Gain = 23.96 dB at IMD3 = -32.34 dBc.

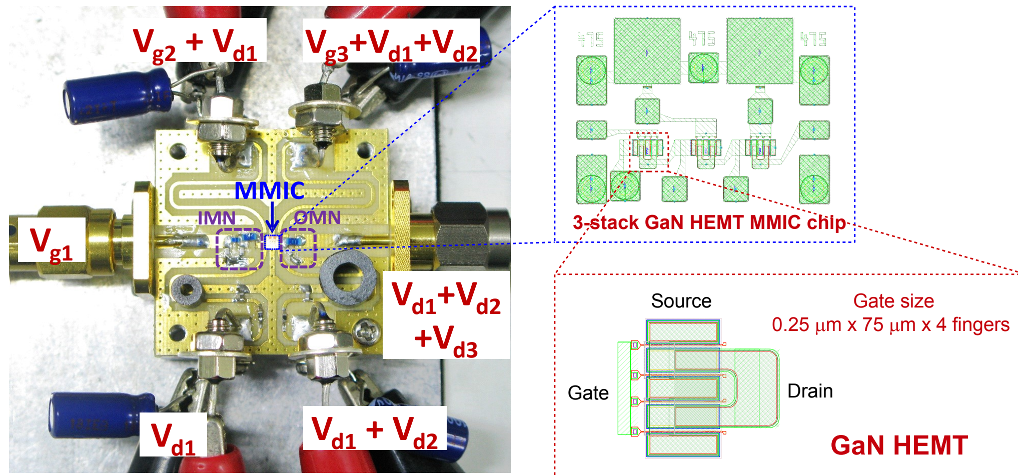


Figure 4.38: Fabricated independently biased 3-stack GaN HEMT power amplifier. The amplifier was fabricated based on the independently biased 3-stack GaN HEMT chip including 3 transistors with the same size of 0.25 μm $\times$ 75 μm $\times$ 4 fingers.

4.4 Summary

This chapter has studied the microwave performances including high frequency power gain, efficiency, linearity, isolation and stability of the 3-stack InGaP/GaAs HBT and GaN HEMT configurations by investigating the benefits from the independently biased functionality. Various bias scenarios for both configurations has been considered to realize the best trade off of the performances. It was found that by independent appropriately controlling the bias condition for individual transistor, the 3-stack HBT configuration could offer not only high power gain but also low distortion, high stability, high isolation performances. It shows a higher MSG compared to the Independently Biased CC and Conventional CC, under the same bias condition, 19.4 dB and 24.0 dB respectively and a higher MAG than Independently Biased CC and Conventional CC 6.4 dB and 8.0 dB respectively. In addition to power gain, it also exhibits higher isolation than Independently Biased CC and Conventional CC by maximum values of 33.2 dB and 41.8 dB respectively. Moreover, when compared to the

conventional 3-stack HBT, it still offers higher power gain and isolation by maximum 15 dB and 39 dB respectively. Besides these, the optimum large-signal for high power gain and low distortion was archived as: PAE = 23.5 %, P_{out} = 12 dBm; Gain = 32.6 dB at IMD3 = -35 dBc. The 3-stack GaN HEMT could deliver not only high output power but high efficiency and low distortion simultaneously with an optimum large-signal performance as: PAE = 46.45 %, P_{out} = 28.82 dBm; Gain = 23.96 dB at IMD3 = -32.34 dBc.

Chapter 5

Conclusions and future work

In this work, it was concluded that power gain mechanism and its improvement methods for not only conventional transistors but quantum devices remains consistent in that power gain of a device can be enhanced by the two key methods, the current transfer and resistance transfer. Using these methods, power gain mechanism of single electron transistor, a quantum device, was studied and its source junction thickness was found to be the key factor for its power gain improvement. By reducing the source junction thickness, power gain of SET can be significantly improved. This improved power gain can contribute to enhance the output current driving capability for SET in digital and logic applications. Moreover, the high cutoff frequency of SET points out that it can work as a ultra-high speed device. The potential future work for the research on power gain of quantum device is probably improving its small output power as well as the power gain by taking the benefit from multi-stage connection of SETs or hybrid connection of SETs and conventional transistors. Continuing with the method of power gain improvement, the independently biased InPGa/GaAs HBT cascode structure was proposed for power gain investigation based on the resistance transfer method, its power gain was found to be better than the conventional one by increasing its output resistance in term of controlling the collector current of the CB transistor. Besides the study of power gain improvement methods, the present work has also investigated the microwave performances of two novel independently biased

3-stack configurations namely 3-stack HBT and 3-stack HEMT by taking the advantage of the two added bias terminals for these configurations. Measured small-signal results for the independently biased 3-stack HBT configuration showed that by using the two added bias terminals for free bias setting, this configuration can deliver higher power gain, higher isolation compared with the conventional cascode and independently biased cascode as well as conventional 3-stack structures at frequency range of 1.5 GHz - 2.5 GHz. Moreover, the measured large-signal results indicated that at optimum bias condition, the amplifier could offer an optimum performance: PAE = 23.5 %, P_{out} = 12 dBm; Gain = 32.6 dB at IMD3 = -35 dBc. Its large-signal performance were also compared and shown better than that of a conventional structure. These results demonstrates the advantage of significant high gain and low distortion for the fabricated amplifier. For the independently biased 3-stack AlGaN/GaN HEMT cascode structure, the simulated large-signal results were studied by investigating the various bias setting thanks to the independently biased control feature. It was concluded that its performances depended mostly on the drain bias voltage of the first-stage transistor. At the optimum value of this drain bias voltage, the amplifier could deliver an optimum performance at an operation frequency of 2.1 GHz as: PAE = 46.45 %, P_{out} = 28.82 dBm; Gain = 23.96 dB at IMD3 = -32.34 dBc.

List of publications

Journal papers

1. *Power gain improvement for single-electron transistors (SETs)*, **D.M. Luong**, and K. Honjo, Jpn. J. Appl. Phys. **53**, 04EJ03, p.1-5, (2014).

2. *Power gain performance enhancement of independently biased heterojunction bipolar transistor cascode chip*, **D.M. Luong**, Y. Takayama, R. Ishikawa, and K. Honjo, Jpn. J. Appl. Phys. **54**, 04DF11, p.1-8, (2015).

International conferences

1. *Power Gain Characteristic of Single-Electron Transistors (SETs)*, **D.M. Luong**, and K. Honjo, 2013 International Conference on Solid State Devices and Materials (SSDM), Fukuoka, Japan, p.302-303, (2013).

2. *Comparison of Power Gain Performance between Conventional and Independently Biased HBT Cascode Chips*, **D.M. Luong**, Y. Takayama, R. Ishikawa, and K. Honjo, 2014 International Conference on Solid State Devices and Materials (SSDM), Tsukuba, Japan, p.120-121, (2014).

3. *Power gain mechanism of single-electron transistor (SET) in comparison to that of heterojunction bipolar transistor (HBT)*, **D.M. Luong**, Y. Takayama, R. Ishikawa, and K. Honjo, 2015 Energy Materials Nanotechnology (EMN) Meeting on Vacuum Electronics, Las Vegas, NV USA, November 21-24, (2015) (Invited).

Domestic conferences

1. *Power Gain Characteristic of Independently Biased HBT Cascode Chip*, **D.M. Luong**, Y. Takayama, R. Ishikawa, and K. Honjo, 2014 IEICE General Conference, Niigata, Japan C-2-24, p. 54, (2014).

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