A STUDY ON ULTRA-LOW POWER AND HIGH SENSITIVITY CMOS RF RECEIVER FOR WIRELESS SENSOR NETWORKS

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Abstract

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Wireless sensor networks (WSN) have been applied in wide range of applications and proved the more and more important contribution in the modern life. In order to evaluate a WSN, many metrics are considered such as cost, latency, power or quality of service. However, since the sensor nodes are usually deployed in large physical areas and inaccessible locations, the battery change becomes impossible. In this scenario, the power consumption is the most important metric. In a sensor node, the RF receiver is one of the communication devices, which consume a vast majority of power. Therefore, this thesis studies ultra low power RF receivers for the long lifetime of the sensor nodes.

Currently, the WSNs use various frequency bands. However, for low power target, the sub-GHz frequency bands are preferred. In this study, ultra-low power 315 MHz and 920 MHz receivers will be proposed for short-range applications and long-range applications of the WSNs respectively.

To achieve ultra-low power target, the thesis considers some issues in architecture, circuit design and fabrication technology for suitable choices. After considering different receiver architectures, the RF detection receiver with the On-Off-Keying (OOK) modulation is chosen. Then the thesis proposes solutions to reduce power consumption and concurrently guarantee high sensitivity for the receivers so that they can communicate at adequate distances for both short and long-range applications.

First, a 920 MHz OOK receiver is designed for the long-range WSN applications. Typically, the RF amplifiers and local oscillators consume the most of power of RF

receivers. In the RF detection receivers, the local oscillators are eliminated, however, the power consumption of the RF amplifiers is still dominant. By reducing the RF gain or removing the RF amplifier, the power consumption of the receivers can be reduced drastically. However, in this case the sensitivity is very limited. In order to overcome the trade-off between power consumption and sensitivity, the switched bias is applied to the RF amplifiers to reduce their power consumption substantially while guaranteeing high RF gain before RF detection. As a result, the receiver consumes only 53 μW at 0.6 V supply with -82 dBm sensitivity at 10 kbps data rate.

Next, an OOK receiver operating at 315 MHz for the short-range WSN applications with low complexity is proposed. In this receiver, the RF amplifier is controlled to operate intermittently for power reduction. Furthermore, taking advantage of the low carrier frequency, a comparator is used to convert the RF signal to a rail-to-rail stream and then data is demodulated in the digital domain. Therefore, no envelope detector or baseband amplifier is required. The architecture of the receiver is verified by using discrete RF modules and FPGAs before it is designed on CMOS technology. By simulation with the physical layout, the 315 MHz OOK receiver consumes 27.6 μW at 200 kbps and achieves -76.4 dBm sensitivity.

Finally, the Synchronized-OOK (S-OOK) modulation scheme is proposed and then an S-OOK receiver operating in the 315 MHz frequency is developed to reduce power consumption more deeply. The S-OOK signal contains not only data but also clock information. By generating a narrow window, the RF front-end is enabled to receive signal only in a short period, therefore, power consumption of the receiver is reduced further. In addition, thank to the clock information contained in the input signal, the data and corresponding clock are demodulated simultaneously without a clock and data recovery circuit. The architecture of the S-OOK receiver is also verified by using discrete RF modules and FPGAs, then VLSI design is carried out. Physical layout

simulation shows that the receiver can achieve -76.4 dBm sensitivity, consumes 8.39 μW, 4.49 μW, 1.36 μW at 100 kbps, 50 kbps and 10 kbps respectively.

In conclusion, with the objective is to look for solutions to minimize power consumption of receivers for extending the lifetime of sensor nodes while guaranteeing high sensitivity, this study proposed novel receiver architectures, which help reduce power consumption significantly. If using the coin battery CR2032 for power supply, the 920 MHz OOK receiver can work continuously in 1.45 years with communication distance of 259 meters; the 315 MHz OOK receivers can work continuously in 2.8 years with approximately 19 meters communication distance in free space. Whereas, the 315 MHz S-OOK receiver with the minimum power consumption of 1.36 μW is suitable for batteryless sensor nodes.

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List of Abbreviations

ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
BAN	**B**ody **A**rea **N**etwork
BOX	**B**uried **OX**ide
BPF	**B**and-**P**ass **F**ilter
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
FPGA	**F**ield-**P**rogrammable **G**ate **A**rray
FD-SOI	**F**ully **D**epleted-SOI
GIDL	**G**ate-**I**nduced **D**rain **L**eakage
IF	**I**ntermediate **F**requency
IR-UWB	**I**mpulse **R**adio **U**ltra-**W**ide **B**and
LAN	**L**ocal **A**rea **N**etwork
LO	**L**ocal **O**scillator
LNA	**L**ow **N**oise **A**mplifier
LPF	**L**ow-**P**ass **F**ilter
OOK	**O**n-**O**ff **K**eying
RF	**R**adio **F**requency
SOI	**S**ilicon **O**n **I**nsulator
SOTB	**S**ilicon **O**n **T**hin **B**uried Oxide
S-OOK	**S**ynchronized-**O**n-**O**ff **K**eying
VLSI	**V**ery-**L**arge **S**caled **I**ntegration
WSN	**W**ireless **S**ensor **N**etwork

Chapter 1

Introduction

1.1 Motivation

1.1.1 Wireless Sensor Networks and Applications

Sensor networks are composed of groups of sensors, which collect data, process and transmit to users. The sensor networks have been researched and developed for a long time. The radar network used in air surveillance is one of the examples of the early sensor networks, in which each radar station is a sensor node. However, since sensor nodes at the beginning are large and high cost, the applications of the sensor networks are limited in some areas such as military or national power grid. Until recently, together with the development of sensing, wireless communication and computing technologies, wireless sensor networks (WSN) have become more popular. The appearance of low cost, small size sensors and advances of the communication technology allows us to develop the WSNs with large number of sensor nodes, bringing the WSNs into the life widely. Nowadays, the WSNs are deployed in the large range of applications and recognized as one of the most important technologies in the 21st century [1]. The WSNs can be used in Security, Field Area Networks (such as envi-

ronment monitoring, habitat monitoring, agriculture), Body Area Networks (BAN), In-Vehicle Networks, Home Automation, Industrial Monitoring and so on.

Security is one of the main applications of the WSNs. In order to protect critical infrastructure such as government buildings, public transportation, power supplies, banks, the WSNs are deployed to identify and prevent risks as soon as possible. Thieves or terrorist attacks, as well as failure caused by natural disasters, will be early detected and prevented, guaranteeing those facilities to be safe every time [2].

For the environment and habitat monitoring, the WSNs are deployed to monitor many parameters such as temperature or humidity. The collected data allows users to analyze accurately the changes of the environment or predict climate trends. The environment monitoring can be carried out to prevent forest fires, collect data of ecology systems or evaluate chemical pollution in an area.

In agriculture, the WSNs collect data related to temperature, light levels or soil moisture across a field for analysis. The analysis results help cultivate or harvest more precisely. The development of the WSNs also benefits aquaculture. Water quality parameters such as dissolved oxygen or pH are measured and a control mechanism is used to balance those parameters, keeping the water condition to be most appropriate for the growth of aquatic products.

Another crucial application of the WSNs is Home Automation. The WSNs make human's life more comfortable, help take care old people more convenient. The sensor nodes are deployed in the buildings at suitable locations to monitor temperature, humidity, light and then control air-conditioning, lighting and ventilating properly. The WSNs gather information on user behavior and his interaction with home appliances, automatically control home appliances according to users' habits. They help reduce energy consumption within the buildings and improve users' life quality.

The previous is some typical applications of the WSNs. Besides, the WSNs can be applied in many other areas such as healthcare, smart meter, telemetry. They have

brought considerable advances in many fields and played more and more important roles in the social life of human being.

1.1.2 Sensor Node Architecture

Figure 1.1 describes the architecture of a typical sensor node, including processing unit, RF transceiver, sensors/actuators and power supply [3, 4].

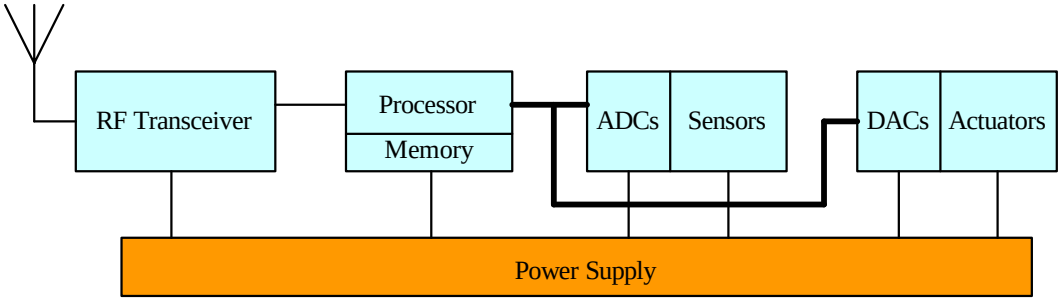

Figure 1.1: Architecture of a typical sensor node

The center of the wireless sensor node is the processing unit, which can be a microcontroller, FPGA or ASIC. It collects data from sensors, processes it and decides necessary operations of the actuators or the communication devices for sending to other nodes. The processing unit is usually connected to the sensors via Analog to Digital Converters (ADCs). The sensor senses necessary parameters depending on applications and converts those parameters to electrical signals (voltage or current), which are received by the processing unit through ADCs. The actuators are used to implement commands from the processing unit for completing a particular operation depending on the purpose of designing the WSN. For the actual communication, each sensor node needs a transmitter and a receiver to form wireless connections between nodes. The transmitter and receiver are usually combined in a single module called the transceiver. It receives digital data then converts to radio waves to transmit to other nodes or vice-versa. The power unit provides the electrical power needed by

the other units in the system. Since the power unit usually consists of batteries with a limited amount of energy available, therefore limiting the lifetime of the node.

1.1.3 Power Consumption of Sensor Node

In traditional sensor networks, the node energy supply is unlimited, the energy consumption is not the main problem for their applications. In WSN applications, a sensor node is equipped with a limited power source due to its hardware constraints. Furthermore, for most applications, the sensor nodes are deployed with a large number, in large areas or the inaccessible locations, replacement of power resources is impossible. In this scenario, the energy consumption becomes the core issue in WSN designs. For short-range applications such as wearable and implantable WSNs, the number is nodes is not so large. However, the volume and weight of the nodes are limited rigorously. The sensor nodes might be implanted in the human body. Hence, the battery replacement or recharging is very difficult. In this case, reducing power consumption is an essential requirement for longer battery lifetime or allowing to apply remote charging techniques.

A survey presented in [3] showed the relationship between computation and RF communication energy based on some typical sensor nodes (Table 1.1). It is clear that the energy required for RF communication is usually much larger than the energy for computation.

Table 1.1: Relationship between computation and RF communication energy in some typical sensor nodes

Node	**RF Energy / Comptation Energy**
Rockwell WINS	1500 to 2700
MEDUSA II	220 to 2900
WINS NG 2.0	1400
RFM TR1000	190

The work in [5] evaluated the influence of processor, transceiver and sensor to the overall energy consumption of a sensor node. Their experiment adopted MSP430f149 microprocessor, CC2420 communication module and DS18B20 temperature sensor. This experiment deploys 20 nodes with random distribution. The system tasks include sending data packets and maintaining routing protocol. The simulation time length is set to 300 s. The range of wireless communication is 200 meters. The energy consumption analysis is based on a node selected randomly. The result shows that the energy consumed by the RF transceiver is more than 77.5% of total energy consumption (Figure 1.2).

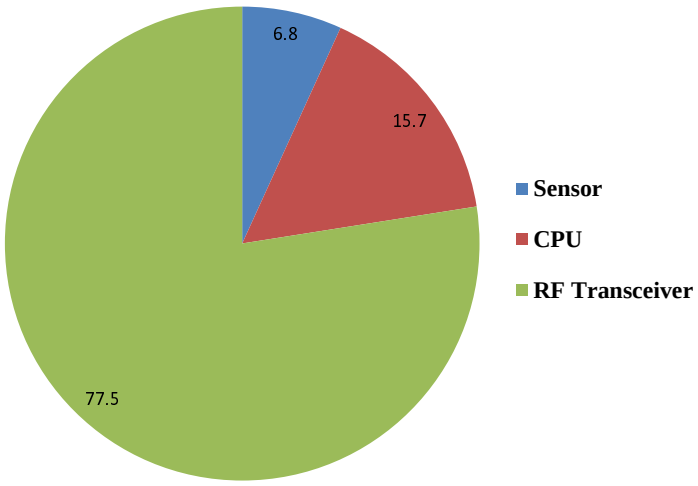

Figure 1.2: Energy consumption of a sensor node

We can see that in existing sensor nodes, the energy consumed by radio communication occupies a majority of node energy consumption. In order to extend the lifetime of the WSNs, reducing the power consumption of the RF transceivers is one of the most important issue.

An RF transceiver includes a transmitter and a receiver. The relationship between the power consumption of the transmitter and the receiver is dependent on the hardware platform. Intuitively, the active power of transmitters is usually higher than the active power of receivers [6, 7]. However, the transmission is a proactive

operation. While the reception is a passive one. It is easier to reduce the active time of transmitters than receivers. In addition, the active time of the transmitter and the receiver is strongly affected by the length and number of data packets. The receiver in a node receives data packets from many neighbor nodes after that the node decides to accept or discard the packets. Therefore, the number of the receiving packets is much greater than the number of the transmitting packets. Consequently, the average power consumption of the receivers is usually larger than that of the transmitters. Figure 1.3 shows power consumption of a RF transceiver in different states described in [5], in which TX, RX, Sleep, Idle, CCA, Tran are transmission, reception, sleep, idle, clear channel assessment and transition states respectively.

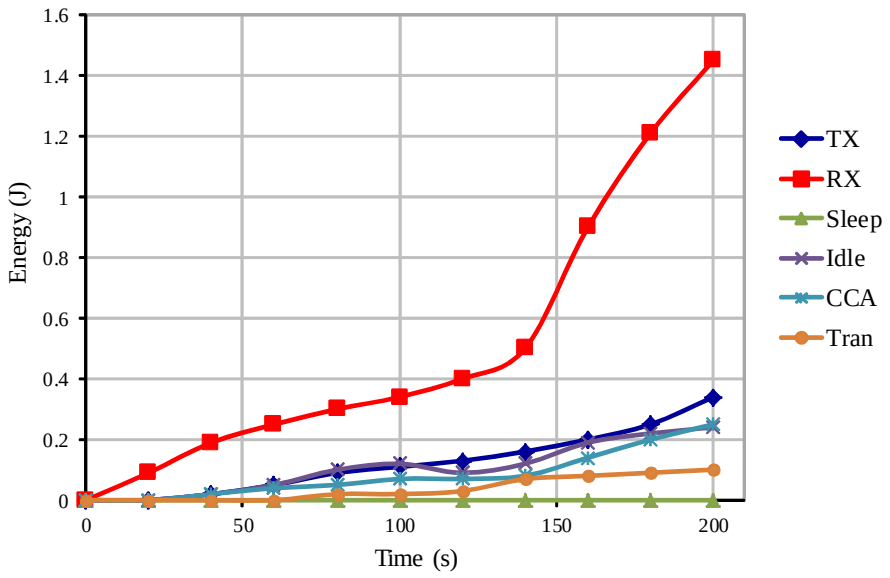

Figure 1.3: Energy consumption of the transceiver in different states

It can be seen, the energy consumed by the receiver is dominant, much greater than energy consumption of the transmitter. Therefore, reducing the power consumption of receivers has been paid the special attention when developing low power sensor nodes for long lifetime of the WSNs. In this study, ultra-low power receiver designs for the WSNs will be presented. New solutions and architectures will be proposed to minimize power consumption of the receivers.

1.2 Goals of This Study

The goal of this study is to design ultra-low power RF receivers for the WSNs. Main requirement is low power for long life battery even though in the case of continuous operation. This study will find out solutions to minimize power consumption of the receiver as possible.

The fundamental choice must be made during designing the receiver is the selection of the operating frequency. Currently, the WSNs use various frequency bands, including 315 MHz, 433 MHz, 868/915 MHz (Europe), 920 MHz (Japan) and 2.4 GHz bands. Table 1.2 lists some receivers common used in the commercial sensor nodes with their specifications at different frequencies [8]. Although commercial 2.4 GHz devices are popular in the market, providing implementation flexibility. However, using this band also brings out high possibility of interference, coming from WLAN 802.11b/g, WiMax, Bluetooth. Furthermore, for low power design, the sub-GHz frequency bands are preferred.

Table 1.2: The main specifications of several commercial RF receivers common used in WSN

Chip	**Frequency (MHz)**	**Data rate (kbps)**	**Power (mW)**	**Modulation**
TR1000	916.5	2.4-115.2	14.4	OOK/ASK
TRF6903	315/433/915	1-64	60	FSK/OOK
CC1000	315/433/916	2.4-76.8	30	FSK/OOK
CC2420	2400	250	33.8	O-QPSK
nRF905	433-915	100	37.5	GFSK
nRF2401	2400	0-1000	75	GFSK
9xStream	902-928	9.6-20	450	FSK
MAX7030	315/433	66	14	OOK/ASK

The applications of the WSNs can be divided into two groups according to the communication range. The long-range applications such as field area networks (environment and habitat monitoring, precise agriculture, marine monitoring) require

large number of nodes, spreading in a large area. Their receivers need to be able to communicate up to hundred meters for reducing the number of nodes [9]. The short-range applications include body area networks (BAN), heathcare, indoor monitoring, in-vehicle network, etc., which require only from a couple of meters to several tens meters of the communication distance [10, 11]. For ultra-low power, the 315 MHz band is the best choice. However, the transmitted power of this band is limited to -6 dBm (ARIB STD-T93 regulation of Japan), so that it can be used only for the short-range applications. The 433 MHz band is also dedicated to short-range devices with the maximum transmission power of 0 dBm. At the 920 MHz frequency band, the maximum output power is 250 mW (+24 dBm) according to the ARIB STD-T108 regulation. With this transmitted power, the receivers operating at 920 MHz can communicate at a distance up to hundreds meters or even several kilometers. Figure 1.4 shows the picture of transmission power, range of communication and typical applications versus frequency in the sub-GHz bands.

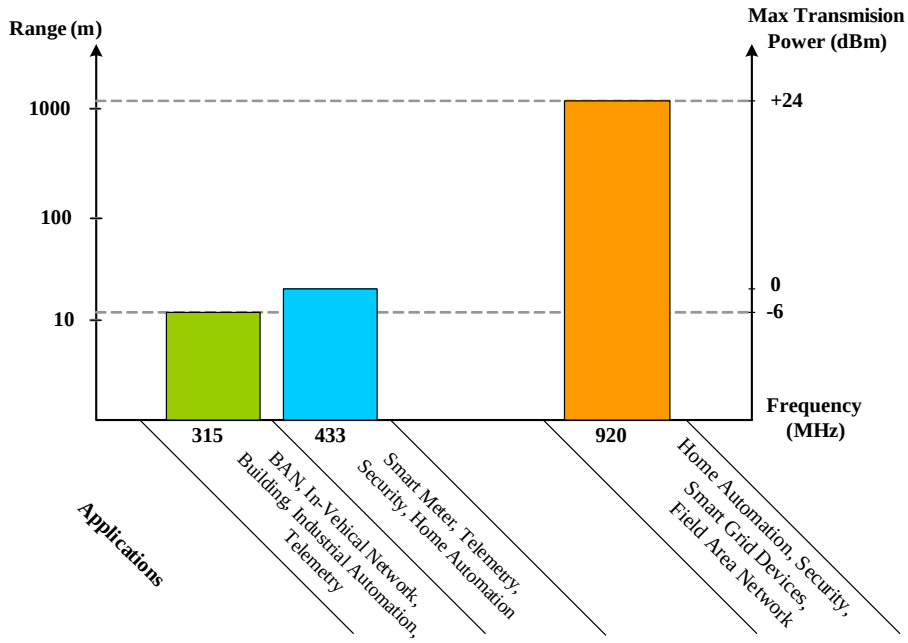

Figure 1.4: Picture on range of communication, maximum transmission power and typical applications in sub-GHz frequencies

In this study, both carrier frequencies 315 MHz and 920 MHz are used to design ultra-low power receivers for short-range and long-range applications of the WSNs. At those frequencies, the sensitivity must be better than -70 dBm to achieve the communication distance of 10 meters and more than 100 meters for 315 MHz and 920 MHz receiver respectively. The 433 MHz frequency is close to 315 MHz, so that the 315 MHz receiver architectures presented in this study can also be used for this band.

With the most WSN applications, the sensed parameters are slowly changing variables such as temperature, humidity, pressure, pH, etc. Therefore, the data rate requirement is usually low [4]. It can be seen from Table 1.2, with the receivers common used in the commercial sensor nodes, the data rate is usually in the range from 1 kbps to several hundreds kbps. In BAN sensors, the data rate is even required much lower, from tens bps to several kbps [11, 12]. However, in order to reduce latency of the system, the data rate is desired to be higher than 1 kbps. In this study, we define the data rate of the proposed receivers is in the range of 1 kbps - 200 kbps.

Assume that the coin battery CR2032 with the capacity of 675 mWh is used for power supply. The lowest power receiver in Table 1.2 can work continuously in only 48 hours (two days). In order to operate continuously at least 1 year without battery change, the power consumption of the receiver has to be lower than 77 μW. With short-range receivers operate at 315 MHz or 433 MHz, the power consumption can be reduced to be lower than that of 920 MHz receivers. In this study, the power target for 315 MHz receivers is 40 μW so that they can last several years. For batteryless sensors using energy harvesting, the required power consumption may be smaller than 10 μW so that the receiver can operate with energy harvested from human motion, human temperature or RF energy. Figure 1.5 shows a view of specifications of available receivers and targets of this study, together with the capability of energy harvesting from different sources [13].

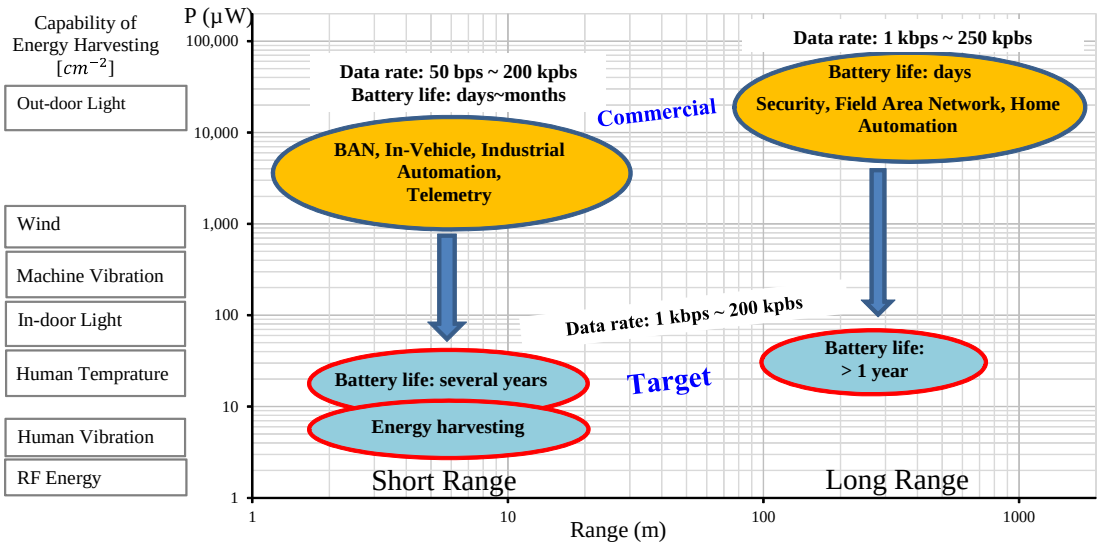

Figure 1.5: Overview of the study targets

In summary, the preliminary specifications of the target receivers are shown in Table1.3.

Table 1.3. The preliminary specifications of the target receivers

Specification	**Receiver in Chapter 3**	**Receiver in Chapter 4**	**Receiver in Chapter 5**
Carrier Freq. (MHz)	920	315	315
Data rate (kbps)	1 - 200		
Sensitivity (dBm)	< -70		
Modulation (chapter 2)	OOK	OOK	S-OOK
Power consumption (μW)	< 77	< 40	< 10
Power Source	Battery	Battery	Energy harvesting
Applications	Long-range WSNs: Field Area Network, Security, Home Automation	Short-range WSNs: BAN, In-Vehicle Network, Industrial Automation, Telemetry	

1.3 Thesis Organization

This chapter has provided the overview on the WSNs: applications of the WSNs and architecture of a single sensor node. The distribution of energy consumption of each component in a node was also presented. From that, the goal of this research

was introduced, which is to design and implement ultra-low power receivers with as minimum power consumption as possible and sensitivity better than -70 dBm.

Next chapter presents some considerations in architecture and circuit design for low power target, in which architecture is an important factor for reducing total power consumption. In addition, platform technology on which the receiver will be fabricated is also discussed.

Chapter 3 and chapter 4 present On-Off Keying (OOK) receivers operating at 920 MHz and 315 MHz respectively. New architectures are proposed, allowing to achieve low complexity, low power with high sensitivity. In those architectures, a clock is provided from outside to cut off RF circuits periodically during the active time.

Chapter 5 proposes the Synchronized On-Off Keying (S-OOK) modulation scheme and an S-OOK receiver at 315 MHz frequency. The receiver in this chapter has deeply duty-cycled RF front-end using a window generated by a digital circuit. Moreover, at the back-end, data and corresponding clock are produced without a clock and data recovery circuit.

Finally, the conclusion of the thesis is drawn in chapter 6, which presents performance comparison. The lifetime and the communication distance in free space are also estimated in this chapter.

1.4 Original Contribution

Several contributions on the architectures and modulation scheme for ultra-low power and high sensitivity receivers have been made in this work. Following are main contributions:

1. Intermittent RF front-end using switched bias has been proposed to overcome the trade-off between power consumption and sensitivity.

2. The study has developed a novel OOK receiver architecture operating at the low carrier frequency (315 MHz) for the short-range applications. In this architecture, no envelope detector or baseband amplifier is employed. Alternatively, a comparator and digital modulation is used for back-end of the receiver.

3. In this study, it is the first time the S-OOK modulation scheme for narrow band signal has been proposed. The S-OOK signal contains not only data but also clock information, leading to the data and corresponding clock are demodulated simultaneously. A separate clock and data recovery circuit is not required after back-end of the S-OOK receivers.

4. This work has also designed and verified an S-OOK receiver operating in 315 MHz frequency band with great power reduction in comparison to the conventional receivers.

Chapter 2

Considerations for Low Power Receiver Design

The well-known method to save energy in systematic level is duty-cycling to reduce the active time of a system. The system is turned on only in a necessary period [14, 15]. Otherwise, it is turned off. Duty-cycled operation of the system can be synchronous or asynchronous and executed by a control unit. In the case of synchronous duty-cycling, it is necessary to have a common clock source to make sure transmitters and receivers are turned on in the same time slot. However, in order to provide such common clock, it is not always simple, especially when number of sensor nodes is large, and they are deployed in a spreading area. Furthermore, the common clock needs to be buffered to distribute to many branches, which may consume considerable energy [16]. The more preferred method is the asynchronous operation, in which an ultra-low power wake-up receiver is attached in each node [17]. The wake-up receiver operates continuously to listen whenever wake-up signal is incoming, and then generates a signal to turn on the main transceiver. Even though this method allows to save much power, if the active power of receivers is large, the lifetime of the nodes is still limited. For example, assume that the ratio of active time to sleep time is 1/10, the receiver in [18]

can work only for 0.3 year with the coin battery CR2032. Therefore, it is necessary to find out solutions to reduce the active power of the receivers. In this section, we present considerations in architecture, circuit design and fabrication technology to reduce the active power of the receivers and then extend the lifetime of the sensor nodes.

2.1 Architecture Consideration

Choosing a suitable architecture for receiver design is an important step to achieve final targets. There are many types of receiver architectures frequently used in modern wireless systems. The simplest one is the RF detection receiver (Figure 2.1). It includes RF gain stages before an envelope detector and baseband amplifier. The disadvantage of this receiver is insensitivity with frequency and phase information; it demodulates data based on amplitude only. Therefore, the ability of interference suppression is not good. In order to reject out-of-band signal, it employs an RF filter after the output of the antenna. Also, the sensitivity of this receiver is heavily limited by the envelope detector. For achieving high sensitivity, high gain RF amplifiers before the envelope detector are needed with the cost of the increase in power consumption.

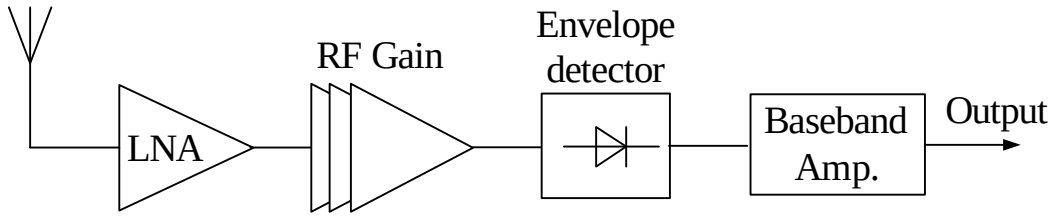

Figure 2.1: RF detection receiver with OOK modulation

For better sensitivity and interference immunity, the conversion receiver architecture is preferable (Figure 2.2). The signal at RF frequency is converted down to IF frequency by a mixer. Then baseband signal can be received using second mixer with condition $\omega_{LO2} = \omega_{IF} = \omega_{in} - \omega_{LO1}$. The number of downconversion stages can be

increased by adding more IF stages before the baseband downconversion. However, using this structure to receive asymmetric spectrum signals such as FSK, QPSK, GMSK and QAM, self-corruption will happen (Figure 2.3). To avoid that effect, the quadrature conversion architecture is proposed (Figure 2.4), generating two versions of baseband signal that together can reconstruct the original information [19].

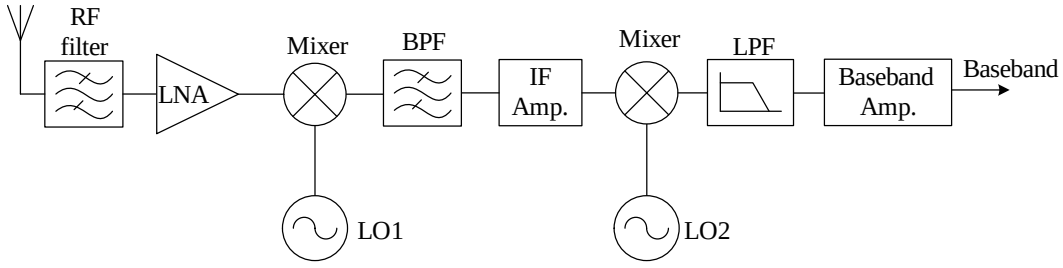

Figure 2.2: Frequency conversion receiver

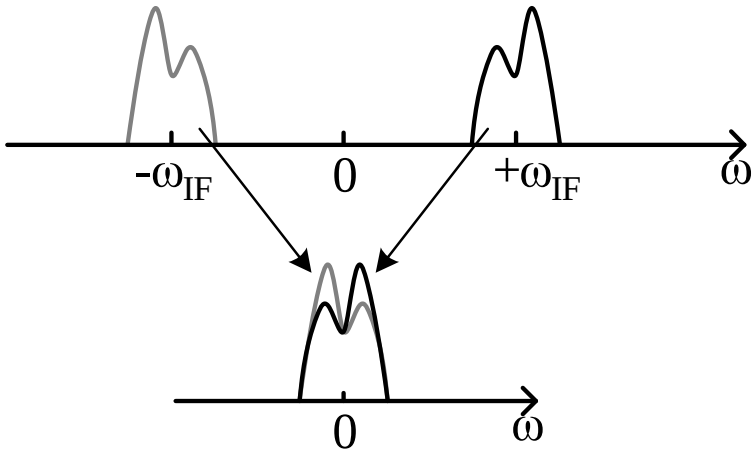

Figure 2.3: Self-corruption in conversion receiver

Another popular receiver architecture is zero-IF or low-IF receiver (Figure 2.5). Depending on relationship $\omega_{LO} = \omega_{in}$ or $\omega_{LO} = \omega_{in} \pm ChannelBandwidth$, the receiver is classified as zero-IF or low-IF receiver, respectively. In this case, channel selection is implemented by low-pass filters, which can be realized on-chip as active circuits with relatively sharp cut-off characteristics.

During designing a receiver, choosing which architecture depends on applications and requirements. The advantage of the frequency conversion receivers is that gain

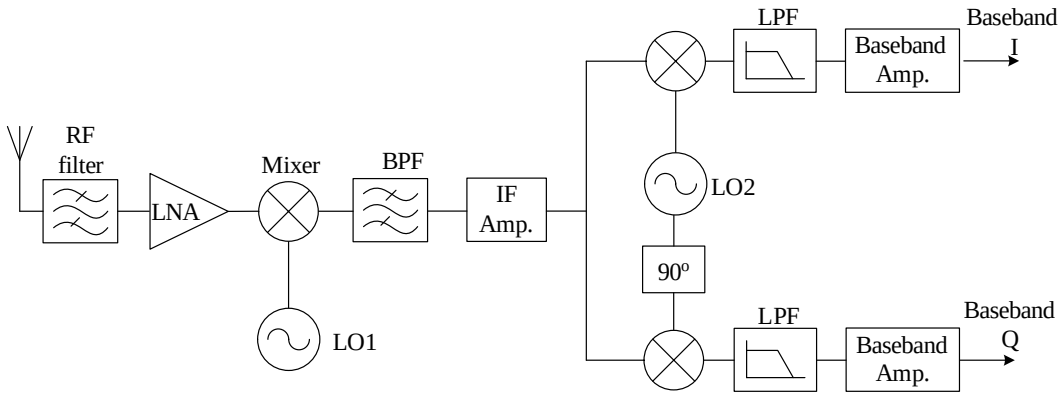

Figure 2.4: Quadrature conversion receiver

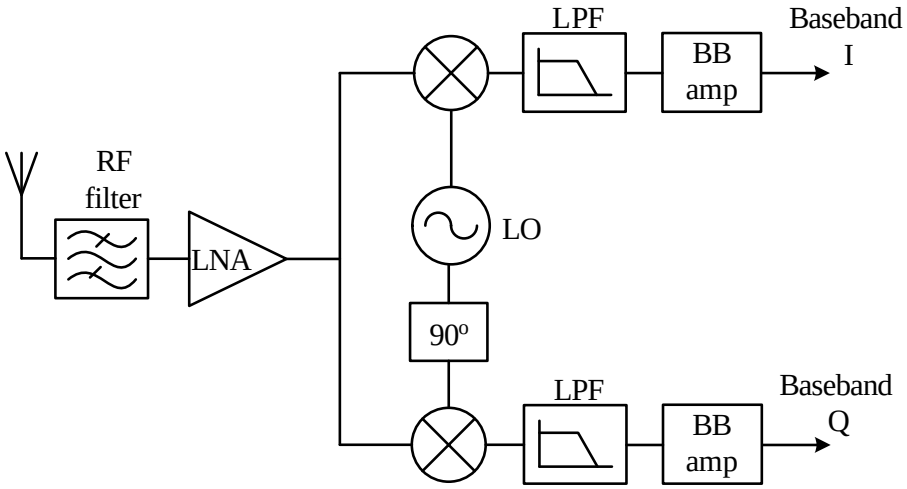

Figure 2.5: Zero-IF or Low-IF Receiver

and selectivity can be realized at lower frequencies, improving performance in terms of sensitivity, noise figure and interference rejection. However, power consumption is limited by the local oscillators. In addition, the strict requirements in frequency accuracy and phase noise usually require a power-hunger frequency synthesizer with an LC oscillator and a phase-locked loop. The RF detection receiver has some disadvantages as mentioned before, however, this type of receiver is simple in circuit design without local oscillators, mixers and IF amplifiers. Therefore, in low data rate applications with not so high sensitivity required, the RF detection receiver is suitable for low power target. In fact, the lowest power receivers published recently are RF detection receivers with OOK modulation scheme [20], [21]. In this study, the

new receiver architectures were proposed based on the RF detection receiver with the OOK modulation.

2.2 Circuit Level Considerations

2.2.1 Matching circuits

Matching impedance is an important issue; it is considered to transfer maximum power from a terminal to another. In a receiver, the low noise amplifier (LNA) is a component interfacing with the antenna. Its input needs to match to the antenna output for maximum gain and minimum noise. There are many techniques of input matching, however, depending on design targets, we have to consider to choose a suitable technique.

A) Shunt resistor:

The easiest way to match input with a resistive source impedance $Z_s = R_s$ is to shunt the input with a resistor R_{sh} equal to R_s as shown in Figure 2.6. This method provides broadband matching, simplicity, relative independence on power consumption. However, the resistor R_{sh} introduces thermal noise of its own at the input, leading to degrading noise performance. The noise factor of this amplifier is calculated [22]:

$$F = 2 + \frac{4\gamma}{g_m R_s}, \tag{2.1}$$

where g_m is the transconductance of M1, γ is the excess noise coefficient. The value of γ is 2/3 for long-channel transistors and can increase to 2 in short-channel devices. In this case, the noise figure is:

$$NF = 10\log(F) = 10\log(2 + \frac{4\gamma}{g_m R_s}) \tag{2.2}$$

It is clear that, the noise figure of this topology exceeds 3dB substantially.

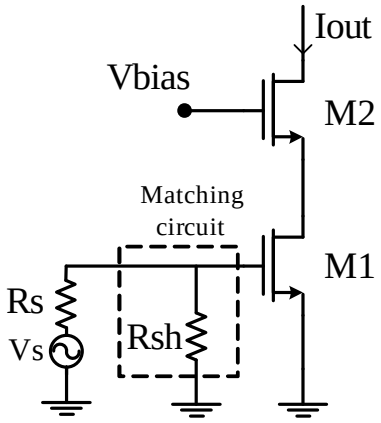

Figure 2.6: Matching by shunt resistor

B) Classic matching:

It is preferred that the input of LNA must be matched to the standard characteristic impedance of 50 Ω without adding the thermal noise of a 50 Ω resistor. It can be completed by using reactance devices (Figure 2.7). The matching circuit can be one of the topologies shown in Figure 2.8 [23]. By choosing a suitable circuit, matching conditions can be met. Although this method introduces mismatch between gain matching and noise matching [24], it is used in many designs because the gain matching can be attained regardless power consumption.

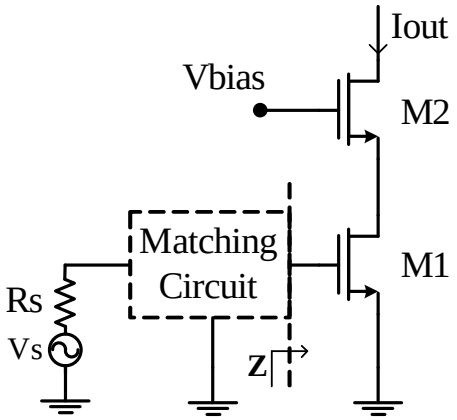

Figure 2.7: Classic matching

C) Simultaneous noise and gain matching

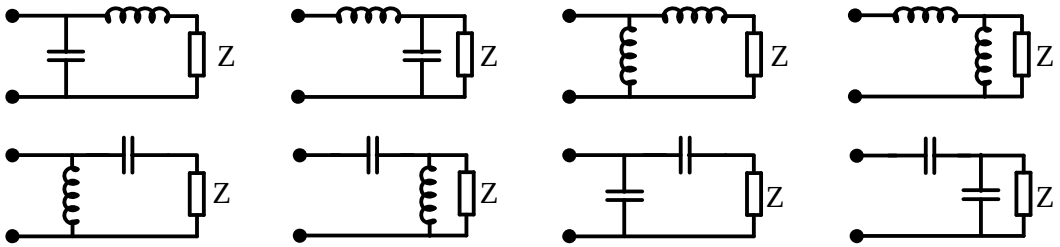

Figure 2.8: Possible matching topologies

This technique overcomes the disadvantage of the classic matching method. By using a source degeneration inductor (Figure 2.9), noise and gain matching conditions can be met simultaneously. In this case, transistor size and gate voltage of M1 must be chosen to meet the matching conditions. These choices, however, usually lead to excessive power dissipation [25], [24], not applicable for ultra-low power circuits.

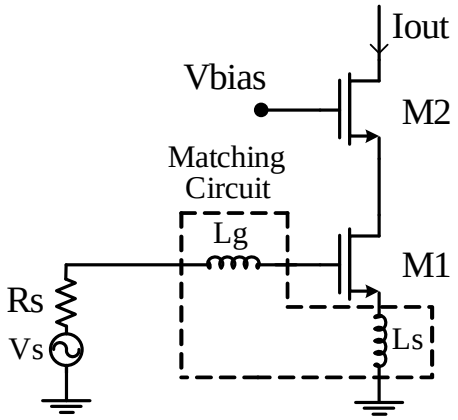

Figure 2.9: Simultaneously noise and gain matching

D) Power-constrained simultaneous noise and gain matching

Schematic of the technique that allows the amplifier meets both noise and gain matching conditions with low power constraint is shown in Figure 2.10. In this technique, the real part of input impedance can be adjusted by L_s. With a give L_s, the requirement of the imaginary part of the input impedance is satisfied by choosing a suitable C_{ex}.

Considering above techniques, the last one is the best choice to get optimum noise figure and match input impedance with source impedance, concurrently meets the

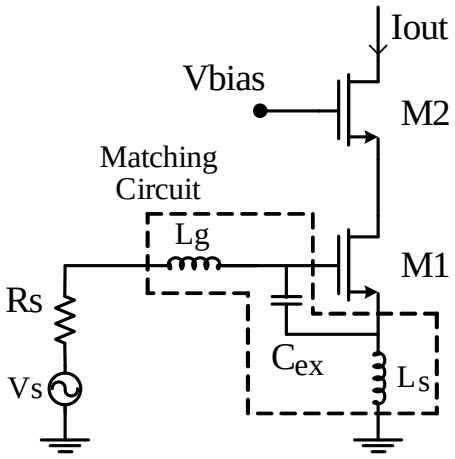

Figure 2.10: Power-constrained simultaneously noise and gain matching

constraint on power. However, the value of L_s is usually small, leading to the matching status to be very sensitive to parasitic inductance and capacitance. Therefore, this technique is not always easy to realize. Qualitatively, we can list up the characteristics of four matching methods in Table 2.1.

Table 2.1. Characteristics of the matching methods

Method	**Noise**	**Meet Low Power Constraint**	**Parasitic Sensitivity**
Shunt Resistor	High	Yes	Low
Classic Matching	Medium	Yes	Low
Simultaneous Noise & Gain Matching	Low	No	High
Power-Constrained Simultaneous Noise & Gain Matching	Low	Yes	High

With applications that prioritize low power consumption, the classic matching technique could be a good choice although it does not provide the optimum noise figure. In addition, the matching circuit in this technique provides a passive gain, increasing total gain of the amplifier. Also for low power target, the shunt resister

technique can be used because it meets matching conditions in broadband and simple to realize regardless power requirement. These matching techniques will be used in the proposed receivers.

2.2.2 Multi-supply voltage

Within many techniques known in the literature to reduce the power consumption of circuits, supply voltage reduction is an effective method. However, that method may cost severely in terms of speed or noise performance. To overcome those issues, multi-supply voltage design is an alternative. A design is partitioned into separate voltage domains; each operates at its own proper supply voltage depending on its requirements [26]. Critical domains are provided higher voltages to maximize performance. Meanwhile, non-critical domains operate at lower voltages for reduction of power consumption.

In RF receivers, RF front-ends play important roles. They decide gain and noise performance and hence the sensitivity of the receivers. Therefore, the RF front-ends may need to operate at high voltages. For low data rate applications, analog baseband and digital processing circuits work at low speeds, timing requirements are non-critical. Those circuits can be supplied lower voltages to optimize power consumption.

2.2.3 Gain and power consumption trade-off

Considering a simple common source amplifier as shown in Figure 2.11. M1 is biased to operate in the saturation mode. The voltage gain of the circuit is calculated [27]:

$$A_v = -g_m R_{Load}, \tag{2.3}$$

where g_m is the transconductance of M1. It is calculated [27]:

$$g_m = \sqrt{2KI_D}, \tag{2.4}$$

in which, K is a coefficient, related to technology and sizes of M1. Substituting (2.4) into (2.3), we have:

$$A_v = -R_{Load}\sqrt{2KI_D} \tag{2.5}$$

From Equation (2.5), there are two solutions to increase voltage gain of the circuit. 1) Increasing I_D. This way directly increases the power consumption of the circuit. 2) Increasing R_{Load}. Since $V_{out} = V_{DD} - I_D R_{Load}$, if R_{Load} increases to a large value, output voltage swing will be limited. This issue can be solved by replacing the resistive load by an LC tank. However, on-chip inductor usually consumes large area and low Q-factor. If integration is not a critical issue, a high Q-factor off-chip inductor can be used for high gain, low power consumption. In the case that voltage swing is not important, the high gain can be achieved with low power consumption by using high resistive loads. In this case, however, the bandwidth of the circuit will be heavily degraded when taking into account capacitance at the output node (Figure 2.12). C_{out} is composed of parasitic capacitance of the circuit at that node and input capacitance of the next stage. Nonetheless, this issue can be circumvented by using low carrier frequency.

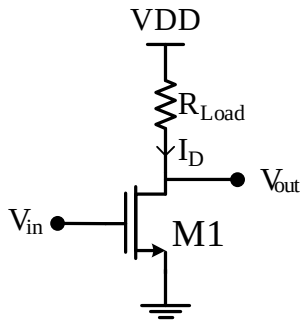

Figure 2.11: Simple common source amplifier

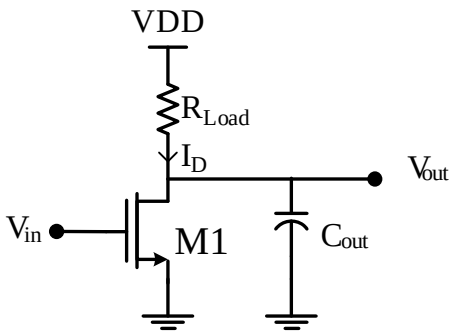

Figure 2.12: Simple common source amplifier with output capacitor

2.3 SOTB CMOS Technology for Low Power

The Silicon-on-Insulator (SOI) CMOSFET has been developed over 30 years [28, 29]. Figure 2.13 shows cross-section of a bulk CMOS transistor and a conventional SOI CMOS transistor. Owing to the insulator layer between source/drain and substrate, circuits on the SOI CMOS technology avoid the latch-up phenomenon. The leakage current and junction capacitance are reduced considerably [30], leading to higher density, lower power consumption, higher speed and no body effect. However, the body of an SOI device is floating; therefore threshold voltage V_{th} is changed in switching state, changing the delay of the circuits and difficult to match transistors for analog designs. The thick buried-oxide (BOX) also insulates thermal. Hence, heat accumulates in transistors rather than spreading through the substrate. In order to overcome disadvantages of the conventional SOI CMOS devices, the Silicon-On-Thin-BOX (SOTB) CMOS technology has been proposed with many advantages over the conventional bulk CMOS [31, 32]. It has been proved that the SOTB CMOS is one of the best candidates for ultra-low voltage, low-power applications [33, 34, 35].

2.3.1 SOTB CMOSFET Structure

Naturally, SOTB CMOS is an Fully-Depleted-SOI (FD-SOI) CMOS technology with very thin BOX and triple well structure [36, 37]. Figure 2.14 shows structure of

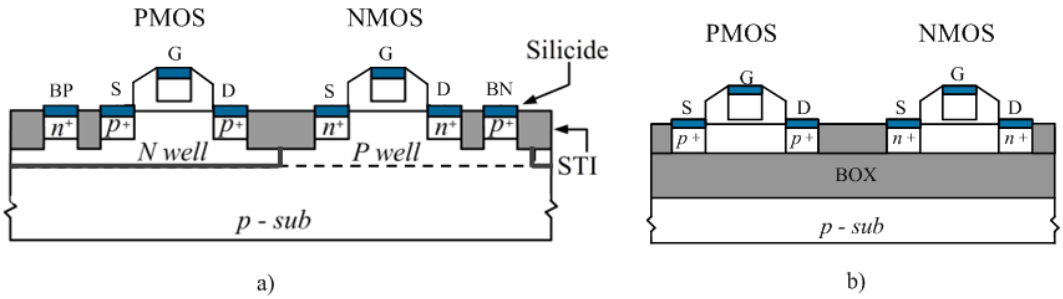

Figure 2.13: a) Bulk CMOS and b) Conventional SOI CMOS

SOTB CMOS transistors. The thickness of the BOX is reduced to about 10 nm, together with Deep Nwell layer, the body voltages of PMOS and NMOS can be applied separately.

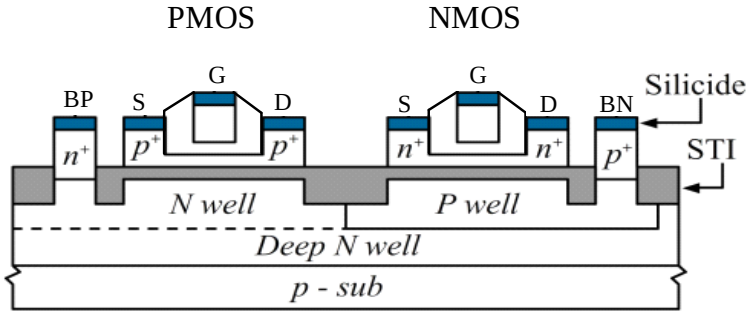

Figure 2.14: Structure of SOTB CMOS

2.3.2 Low operation voltage

The supply voltage should decrease proportionally to the miniaturization of transistors. However, in sub-100-nm technologies, further reduction of the supply voltage is difficult because of increase in the variation of V_{th}. In SOTB CMOSFETs, variation of V_{th} is suppressed considerably [38, 39]. As a result, circuits on SOTB CMOS devices can operate at low voltage down to 0.22 V [34].

2.3.3 Ultralow leakage current

Leakage current I_{off} in CMOSFETs includes the subthreshold leakage current, gate-induced drain leakage (GIDL) current and junction leakage current [40]. In Bulk CMOS, the GIDL current is the major element of the I_{off}, which flows to substrate. Because of the BOX layer, the GIDL current of an SOI transistor is suppressed, the I_{off} is dominated by the subthreshold leakage current. In SOTB devices, the GIDL current is also suppressed. The subthreshold leakage current can be reduced drastically [33, 35] by applying suitable back-gate bias voltage. In addition, the leakage is reduced easily by decreasing overlap length L_{ov} between gate and source/drain extensions.

Besides, the SOTB CMOS device also provides a larger tranconductance than the bulk CMOS device, providing a higher gain at the same current consumption. Appendix A shows more information on characteristics of the SOTB CMOS devices. Table 2.2 summarizes some key specifications of the SOTB CMOS in comparison with Bulk CMOS and SOI CMOS.

Table 2.2. Key specifications of the SOTB CMOS in comparison with Bulk CMOS and SOI CMOS.

Technology	Gm	Leakage	Drain Conductance	Vth
Bulk CMOS	Low	GIDL dominant	High	High (~0.4V)
SOI CMOS	High	Subthreshold leakage dominant	Low	Low (~0.2V)
SOTB CMOS	High	Subthreshold leakage is controlled by back bias	Low	Low (~0.2V)

2.4 Conclusion

This chapter presents some aspects in system architecture, circuit design and choice of technology for the low power consumption. To achieve required targets, the first thing should be considered is the system architecture. There are many receiver architectures used in modern communications such as RF detection, frequency conversion receiver, low-IF receiver. Although the RF detection receiver is limited in sensitivity and interference rejection, it is the best choice for ultra-low power applications. In this study, the new receiver architectures are proposed based on the RF detection receiver with the OOK modulation scheme. In circuit level, the low power techniques were discussed, in which topologies of matching circuits and gain stages are very important and need to be considered carefully. Finally, the structure and characteristics of CMOS technologies were presented briefly. It has been proved that the SOTB CMOS is a suitable process for ultra-low voltage, low power applications.

Chapter 3

920MHz OOK Receiver with Switched Bias for Long-Range Applications

In RF receivers, usually RF front-ends and local oscillators consume most of power [18], [41], [42]. Therefore, many solutions were proposed to reduce the power consumption of the RF front-ends and the local oscillators. With the RF detection receivers, local oscillators, mixers, and IF bandpass filters are eliminated, simplifying structure and reducing power consumption significantly. However, the RF amplifiers still dissipate dominant power in those receivers such as in [18], [43] with more than 70 % of their power dissipated by the RF amplifiers.

The work in [20] demonstrated a receiver structure in which the RF amplifier is not employed. Alternatively, RF signal is sampled directly from the output of the antenna by intermittent samplers so that the power consumption of the receiver is reduced drastically. However, sensitivity of that receiver is limited, only -55 dBm because there is no RF amplifier before RF envelope detection.

In this chapter, we present a receiver design, in which a solution is proposed to overcome the trade-off between power consumption and sensitivity. In the receiver, high gain RF amplifiers are employed to achieve high sensitivity. However, the power consumption of the RF amplifiers does not increase significantly because of their intermittent operation. The proposed receiver operates at 920 MHz, dedicated for the long-range WSN applications.

3.1 Architecture

This receiver was presented in [44], its architecture is shown in Figure 3.1. In order to achieve low power target, the RF detection architecture is employed with OOK modulation. However, different from the conventional RF detection receiver as shown in Figure 2.1, the RF amplifiers do not operate continuously, but intermittently. After the envelope detector, the signal has intermediate frequency and then demodulated by a sample & hold circuit.

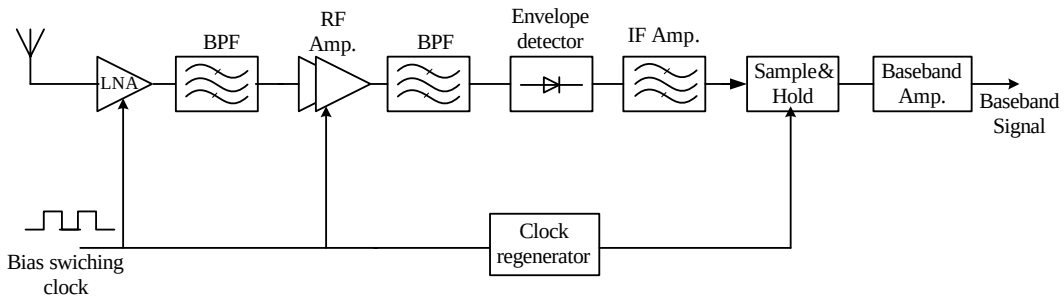

Figure 3.1: Detection Receiver with Switched Bias.

The RF stages are common source cascaded amplifiers. A clock signal is applied to the bias terminal of the cascaded transistor (Figure 3.2a) instead of a constant voltage (Figure 3.2b). The cascaded transistor M2 in Figure 3.2a plays the role of a lock. It opens only when the clock is high. Assume that a 50 % duty-cycle clock is used for biasing, the power consumption of the circuit in Figure 3.2a is

reduced by approximately 50 % in comparison with the constant bias topology in Figure 3.2b. Figure 3.3 shows the operation of the receiver with the bias switch technique. After the RF amplifiers, the signal is an RF pulse chain at the duration of high bits (Figure 3.3c). At the output of the envelope detector, the signal has the same frequency as the bias clock (Figure 3.3d). In this design, we used a 2.5 MHz clock for switching bias of the cascaded transistors. The final bit sequence is recovered using a sample&hold circuit followed by baseband blocks (Figure 3.3e, f), similar to the double sampling method presented in [45].

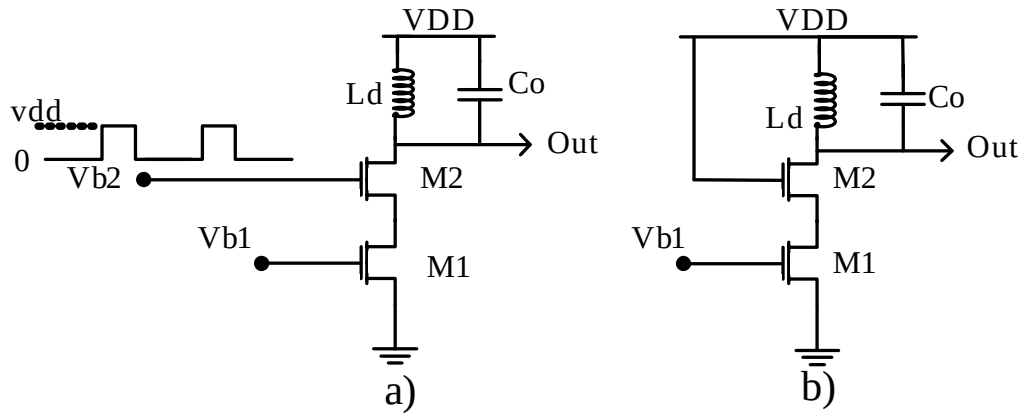

Figure 3.2: Switched Bias Cascaded Common Source Stage.

3.2 Circuit Implementation and Simulation Results

The receiver is designed and simulated on the 65 nm SOTB CMOS process. Schematic of the RF front-end is shown in Figure 3.4. In the first stage, the classic input matching method is adopted to optimize for gain instead of noise figure. The matching circuit includes C1, C3, L1. Loads of the RF amplifiers are LC tanks with the high-Q off-chip inductor L2, L3. C5, C7 are total capacitances at the output nodes. L2, L3 are chosen to resonate with C5, C7, respectively. L2, C5 and L3, C7 form the

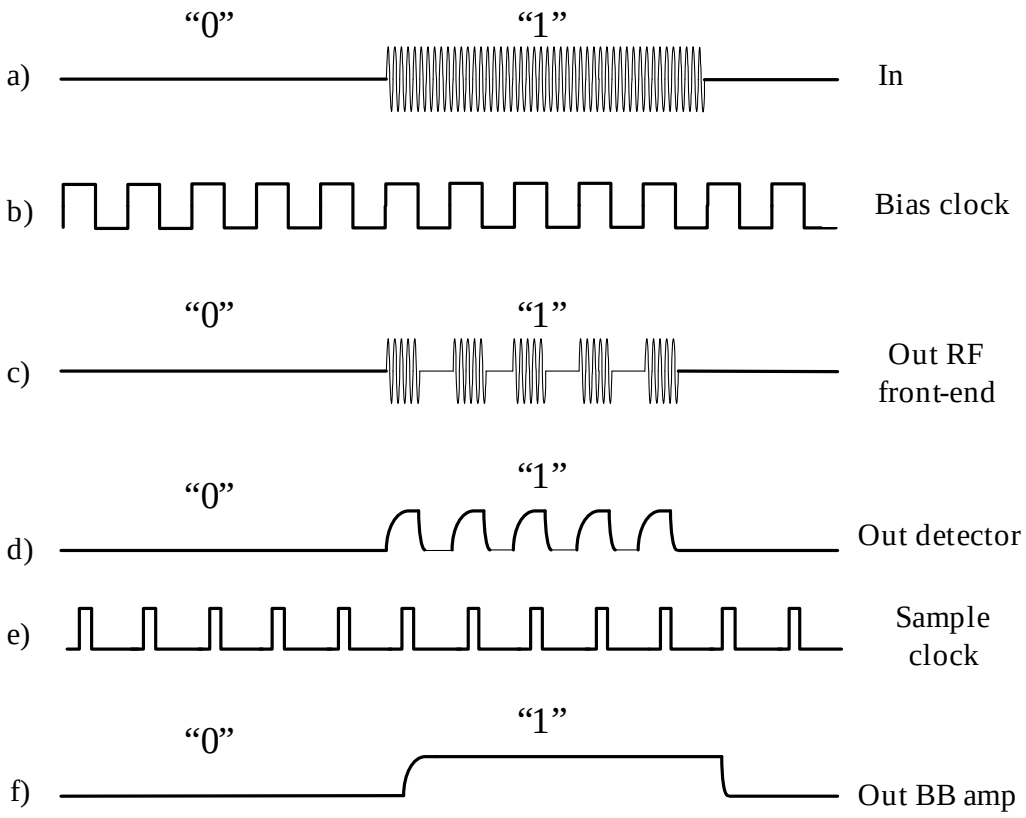

Figure 3.3: Timing chart.

output loads of each state at the interest frequency and concurrently play the role of filters to attenuate low-frequency signal caused by the bias clock. C2, C4 and C6 are AC coupled capacitors. Figure 3.5 shows the simulated AC characteristics of the RF front-end. It achieves a total gain of 47 dB, a noise figure of 4.65 dB at 920 MHz with power consumption of 45.6 μW.

The envelope detector is shown in Figure 3.6. M and M' are biased to operate in the weak inversion regime ($V_{GS} \approx V_{th}$) [46]. Two identical branches are employed to create the differential output. The capacitor C_{det} forms a pole at the frequency [16]:

$$f_{pole} = \frac{g_m}{2\pi C_{det}} \tag{3.1}$$

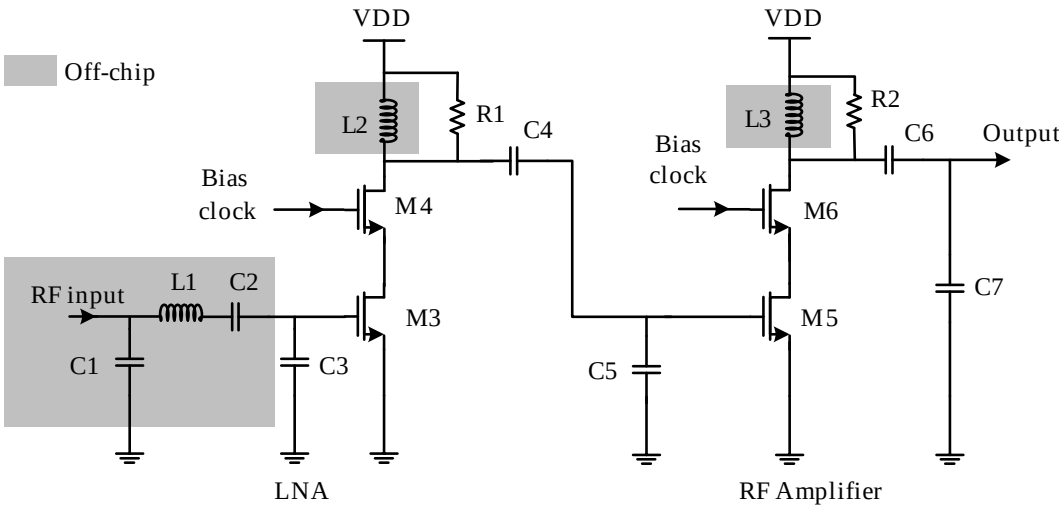

Figure 3.4: RF front-end.

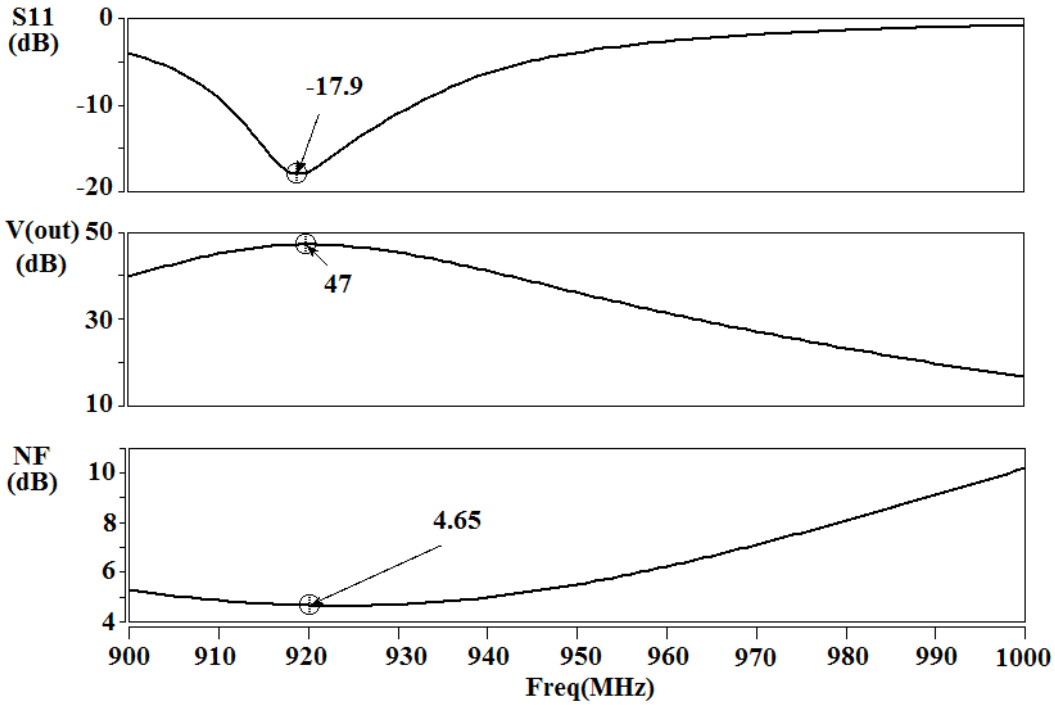

Figure 3.5: Simulated AC characteristic of the RF amplifier

Where g_m is tranconductance of M. This pole defines the bandwidth of the envelope detector, and is designed to filter out the carrier frequency and the high-order

harmonics. The bandwidth is also set high enough so that the IF signal with the frequency of the bias clock can pass without attenuation.

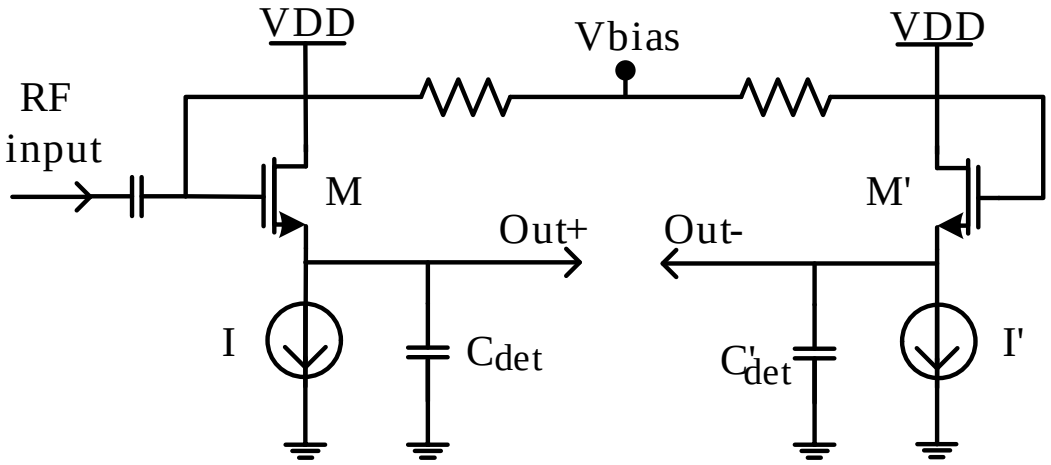

Figure 3.6: Envelope detector

The IF amplifier is a fully-differential operational amplifier (Figure 3.7), including two stages. The tail current source of the first stage is split into two halves connected by a capacitor. The transfer function of this amplifier has a zero at DC [47], suppressing DC offset caused by asymmetrical factors at the inputs. The gain of the IF amplifier can be set from 20 dB to greater than 40 dB. Figure 3.8 shows AC characteristic of the IF amplifier with a zero at DC. Following the IF amplifier is simple sample&hold circuit including CMOS switches and small capacitors.

The baseband amplifier is also a two-stage operational amplifier with differential inputs, single-end output. In the first stage, loads are diode-connected transistors. With this kind of load, a common mode feedback circuit is not necessary. Figure 3.9 and Figure 3.10 are schematic and AC characteristic respectively of the baseband amplifier.

Figure 3.11 and Figure 3.12 show the layout pattern and microphotograph of the receiver respectively. The active core occupies an area of 985 x 600 μm^2.

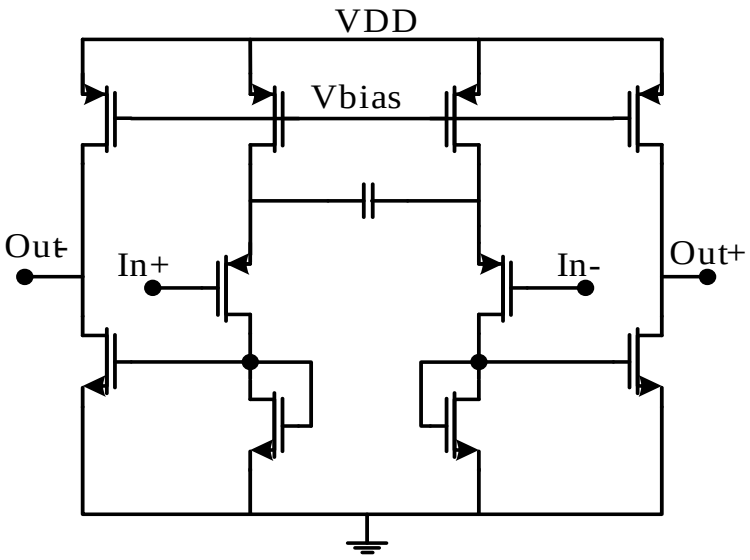

Figure 3.7: IF amplifier

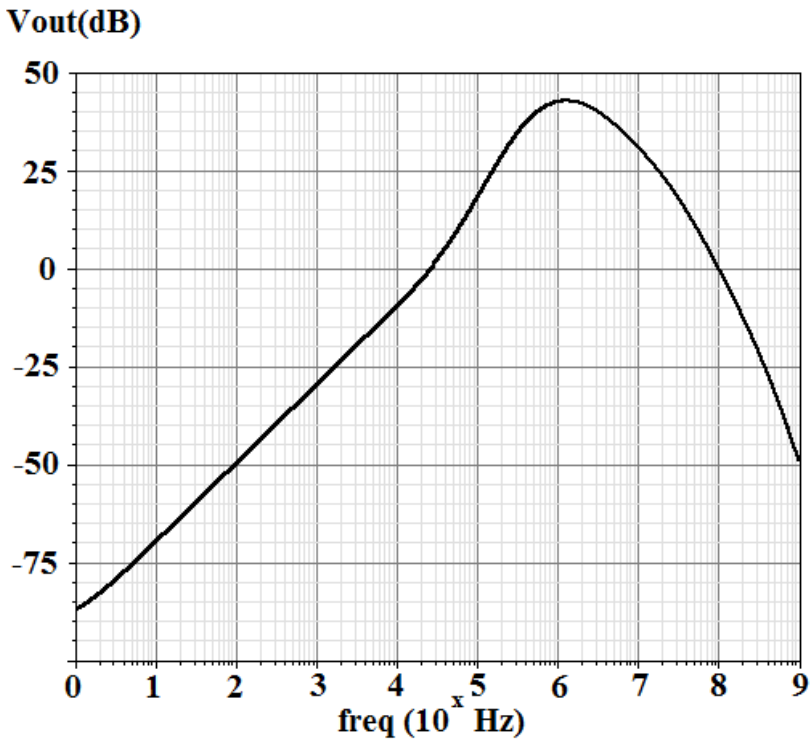

Figure 3.8: Simulated AC characteristic of the IF amplifier

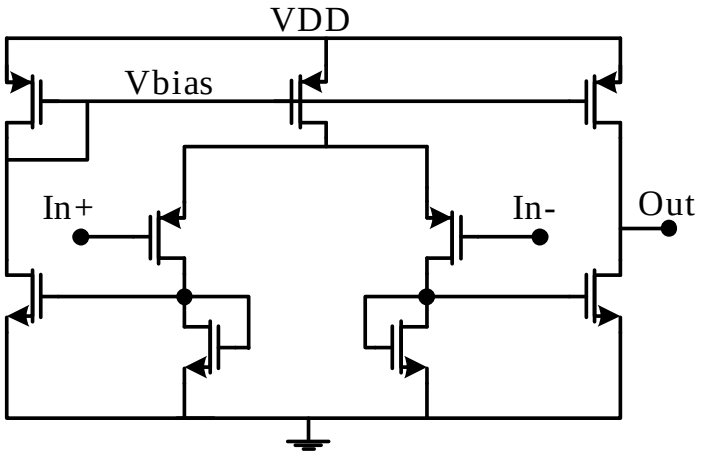

Figure 3.9: Baseband amplifier

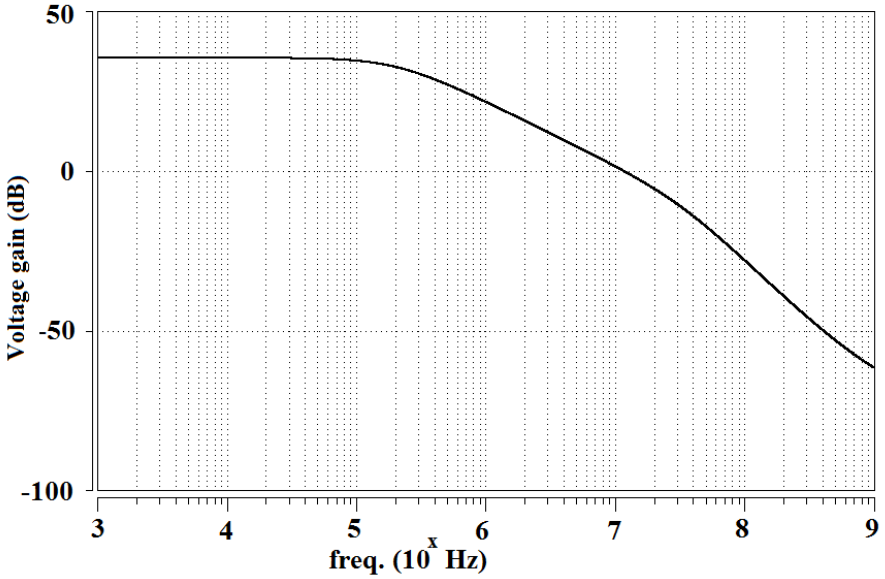

Figure 3.10: Simulated AC characteristic of the baseband amplifier

3.3 Performance and Comparison

Figure 3.13 and Table 3.1 depict sensitivity at different data rates and current consumption of the receiver. At 10 kbps, the proposed receiver can achieve -82 dBm sensitivity. It should be noticed that without the switched bias and the sample & hold circuit is shorted, the receiver becomes a conventional RF detection receiver.

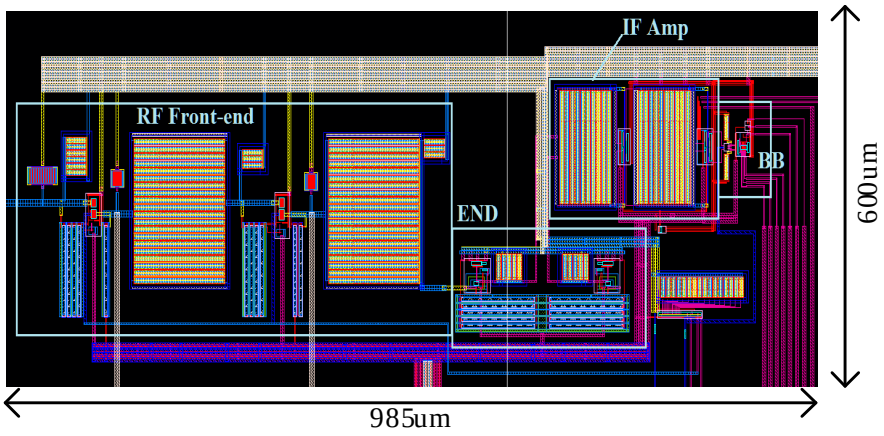

Figure 3.11: Layout pattern of the receiver

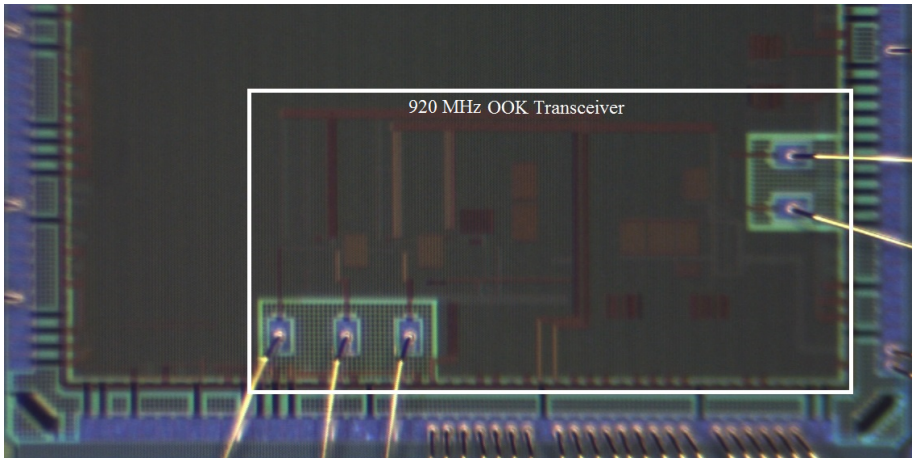

Figure 3.12: Microphotograph of the receiver

When operating as conventional one, the receiver consumes 162.8 μA from 0.6 V supply. Whereas, with 50 % duty-cycle clock for switching bias, the current consumption decreases to 88.5 μA, equivalent to 53 μW.

The Table 3.2 shows the performance summary of the proposed receiver. Main specifications of some state-of-art receivers operating at the same frequency band are also shown for comparison. We can see the outstanding performance of the proposed receiver in power consumption. When operating as a conventional RF detection receiver, the power consumption approximates 98 μW. With switched bias, the power

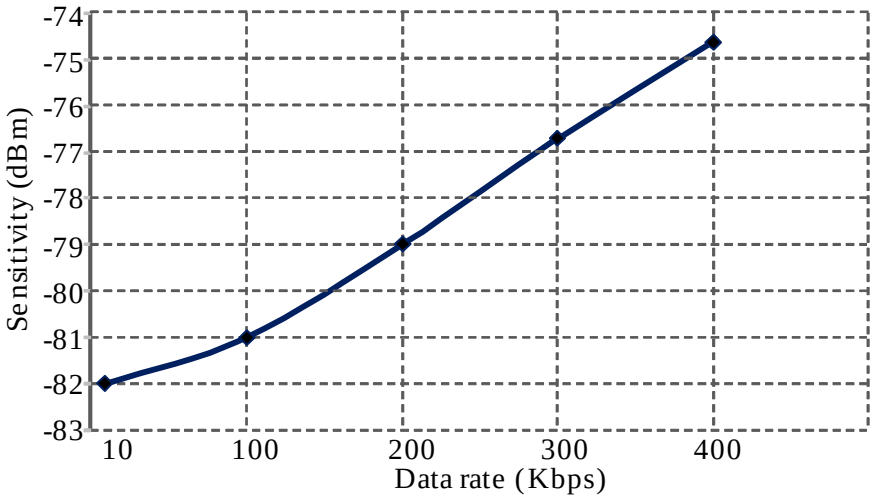

Figure 3.13: Sensitivity vs. Data Rate

Table 3.1: Current consumption of the receiver from 0.6 V supply

Circuit	Current(μA)	Circuit	Current(μA)
LNA	35/69*	IF amp.	7.4
RF amp.	41/81.3*	BB amp.	3.3
Env. det.	0.6	Others	1.2
Total current	88.5/162.8*		

* Conventional operation

consumption is reduced to 53 μW (46 % power reduction), smaller than half of power of other receivers. In terms of energy efficiency, the receiver in reference [42] is better, however, its sensitivity is much worse than this work (-50 dBm vs. -82 dBm).

3.4 Conclusion

In this chapter, the ultra-low power receiver operating at 920 MHz frequency for the long-range WSNs was presented, in which the switched bias is applied for intermittent operation of the RF front-end. In this receiver, the RF amplifiers are single-ended cascade common source amplifiers, the bias of the cascade transistors is switched by a clock to duty-cycle the RF amplifiers. The LNA is matched with input source

Table 3.2: Performance comparison

Parameter	Ref[48]	Ref[41]	Ref[49]	Ref[42]	**This work**
Technology	0.13 µm	40 nm	90 nm	90 nm	65 nm SOTB
Frequency (MHz)	868/915	782-932	915	868/915	920
Modulation	FSK	FSK	OOK	BPSK	OOK
Data rate (kbps)	45	12.5-625	10-100	2000	10-200
Sensitivity (dBm)	-89	-81	-56 -83	-50	**-82**
Power (µW)	1920	382.5	121	216	**53/98****
Energy/bit (nJ/bit)	42.66	0.612	1.2	0.108	**0.265/0.49****

(**) Power consumption and energy efficiency when operating as convention, without bias switching and the sample & hold circuit is shorted

impedance by the classical method to provide a passive gain and also overcome the low-power constraint of the receiver. It consumes 53 µW from 0.6 V supply with the best sensitivity of -82 dBm at 10 kbps.

Chapter 4

315MHz OOK Receiver Using Comparator and Digital Demodulation for Short-Range Applications

Following the regulation of the ARIB (Japanese association of radio industries and businesses), the 315 MHz band is defined as above 312 MHz to below 315.25 MHz. This low-frequency band is a suitable choice for ultra-low power applications. Radio waves of this frequency band can propagate through a longer distance than that of higher frequency band with the same transmission power because of the small loss in free space. The equivalent isotropically radiated power (EIRP) imposed by ARIB STD-T93 is shown in Figure 4.1. From 312 MHz to 315.05 MHz, EIRP has to be equal or less than 250 μW (-6 dBm); from 315.05 MHz to 315.25 MHz, EIRP is 25 μW (-16 dBm) or less; out-of-band emission intensity is 250 nW (-36 dBm) or less. Since the maximum transmitted power is limited to -6 dBm, this frequency band is dedicated to the short-range applications.

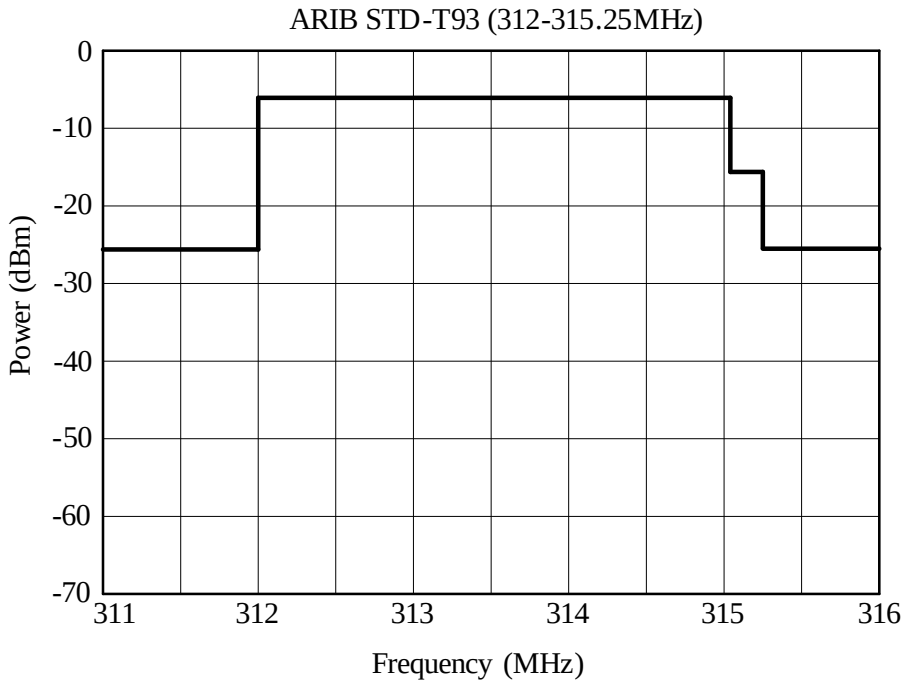

Figure 4.1: Power mask of 315 MHz band

In this section, a receiver design using OOK modulation at 315 MHz frequency band is proposed with low complexity and low power for the short-range WSN applications such as Body Area Networks (BAN), Indoor Monitoring, In-Vehicle Network. In this receiver, the RF amplifier operates intermittently for power reduction, similar to the receiver in Chapter 3. Furthermore, taking advantage of the low carrier frequency, the RF signal after the RF amplifier is directly converted to the digital signal. Thus, subsequent processing can be implemented in digital manner. The proposed architecture is verified by using discrete RF modules and FPGAs; then VLSI design is carried out.

4.1 System Architecture

In the conventional OOK receiver (Figure 2.1), RF signal after RF gain stages is converted to baseband by using an envelope detector. The baseband signal after the

envelope detector is usually small. Therefore, a variable-gain amplifier is used before digital processing. The receiver presented in this section has structure illustrated in Figure 4.2. It removes the analog baseband amplifier. Alternatively, the RF signal is amplified by high-gain RF amplifiers and then clipped by a threshold circuit (comparator) to have rail-to-rail level. After the threshold circuit, the signal is considered as a digital stream. A clock is applied to the RF front-end to turn it on and off periodically. Hence power consumption of the RF front-end and consequently total power consumption of the receiver is reduced considerably.

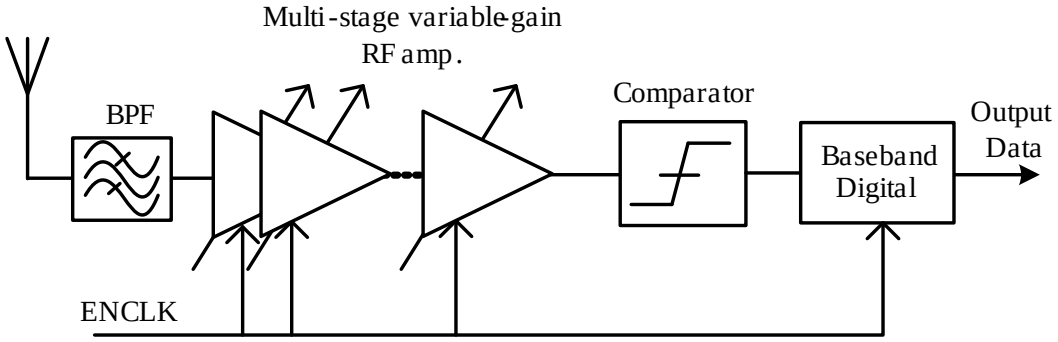

Figure 4.2: Architecture of the proposed receiver.

The timing chart in Figure 4.3 explains the operational principle of the receiver. "In" is RF input signal. $ENCLK$ with the frequency much higher than data rate is used to enable or disable the RF front-end. After the RF front-end, the signal for bit "1" is an RF pulse chain with pulse period equal to ENCLK period and the signal according to bit "0" remains unchanged, similar to the receiver in the previous section. At the comparator output, we obtain a 315 MHz rail-to-rail pulse stream. Finally, the output data is recovered by the digital baseband block. Schematic and operation of the digital circuit will be described in following section.

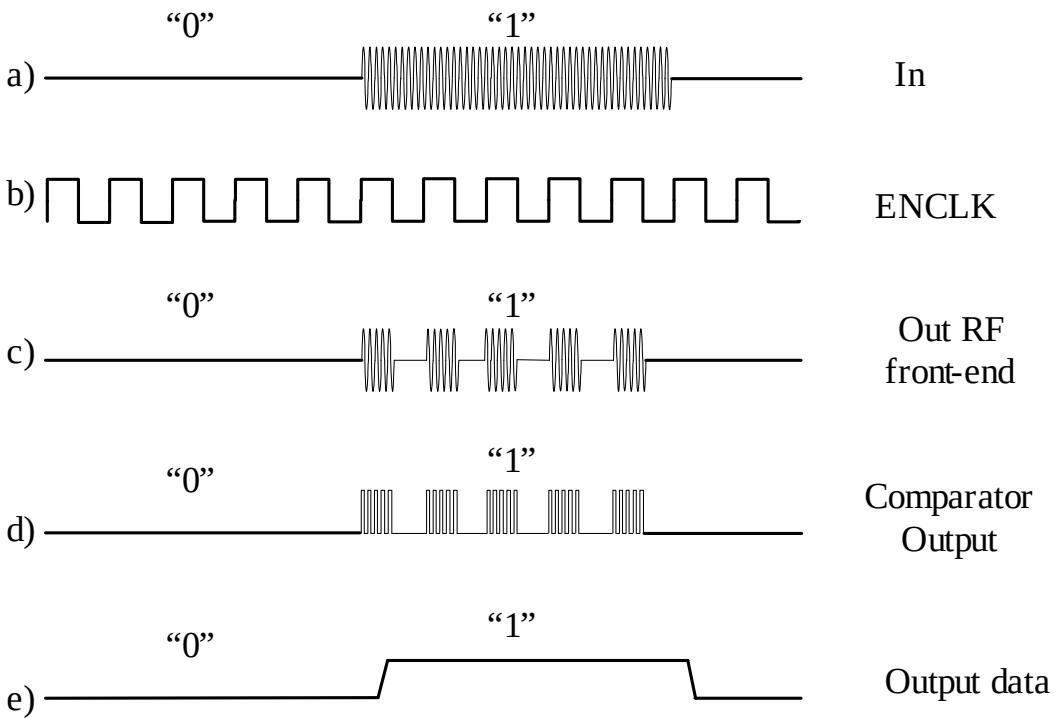

Figure 4.3: Timing chart of the proposed receiver.

4.2 Digital Baseband Processing

In the previous section, we knew that the 315 MHz RF signal is converted to a digital stream as described in Figure 4.3. In this case, the bit ”1” is according to groups of digital pulses. The digital circuit recovers data from these pulse groups. Figure 4.4 is schematic of the digital circuit and its operation is shown in Figure 4.5.

At first, there is no pulse at the input IN (comparator output), the node $X1$ is low so that the logic gate $I1$ is transparent with IN. $Q0$ is low hence the N-bit counter and flip-flop $FF1$ are cleared. When the first pulse in a pulse group from the comparator comes to the input, a transition from high to low appears at $X0$, leading $Q0$ from low to high and $X1$ becomes high. When $X1$ is high, the logic gate $I1$ closes and becomes ineffective with next pulses in the group. The counter starts to count with the clock $ICLK$, which has the frequency higher than that of the on-off RF front-end clock $ENCLK$ but much lower than 315 MHz. When the

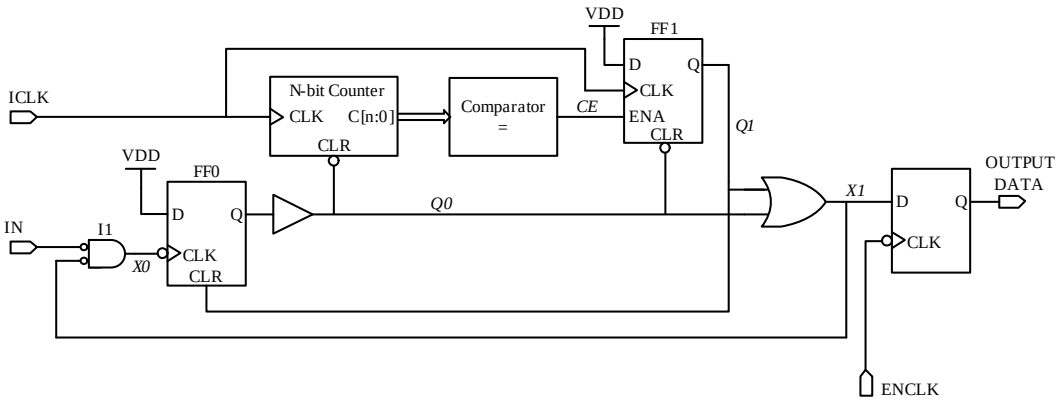

Figure 4.4: Schematic of digital circuit.

output of the counter is equal to a constant, the output of the comparator CE will be high, resulting in $Q1$ high at next the positive edge of $ICLK$. $Q1$ will clear $FF0$ and pull $Q0$ down, and then the counter and $FF1$ will be cleared. Consequently, $X1$ will go down. Frequency of ICLK and the comparison constant are chosen so that negative edge of $X1$ appears after the last pulse of a group and before the first pulse of the next group. Finally, the output data is recovered by latching $X1$ using the negative edge of $ENCLK$ (Figure 4.5). It can be seen that since the output of the comparator can be observed as a digital stream, a variable-gain baseband amplifier can be deleted. Alternatively, a very simple digital circuit is used to recover data as shown in Figure 4.4.

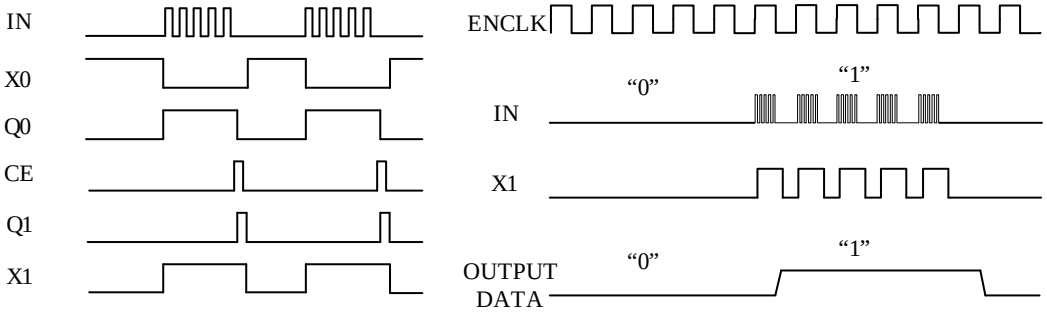

Figure 4.5: Operation of the digital circuit.

4.3 Architecture Verification

In order to verify the operation of the proposed architecture, we implement a prototype using a variable gain amplifier, a comparator for the RF front-end and an FPGA for implementation of the digital part. Here the Analog Device amplifier AD8369 with a maximum gain of 34 dB, the Texas Instruments comparator LMH7220 and the Altera Stratix IV FPGA are used for the experiment. The FPGA also generates the $ENCLK$ signal to turn the RF amplifier on/off. We choose frequency 1.5 MHz for $ENCLK$ and 25 MHz for $ICLK$. Therefore, the comparison constant in the digital circuit is 9 to make sure that $X1$ goes down later than the last pulse of a group and earlier than the first pulse of next group as discussed in the previous section.

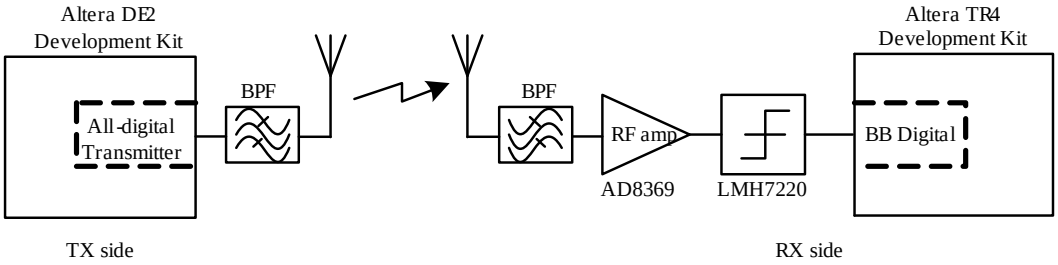

Figure 4.6: System prototype.

Figure 4.6 is block diagram of the system prototype with specific components.

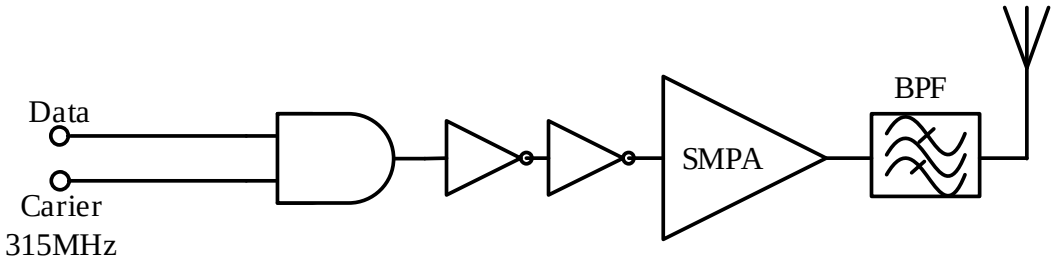

Figure 4.7: 315MHZ Fully-digital transmitter.

To verify the architecture in systematic level, a 315 MHz OOK fully-digital transmitter is designed as shown in Figure 4.7. It is similar to the transmitter presented

in [20], except power amplifier. The power amplifier in [20] is a class-F one while a switching-mode power amplifier (SMPA) is employed in this work [50, 51]. Thus, the transmitter can be implemented entirely on the FPGA. Figure 4.8 shows setting picture for experiment. Figure 4.9 is output spectrum with 100 kbps data rate of the transmitter. Output power at the center frequency is about -10.5 dBm and power level is -25 dB lower than the peak at the frequency offset of 500 kHz from the center, within the regulation of Japan.

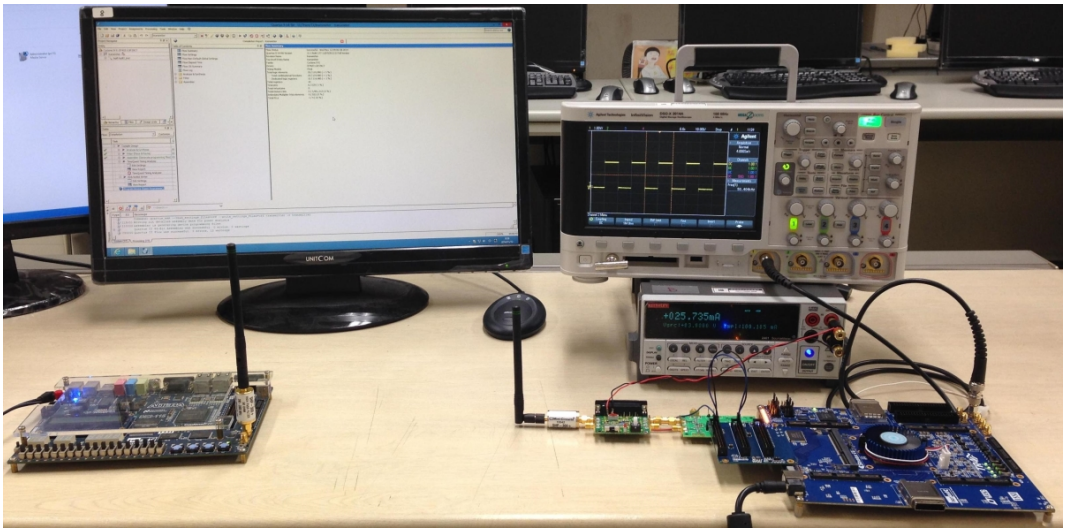

Figure 4.8: Experiment setup.

With the prototype system, the receiver and transmitter communicate successfully at a distance of 1 meter. Figure 4.10 shows waveforms of the $ENCLK$ and the output of the comparator corresponding to bit "1" coming to the receiver. When $ENCLK$ is off, there is no signal, and when $ENCLK$ is high, the signal includes pulse groups. Figure 4.3 is the waveform according to the case when a bit sequence "101010" is received at 100 kbps data rate.

At maximum gain setting, the prototype receiver achieves sensitivity better than -45 dBm (bit-error-rate (BER) $<$ 1E-3). Figure 4.12 shows measured BER performance of the receiver according to data rates 100 kbps and 200 kbps. It indicates

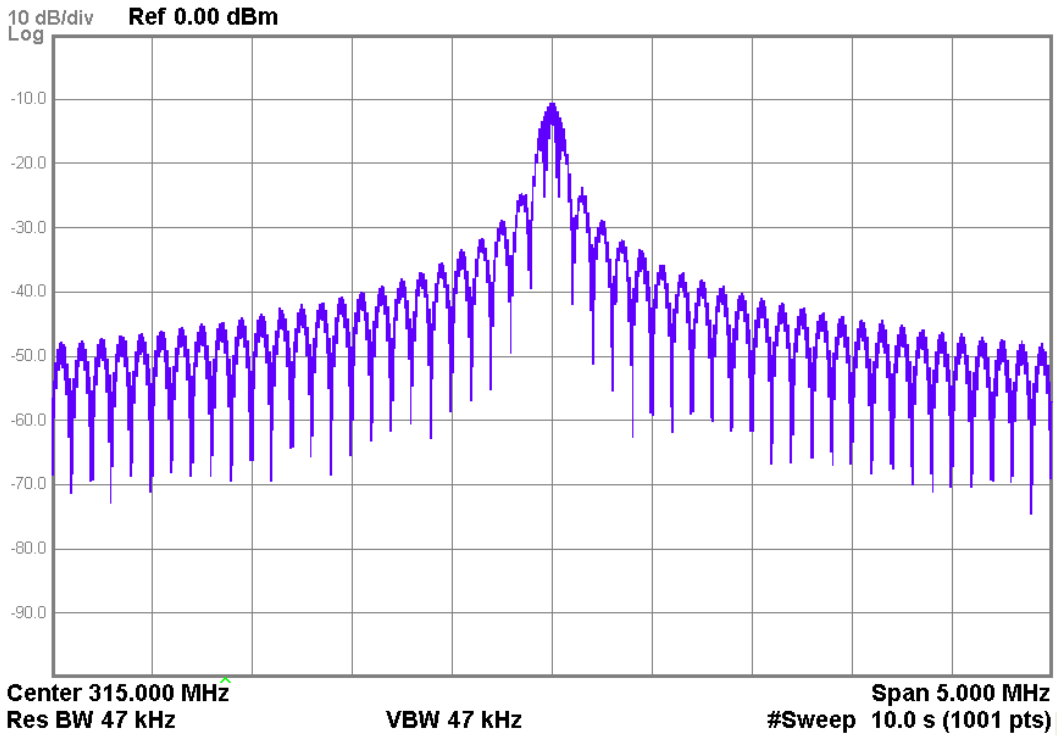

Figure 4.9: Output spectrum of the transmitter.

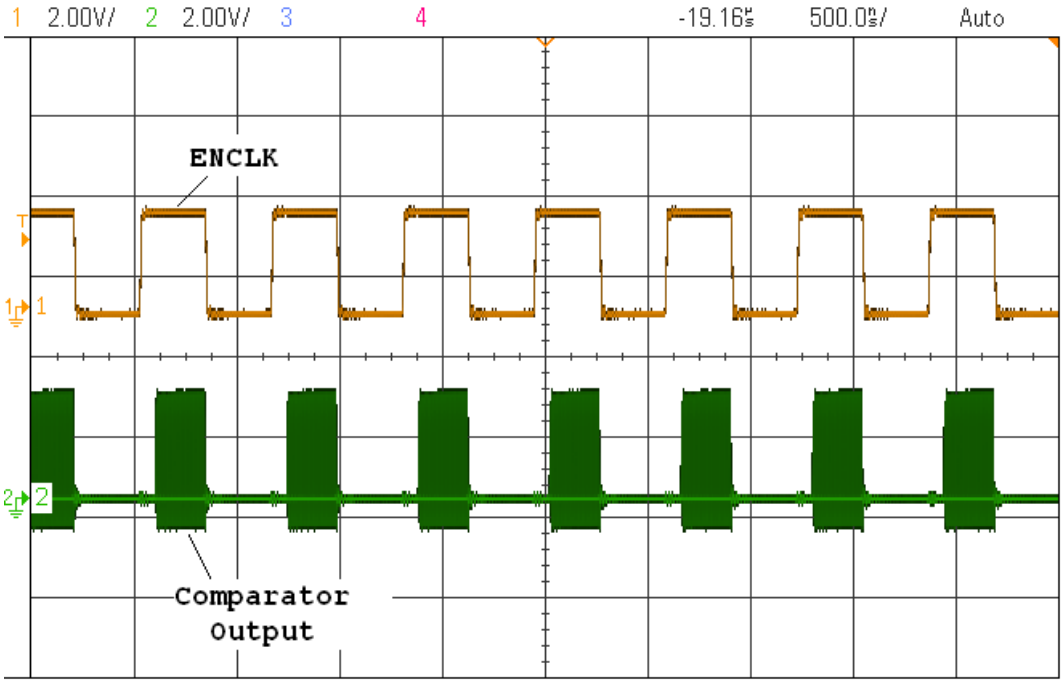

Figure 4.10: ENCLK and comparator output.

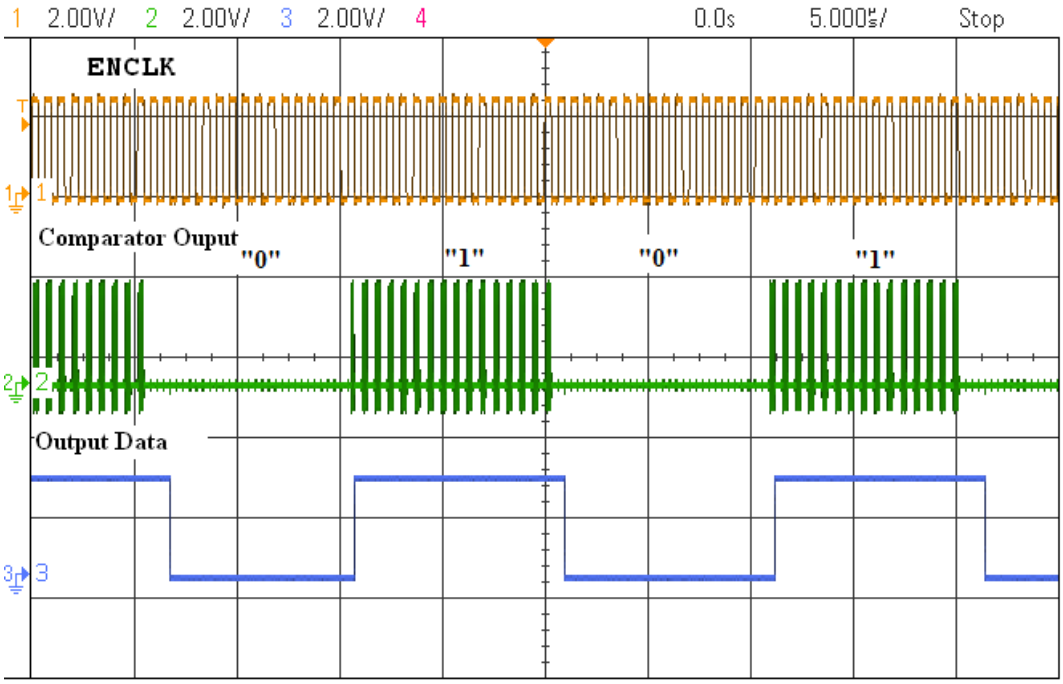

Figure 4.11: Waveform according to bit sequence "101010" received.

that BER changes rapidly when input power changes around sensitivity level. It is predictable because when the output of the RF amplifier is lower than offset voltage of the comparator, there is no pulse stream at the input of the digital block. If the output of the RF amplifier is higher than offset voltage of the comparator, the reliability of the receiver operation mainly depends on digital processing. When input power is higher than -30 dBm, BER performance degrades because of non-linearity in the RF amplifier (Figure 4.13). However, BER of the receiver is still smaller than 1E-3 until -15 dBm of the input power. Figure 4.14 shows measured BER of the receiver with 20 dB gain setting. In this case, the receiver works reliably with BER $<$ 1E-3 from -32 dBm to 5 dBm of the input power (Figure 4.14).

We can see that with only 2-step gain setting of the RF amplifier, the prototype receiver can operate properly with the 50 dB range of input power from -45 dBm to +5 dBm.

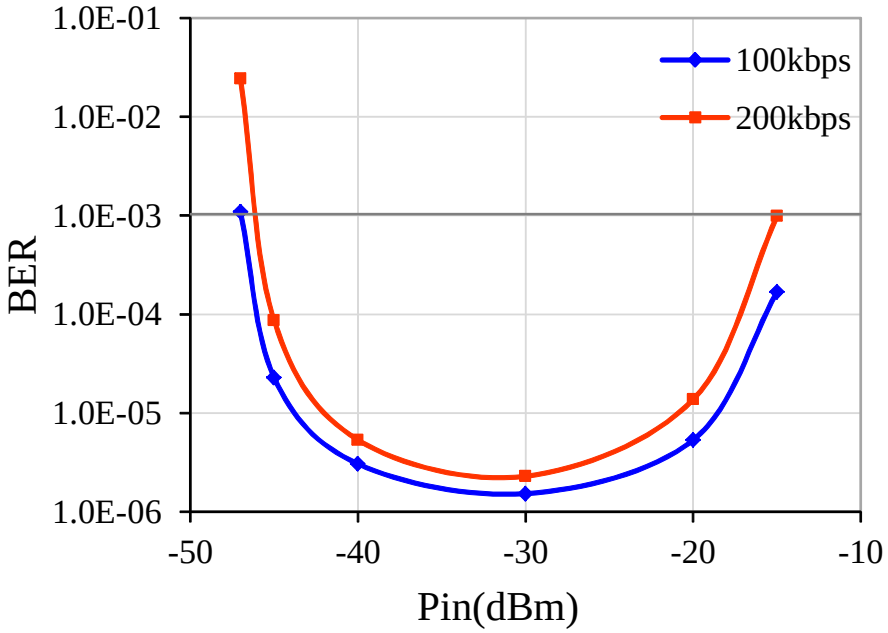

Figure 4.12: Measured BER at maximum gain setting.

Table 4.1: Resource usage of the digital circuit

Component	**Quantity**
Combinational ALUTs	13
FFs	14

Table 4.1 lists utilized resources for the digital circuit, including 13 ALUTs (adaptive look-up table) and 14 FFs (flip-flop). It shows that the digital part of the receiver is very simple, only a few of logic elements are utilized. Table 4.2 is the current consumption breakdown corresponding to two cases, with or without On-Off RF front-end. The RF front-end consumes almost total power while power consumption of the digital part is very small.

It can be seen that the proposed architecture of the receiver can be realized without any baseband amplifier, and when applying $ENCLK$ to the RF front-end, total power consumption is further reduced by approximately 42 %.

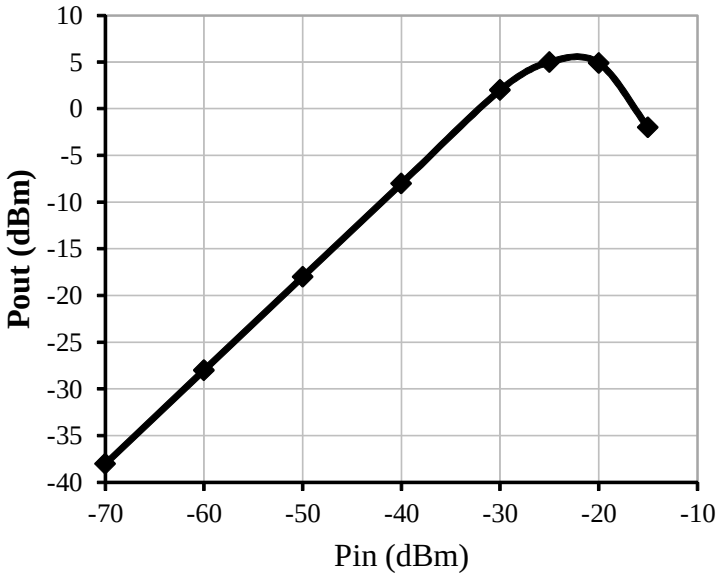

Figure 4.13: Nonlinearity in the RF amplifier with the maximum gain.

Table 4.2: Current consumption(mA)/3 V

	With ENCLK	**Without ENCLK**
RF Front-end	24.3	42.5
Digital	<1	<1
Total	≈25.3	≈43.5
Reduction (%)	42	0

4.4 VLSI Design on 65 nm SOTB CMOS Process

4.4.1 Circuit design

Figure 4.15 is the block diagram and schematic of the RF amplifier. In order to get high gain, the RF amplifier is implemented by cascading 5 stages. When applying $ENCLK$ to the amplifier, the transient will appear, generating noise and degrading performance. To solve this issue, differential topology is employed. The transient caused by $ENCLK$ appears in both outputs of differential stages, and they are compensated. The first stage is a single-ended-to-differential converter, next stages are fully differential. Current source tail is split into two halves connected by capacitor

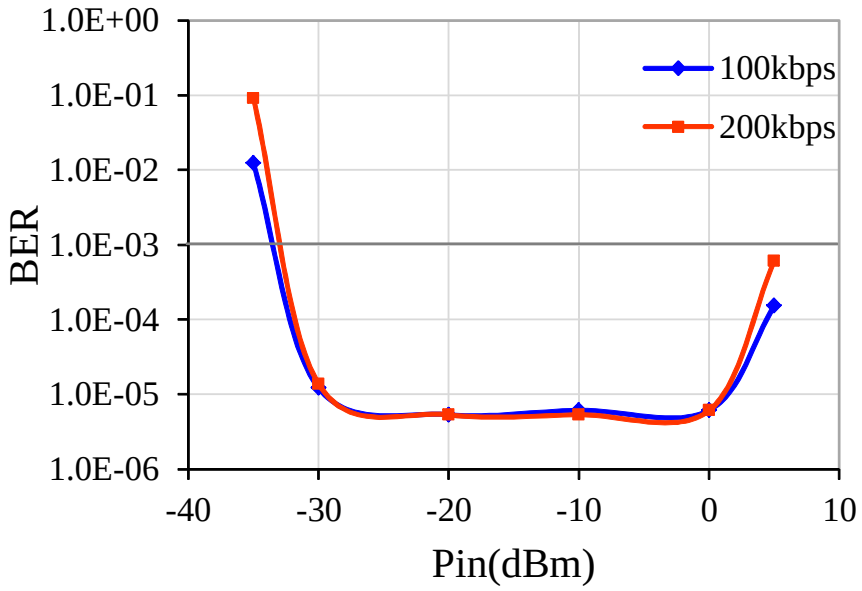

Figure 4.14: Measured BER at 20 dB gain setting.

C1 to suppress DC offset caused by asymmetry of devices. CMOS switches are added below current sources of each stage to enable or disable it. The first priority is low power. Therefore, we use shunt resistor method for input matching. Gain control is implemented by using a 3-bit digitally controllable PMOS resistor connected between output nodes, providing four gain settings. The RF amplifier consumes a current of 98 μA from the 1 V supply.

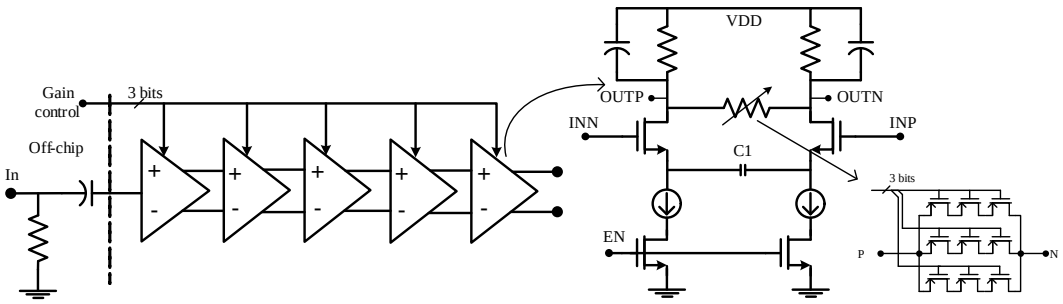

Figure 4.15: RF differential cascaded amplifier.

Schematic of the comparator is shown is Figure 4.16(a). It composes of a preamplifier followed by a variable threshold inverter. The preamplifier is a differential-

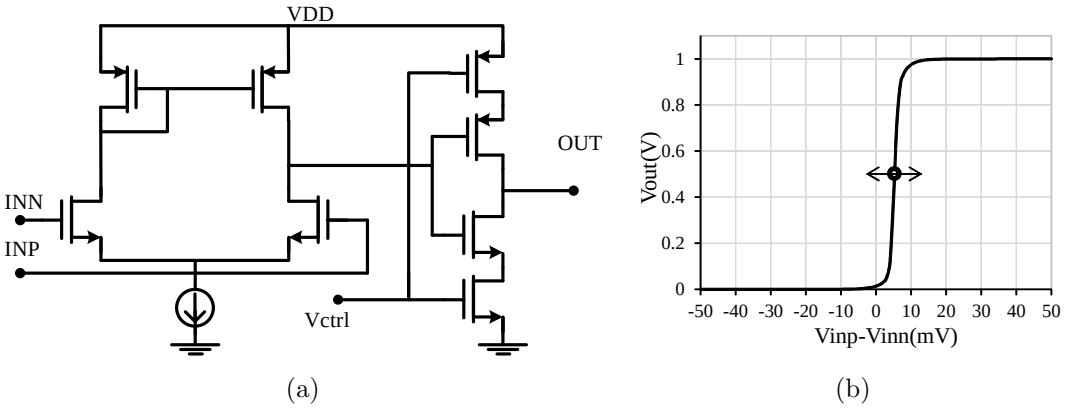

Figure 4.16: a) Schematic of comparator. b) Output characteristic.

input-single-ended-output type. Figure 4.16(b) is characteristic of the comparator. The threshold of the comparator can be adjusted to adapt with process variation. It consumes a power of 5 μW. Baseband digital circuit as described in Figure 4.4 is synthesized and laid-out automatically by IC compiler, occupying 35 x 40 μm^2 area and consuming only 0.56 μW. Figure 4.17 is layout picture of the receiver. The active core consumes an area of 320 x 188 μm^2.

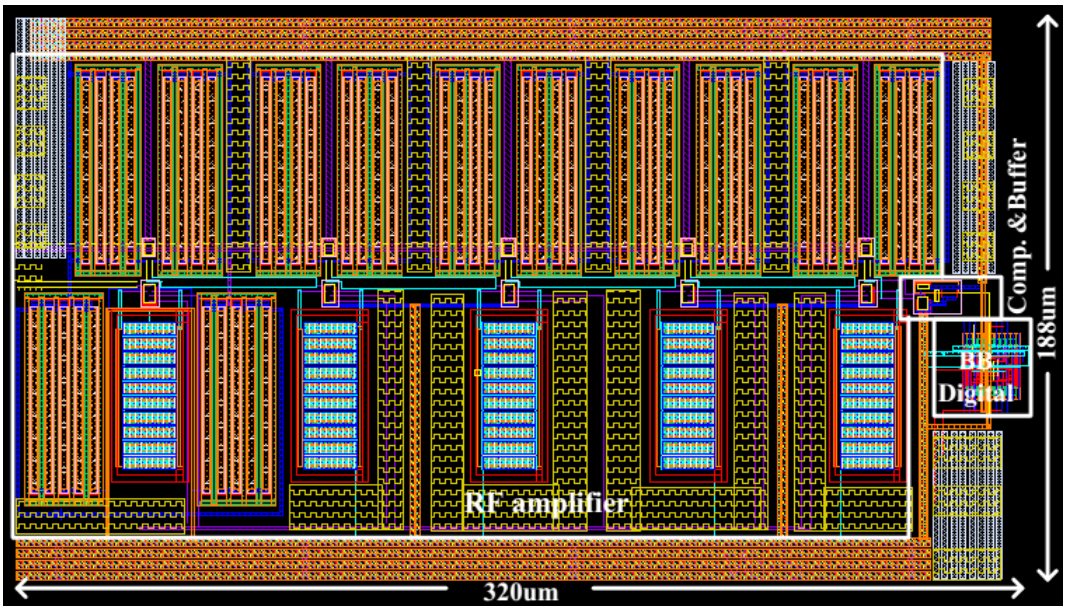

Figure 4.17: Layout picture of the receiver.

4.4.2 Simulation results

The simulation was implemented using netlist of the receiver with extracted parameters from the physical layout pattern. The simulated AC characteristic of the RF amplifier according to 4 gain settings is shown in Figure 4.18. It provides a digitally controllable gain from 15.8 dB to 59.7 dB at 315 MHz with approximately 15 dB each step.

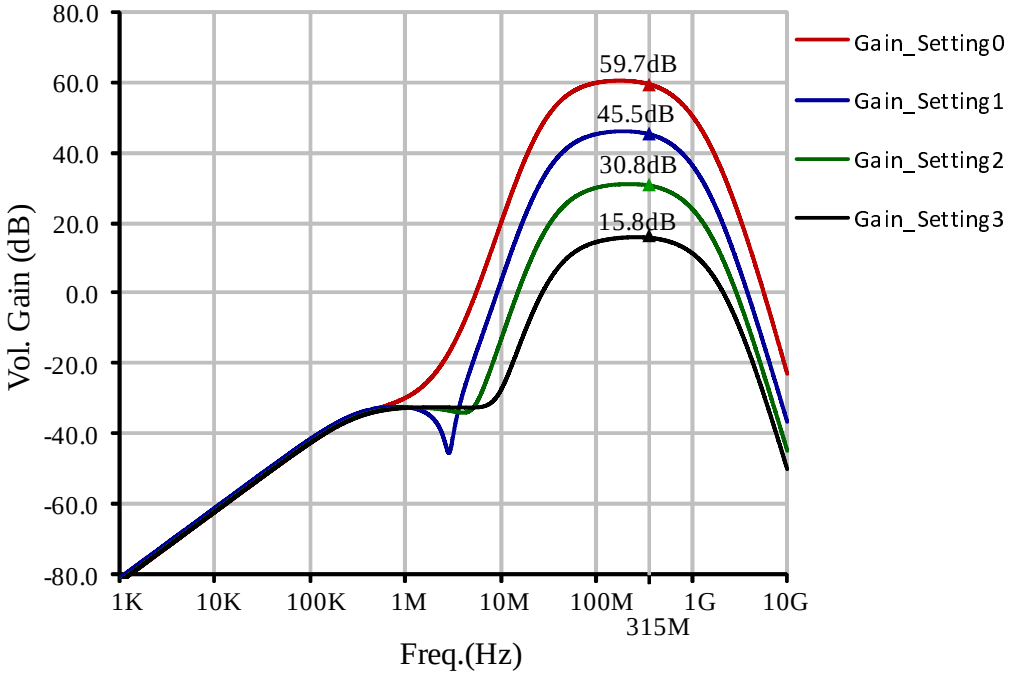

Figure 4.18: AC characteristic of the RF amplifier.

To examine linearity of the RF amplifier, its output is analyzed in the frequency domain. Power at the carrier frequency of 315MHz is calculated on 50 Ω load. Figure 4.19 is *Pout* vs. *Pin* plots with different gain settings. It can be seen that the RF amplifier can accommodate the range of input level up to -25 dBm, at which non-linearity phenomenon begins to appear with the smallest gain setting.

Figure 4.20 and Figure 4.21 show waveforms of the transient analysis at 200 kbps data rate with $ENCLK$ of 1 MHz 50 % and 20 % duty cycle respectively. In the

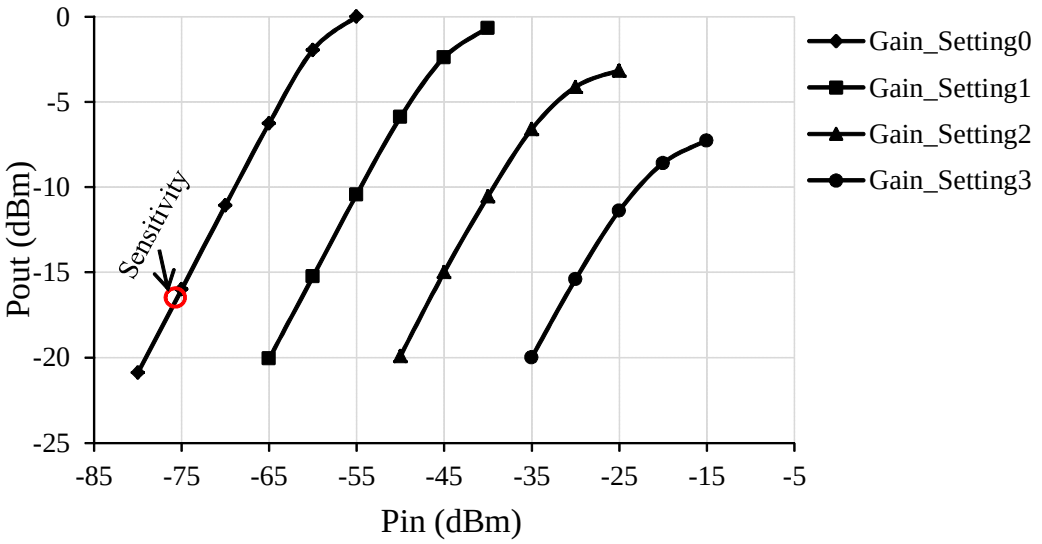

Figure 4.19: Pout vs. Pin plots.

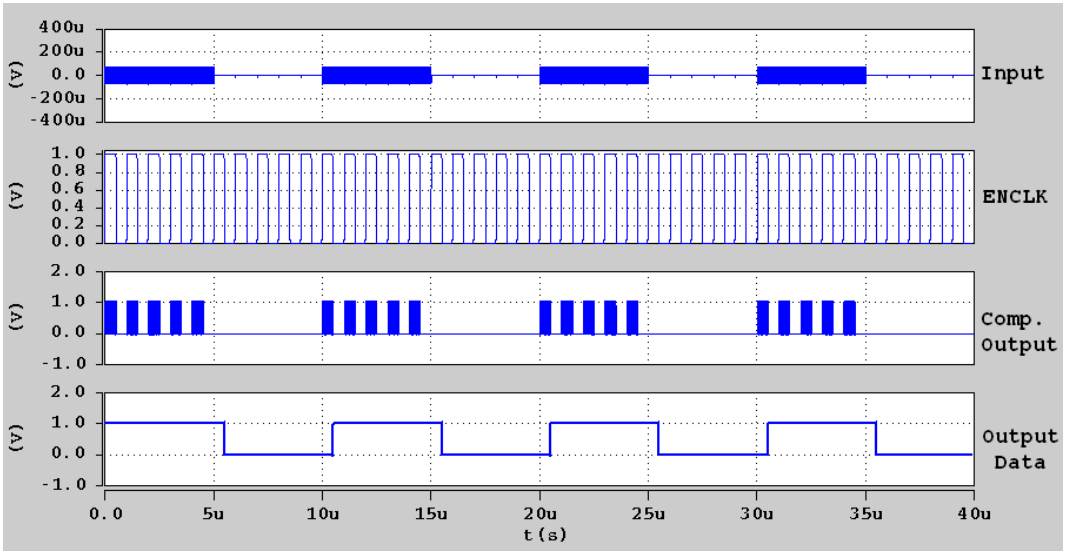

Figure 4.20: Transient analysis with -70 dBm input power, data rate 200 kbps, 50 % duty cycle ENCLK.

first case, average power consumption is 54.5 μW and further reduces to 27.6 μW in the case of 20 % duty cycle $ENCLK$. We can reduce the duty cycle of the ENCLK to reduce more power consumption. However, it is limited by the time constant of the circuit. With 1 MHz frequency, 20 % duty cycle corresponds to 200 ns, a value smaller than this number might cause the receiver not to operate. In the case of lower

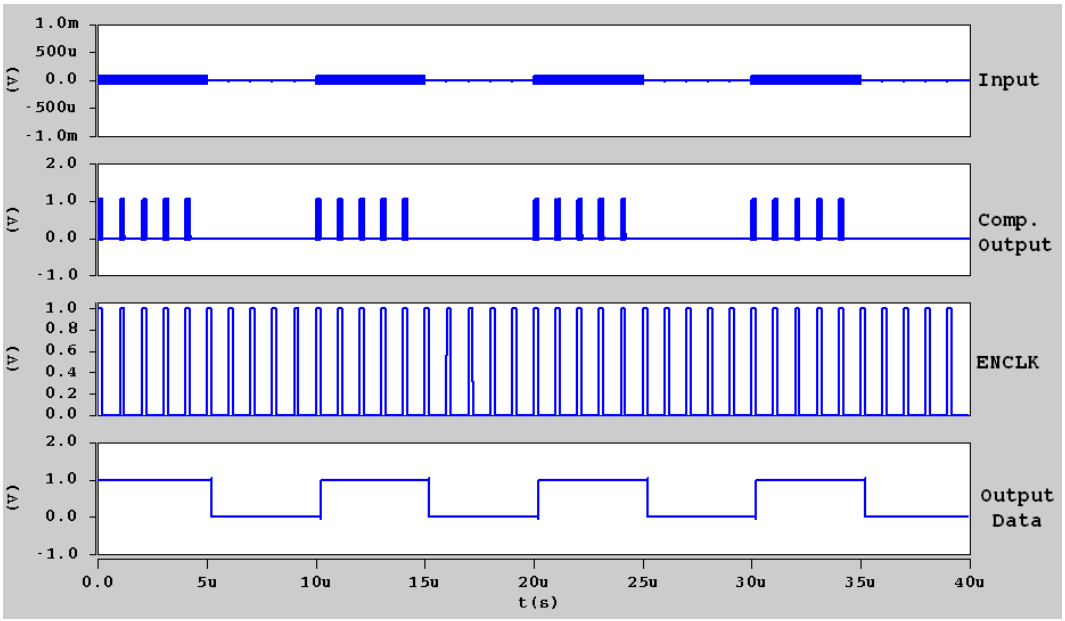

Figure 4.21: Transient analysis with -70 dBm input power, data rate 200 kbps, 20 % duty cycle ENCLK.

data rate, we can increase period of the $ENCLK$, and then reduce its duty cycle, resulting in further decrease of power consumption.

Sensitivity of the receiver is calculated by following equation [19]:

$$Pin_{min} = -174 + 10\log BW + NF + SNR, \tag{4.1}$$

where Pin_{min} is expressed in dBm, BW is bandwidth (Hz), NF is noise figure (dB) and SNR is signal-to-noise ratio (dB). The noise of the receiver is mostly caused by the RF amplifier and the preamplifier of the comparator. With maximum gain setting of the RF amplifier, they contribute a noise figure of 28.6 dB at 315 MHz (Figure 4.22). The SNR required to detect bits reliably is typically 12 dB. If using a 500-kHz-bandwidth off-chip bandpass filter at the input, sensitivity of the receiver can be derived:

$$Pin_{min} = -174 + 10\log(5 \times 10^5) + 28.6 + 12 \approx -76.4 \quad dBm$$

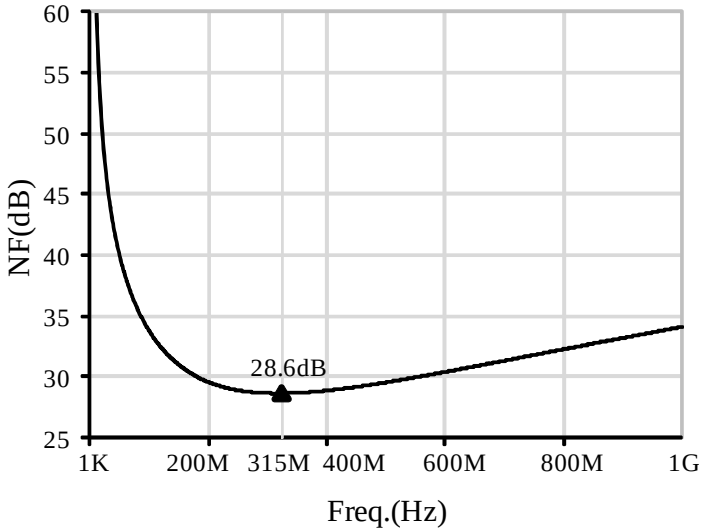

Figure 4.22: Simulated noise figure.

Table 4.3 shows a summary of the performance of the receiver. To evaluate the effectiveness of the proposed architecture, we assume that the comparator and the digital circuit in Figure 4.2 are replaced by the envelope detector and the baseband amplifier in Chapter 3, the RF amplifier operates continuously. The receiver becomes a conventional RF detection receiver (Figure 4.23). Total power consumption of the

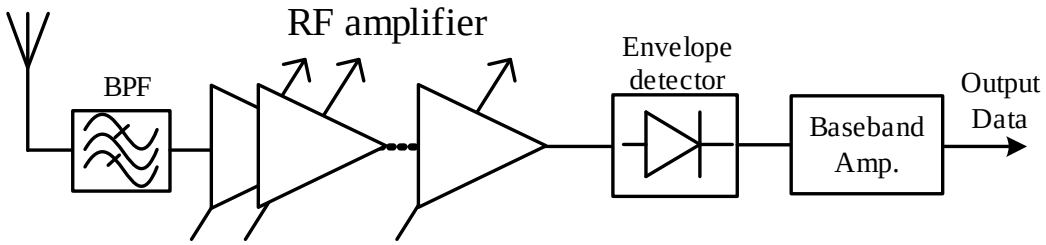

Figure 4.23: Conventional OOK receiver

receiver in this case is:

$$P_{total} = P_{RFamp} + P_{env} + P_{BBamp} = 98 + 0.6 + 3.3 = 101.9 \quad \mu\text{W}$$

The power dissipation of both architectures is shown in Table 4.4 and Figure 4.24. From the figure, we can see the power reduction given by the proposed architecture.

Table 4.3: Performance summary

Parameter	**Value**
CMOS Technology	65 nm SOTB
Supply (V)	1
Frequency (MHz)	312-315
Modulation	OOK
Data rate (kbps)	200
Sensitivity (dBm)	-76.4
Power (µW)	27.6
Energy/bit (nJ/bit)	0.138

Table 4.4: Breakdown on power consumption of conventional receiver and proposed receiver

Conventional RX		**Proposed RX**	
Circuit	Power (µW)	Circuit	Power (µW)
RF amp.	98	Intermittent RF amp.	22
Env. Detector	0.6	Comparator	5
BB amp.	3.3	Digital	0.56
Total	**101.9**	**Total**	**27.6**

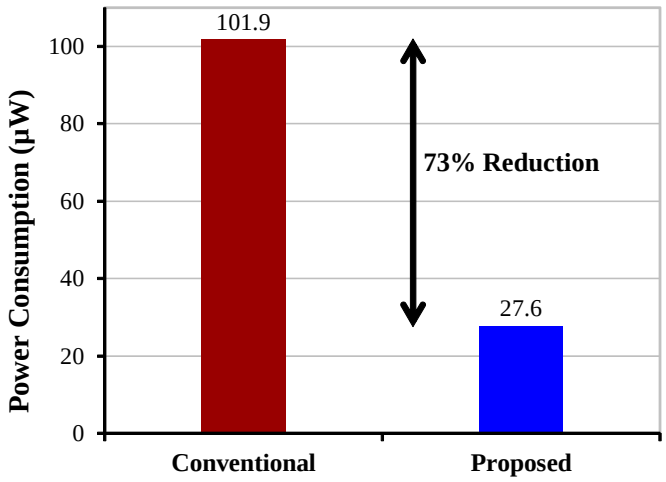

Figure 4.24: Power consumption of the conventional and proposed receivers

4.5 Conclusion

In this chapter, the OOK receiver operating in 315 MHz frequency band was presented. A novel architecture is adopted instead of the conventional RF detection receiver. A comparator together with a simple digital circuit undertakes demodulation task of the receiver. The architecture was verified by discrete RF modules and FPGAs before designing on the CMOS circuit. With VLSI design on the SOTB CMOS technology, the receiver can achieve -76.4 dBm sensitivity with power consumption of only -27.6 μW from 1 V supply at 200 kbps data rate.

Chapter 5

Synchronized-OOK Modulation Scheme and Receiver for Batteryless Short-Range Applications

In chapter 3 and chapter 4, a technique was used to overcome the trade-off between power consumption and sensitivity, in which the receiver uses cascaded RF amplifiers to achieve high sensitivity and the RF amplifiers operate intermittently to decrease power consumption. However, speed of intermittent operation must be higher than data rate several times because of asynchronization between transmission and reception. As a result, data rate is limited, and power consumption of the RF amplifier is still large in comparison with that of subsequent blocks.

In this chapter, we propose the synchronized-OOK (S-OOK) modulation scheme and an S-OOK receiver architecture operating in the 315 MHz frequency band for the short-range WSN applications. The S-OOK modulation allows received data to be synchronized with output clock using a simple digital circuit, no separate clock

and data recovery (CDR) circuit is required. Furthermore, the RF front-end works intermittently with intermittent speed as double of data rate despite asynchronization between transmission and reception sides, reducing further power consumption of the receiver so that it can be used for batteryless sensor nodes.

5.1 S-OOK Modulation

5.1.1 Format of S-OOK signal

Transmission signal used for this receiver is the S-OOK signal. The S-OOK pulse modulation was first proposed in [52] for Impulse Radio Ultra-Wide Band (IR-UWB) transceivers. Here we modify it for narrow band applications. Figure 5.1 shows format of the transmission signal, in which T_b is bit duration. In the conventional OOK modulation, RF carrier occupies whole duration of bit "1" and absents in the whole bit "0" (Figure 5.1a). On the other hand, in the S-OOK modulation, RF signal is composed of two kinds of RF pulses, synchronization pulses and data pulses. Bit "1" corresponds to 2 RF pulses. The first one is synchronization pulse, and the other is data pulse. Whereas bit "0" corresponds to only synchronization pulse (Figure 5.1b). The cycle of the synchronization pulses is T_b, equal to the bit duration. Each RF pulse has the width of T_p. T_p must be large enough so that the signal is still narrow-band, different from the signal described in [52], where each pulse is an ultra-wide band pulse. The distance between synchronization and data pulses in [52] is a certain value between 0 and T_b while this distance must be half of T_b in our architecture.

5.1.2 S-OOK demodulation

The received data ($ODATA$) and the corresponding clock ($DCLK$) will be detected after getting the S-OOK baseband signal ($BBSIGNAL$). Figure 5.2 describes the

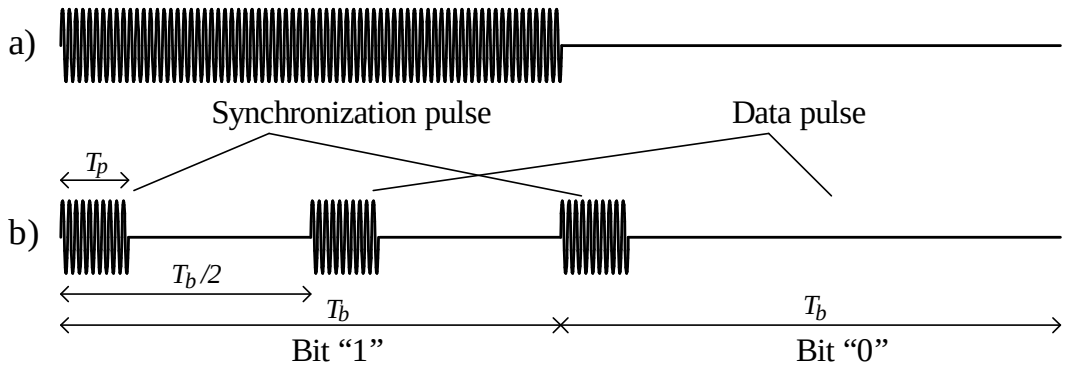

Figure 5.1: a) Conventional OOK signal. b) S-OOK signal.

timing chart of the S-OOK demodulation. In Figure 5.2, the timing relationships between edges of the signals are presented accurately. *ShortPulse* and *LongPulse* are generated synchronously with the rising edge of *BBSIGNAL*, in which *LongPulse* lasts longer than $T_b/2$ while *ShortPulse* lasts shorter than $T_b/2$. The output data *ODATA* can be obtained by latching *ShortPulse* using the falling edge of *LongPulse* and the clock *DCLK* is simply inverse of *LongPulse*.

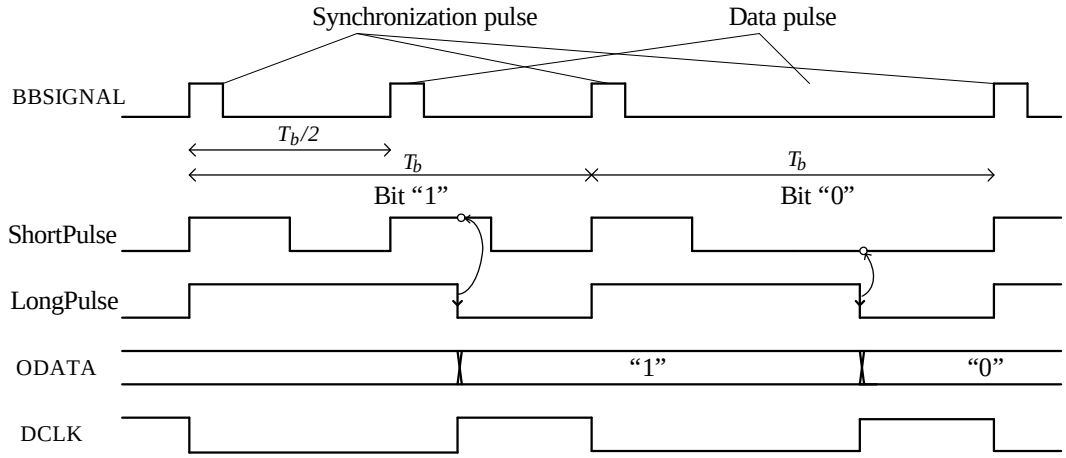

Figure 5.2: S-OOK demodulation.

5.1.3 S-OOK transmission

Figure 5.3 is the block diagram of the S-OOK transmitter, including the S-OOK modulator and the power amplifier. The timing chart in Figure 5.4 describes the operation of the S-OOK transmission. *Synchronization Pulse* and *Int Data Pulse* are generated based on the rising edge and the falling edge of the *Data Clk* respectively. After that the S-OOK modulation signal can be obtained by using an AND gate and an OR gate. This modulation signal controls the power amplifier to transmit the S-OOK RF signal. In this case, Data Clk must be 50% duty-cycle to make sure the Synchronization Pulse far from the Data Pulse $T_b/2$.

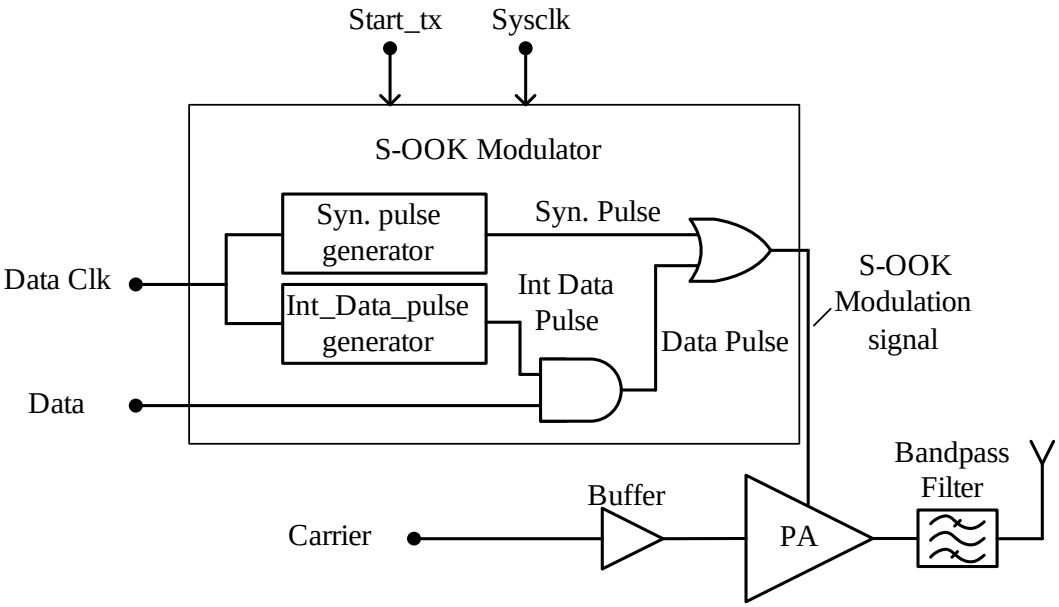

Figure 5.3: S-OOK transmitter.

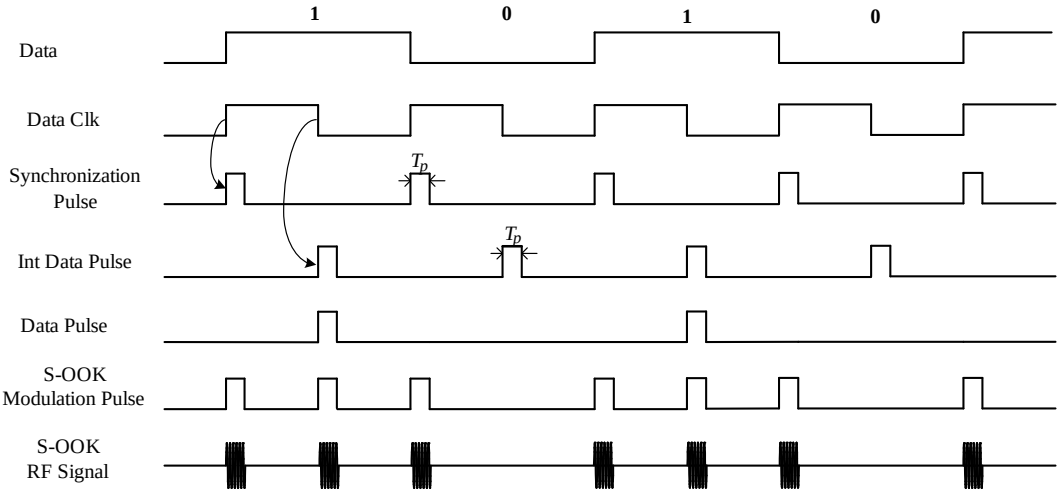

Figure 5.4: Timing chart of S-OOK modulation.

5.2 S-OOK Receiver Architecture

5.2.1 Receiver architecture

Figure 5.5 is block diagram of the proposed receiver, consisting of a variable-gain RF amplifier, a comparator and a digital part. The digital part includes a baseband extractor, a window generator and a demodulator & synchronizer. The receiver front-end is same with that of the receiver presented in Section 3.2. Therefore, no IF or baseband amplifier is needed. After the multi-stage cascaded RF amplifier, input RF pulses including synchronization pulses and data pulses are clipped by the comparator to become pulse groups with rail-to-rail level. The baseband extractor generates baseband signal, which is fed to the window generator and the demodulator & synchronizer. The window generator uses the baseband signal to create a window (*RFENA*) which enables the RF front-end in the period that covers the beginning part of each input RF pulse and disables it in other time. The demodulator & synchronizer extracts output data and synchronization clock for next processing. In this architecture, the digital part operates continuously while the RF front-end including

the RF amplifier and the comparator operates only when the *RFENA* window is high. Therefore, the power consumption of the circuits is reduced significantly.

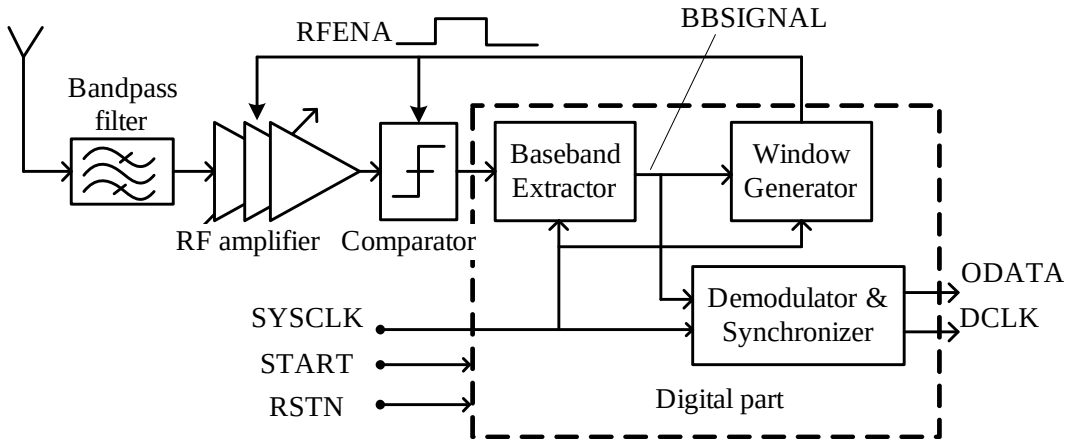

Figure 5.5: Block diagram of the proposed receiver.

5.2.2 Operation

Figure 5.7 describes detailed schematic of the digital part, in which the baseband extractor, the LongPulse generator and the ShortPulse generator have same schematic as shown in Figure 5.6. *NComparator* stands for the numerical comparator, used to differentiate from the comparator of the RF front-end.

The timing chart in Figure 5.8 describes the operation of the receiver. When *START* goes up, *RFENA* is high, enabling the RF front-end. The receiver is ready to receive input RF signal from the antenna (Figure 5.8b). The input RF signal is amplified by the RF amplifier, then directly converted to rail-to-rail pulse stream by the comparator (Figure 5.8c, d).

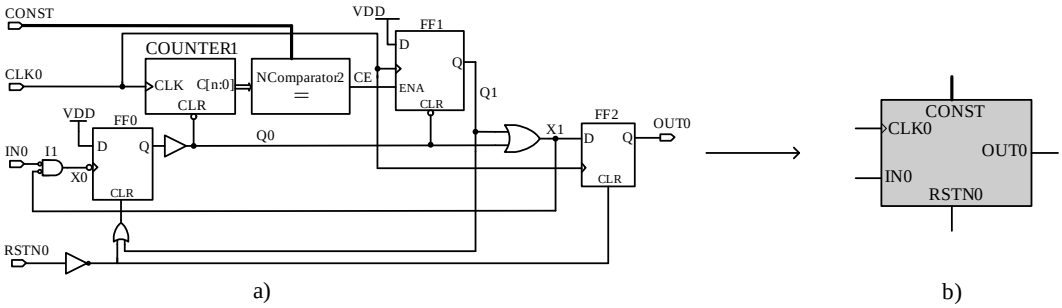

Figure 5.6: Schematic (a) and symbol (b) of the baseband extractor, LongPulse generator and ShortPulse generator.

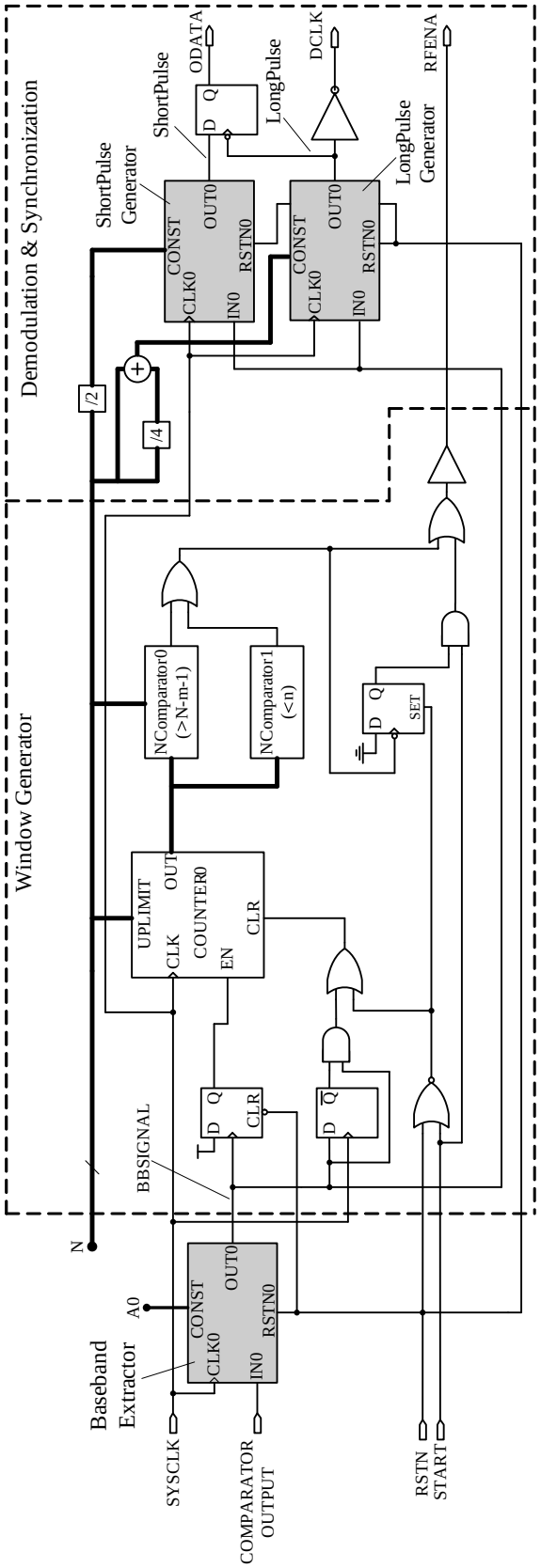

Figure 5.7: Schematic of the digital part.

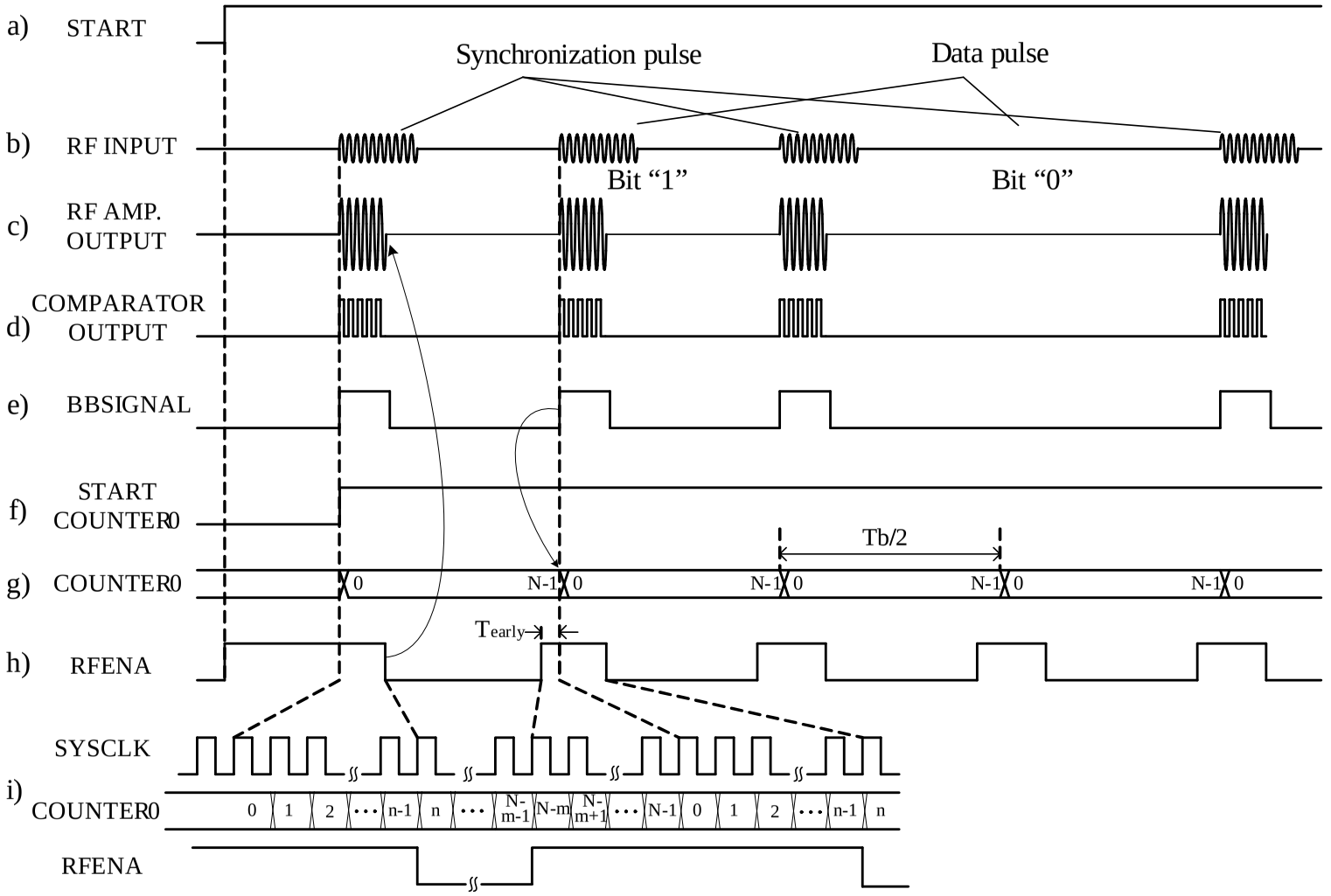

Figure 5.8: Timing chart for explaining operation.

Baseband extraction:

After the comparator, the baseband pulse chain is detected by the baseband extractor. Considering the circuit in Figure 5.6, it is almost same the circuit in Section 3.2.2. The *COUNTER1* is triggered by a rising edge at the *IN0* input. During the *COUNTER1* counting, the *OUT0* output is asserted and other incoming rising edges at *IN0* are ignored. *OUT0* is cleared only when the *COUNTER1* reaches an upper limitation value, which is assigned by the *CONST* input. For the baseband extractor, *CONST* is set by *A0* in Figure 5.7. At the output of the baseband extractor, we get baseband signal *BBSIGNAL* as shown in Figure 5.8e. *A0* is chosen so that the falling edge of *BBSIGNAL* is later than the last pulse of each input pulse group.

Window generation:

The first rising edge of *BBSIGNAL* will start the *COUNTER0* in the window generator, which operates based on *SYSCLK* (Figure 5.8f). When the *COUNTER0* reaches *N-1*, where $N = T_b/(2 \times T_{SYSCLK})$, it will be restarted by the rising edge of a *BBSIGNAL* pulse, which can be data or synchronization pulse (Figure 5.8g). In the case of bit "0", there is no data pulse, the *COUNTER0* will restart automatically when reaching *N-1*. At first, *RFENA* raises together with *START* to listen the input RF signal (Figure 5.8h). After that, *RFENA* is cleared if $COUNTER0 \geq n$ and set again if $COUNTER0 \geq (N - m)$, n and m are chosen so that the window *RFENA* has a desired width (Figure 5.8i). By that way, *RFENA* is generated to enable the RF front-end every time the input RF pulse is incoming. Since operation of the window generator is decided by the rising edge of the input RF pulse, the falling edge of *RFENA* can be set earlier than end of the input RF pulse to reduce active time of the RF front-end, resulting in further reduction of power consumption of the receiver.

Demodulation and synchronization:

After getting baseband pulses, data and corresponding clock are generated by the demodulator & synchorizer as presented in Section 5.1.2. *ShortPulse* and *LongPulse*

(Figure 5.2) are generated by the ShortPulse generator and the LongPulse generator, respectively (Figure 5.6). Their operation is same as the baseband extractor. The difference is only upper limitation values of the *COUNTER1* (*CONST*). In this case, *CONST* is set to $N/2$ and $N+N/4$ for *ShortPulse* and *LongPulse* respectively so that *ShortPulse* is shorter than $T_b/2$ and *LongPulse* lasts longer than $T_b/2$. Depending on desired data rate, N is assigned to a suitable value based on the equation $N = T_b/(2 \times T_{SYSCLK})$.

The solution that RF front-end is gated by a window pulse was presented in [53] for IR-UWB receivers. However, the receiver in [53] uses a delay-locked loop (DLL) with a digital controlled delay line, an SAR (successive approximation register) controller, a divider and a phase detector. It is very complex and consumes a large amount of power. They have to transmit many sub-bits for both bit "1" and bit "0" with known sub-bit period and use a clock signal to track the input pulse chain. Therefore, energy efficiency is limited. Moreover, a preamble transmission is also required to establish synchronization. In contrast, the solution presented here requires only a counter and two numerical comparators. Hence, the structure is very simple.

Although we do not use a close loop such as DLL to synchronize *RFENA* with the RF input, but *RFENA* is always generated timely by using S-OOK modulation. We will calculate the maximum frequency error between transmitter clock source and receiver clock source with that the window *RFENA* is still generated correctly.

RFENA is designed to rise at T_{early} before the input RF pulse (Figure 5.8h). Assume that variation of frequency for both receiver clock source and transmitter clock source is δ. It means maximum error between the transmitter and receiver clock sources is 2δ. Since the *COUNTER0* is reset and resynchronized at least once after every bit duration of T_b by the synchronization pulses, the maximum timing error is accumulated in only one bit duration. In the case that the incoming bit stream

contains only bit "0", after each bit duration, T_{early} changes a maximum amount:

$$\Delta T_{early_{max}} = \frac{1}{DR(1-\delta)} - \frac{1}{DR(1+\delta)} = \frac{1}{DR}\frac{2\delta}{1-\delta^2} \tag{5.1}$$

where, $DR = 1/T_b$ is data rate. If the desired $T_{early} = 2T_{SYSCLK}$ and it is allowed to vary from $1T_{SYSCLK}$ to $3T_{SYSCLK}$, following inequality is yielded:

$$\Delta T_{early_{max}} = \frac{1}{DR}\frac{2\delta}{1-\delta^2} \leq T_{SYSCLK} \tag{5.2}$$

For example, if *SYSCLK* is 25 MHz and data rate is 100 kbps, δ can be derived: $\delta \leq 2E-3$. In practice, this value is very relaxed. With typical crystals, frequency variation is around 20 ppm (part per million), i.e. 20E-6, much better than the allowed value as calculated above.

5.3 Architecture Verification

In this section, we describe the experiment to verify the proposed architecture. The Analog Device amplifier AD8369 and the Texas Instruments comparator LMH7220 are used for the RF front-end and the Altera Stratix IV FPGA is used for implementing the digital circuit. The Maxim switch MAX4636 is used to switch supply for the RF front-end (Figure 5.9). The digital part of the receiver is implemented to operate at data rates of 1 kbps, 5 kbps and 10 kbps. A 10 MHz clock is used for the system clock. The window *RFENA* has the width of 1.5 µs.

A 315 MHz all-digital transmitter is also implemented to communicate with the receiver. The block diagram of the transmitter is shown in Figure 5.3. The whole transmitter is implemented completely on an FPGA, similar to the transmitter in Section 4.3. Figure 5.10 and Figure 5.11 are waveforms and envelope of the output

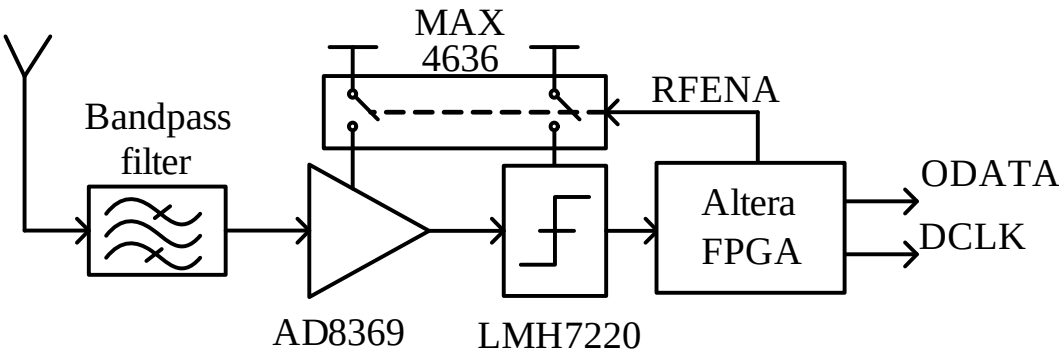

Figure 5.9: RX for verification.

spectrum of the transmitter respectively at 10 kbps data rate, each synchronization and data pulse has the width of 4 μs.

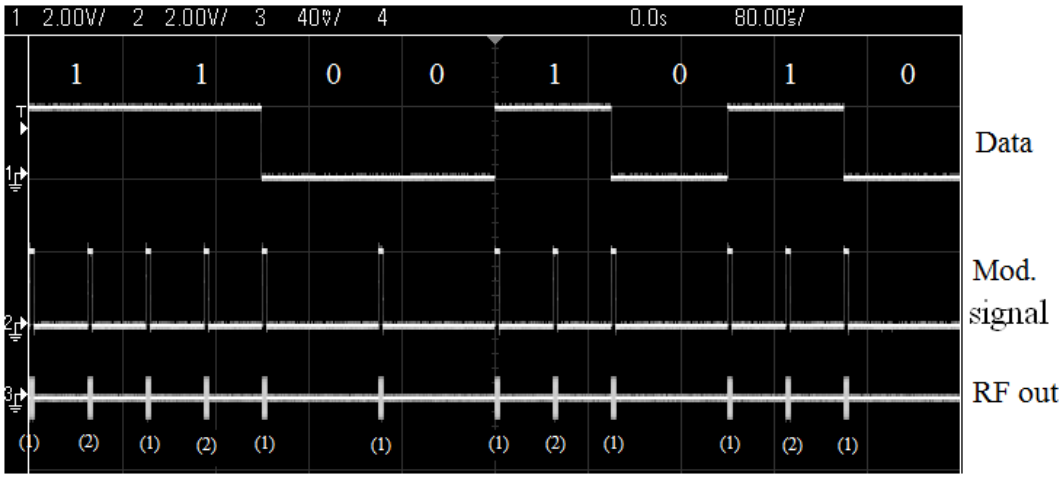

Figure 5.10: Output waveform of transmitter ([1]Synchronization pulse, [2]Data pulse).

Figure 5.12 shows experiment setup, in which the receiver and the transmitter communicate at a distance less than 1 meter. Figure 5.13 describes measured real-time waveforms of the receiver and corresponding transmitted data. It can be seen that the data is demodulated correctly with a delay smaller than one bit duration. Figure 5.14 is the measured BER characteristic of the receiver with different data rates. At 1kbps and 5kbps, $BER < 1E-3$ with $P_{in} \geq$ -45 dBm. At 10 kbps, $BER < 1E-3$ with $P_{in} \geq$ -44 dBm. We can see, when input power is larger than

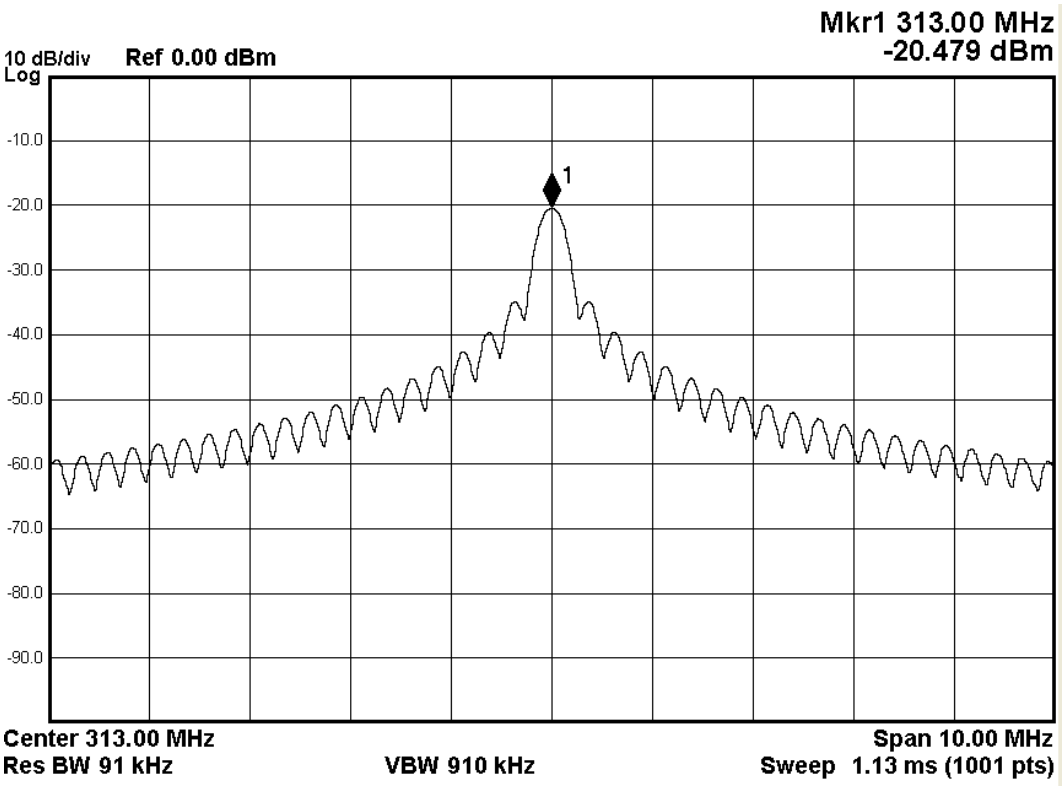

Figure 5.11: Output spectrum of transmitter.

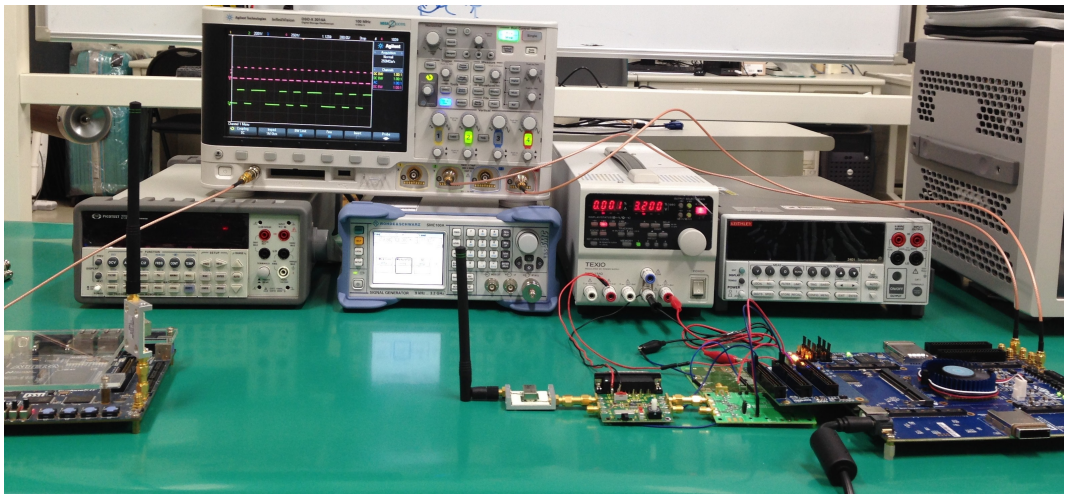

Figure 5.12: Experiment setup.

the minimum values, BER performance is almost same with different input levels. It can be explained that once the output of the RF amplifier is over the threshold of the comparator, reliability of the receiver mostly depends on the digital part. The

column diagram in Figure 5.15 is current consumption breakdown from 3.2 V supply of the RF amplifier and the comparator according to data rates of 1 kbps, 5 kbps and 10 kbps. Currents at normal operation are also shown for comparison.

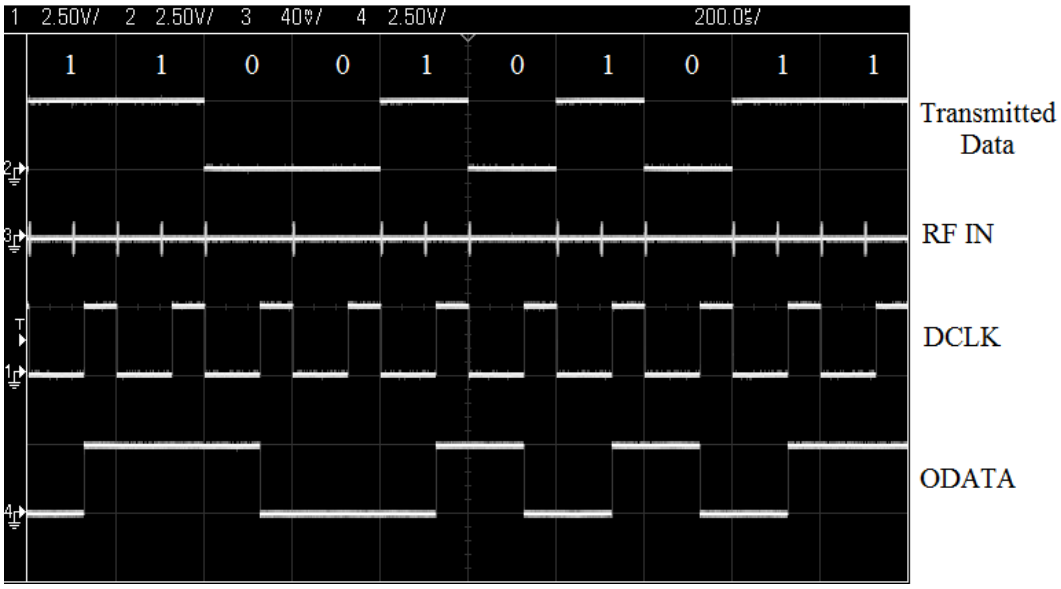

Figure 5.13: Measured real-time waveform.

It can be seen that, the receiver works properly ($BER < 1E-3$) with the range of input power from -44 dBm to more than 5 dBm. The RF circuits dissipate power much smaller than that of the conventional operation.

5.4 VLSI Design on 65nm SOTB CMOS Process

Schematic of the RF front-end circuit is shown in Figure 5.16. It is same as that of the receiver described in Section 4.4, except the preamplifier of the comparator, which is also added a switch below the current source tail. The RF gain can be tuned from 15.8 dB to 59.7 dB at 315 MHz with noise figure of 28.6 dB as shown in Figure 4.18 and Figure 4.22. The comparator includes a differential-to-single-ended converter and a variable threshold inverter. When enabled, the RF amplifier and the comparator consume a total current of 103 µA from the 1 V supply.

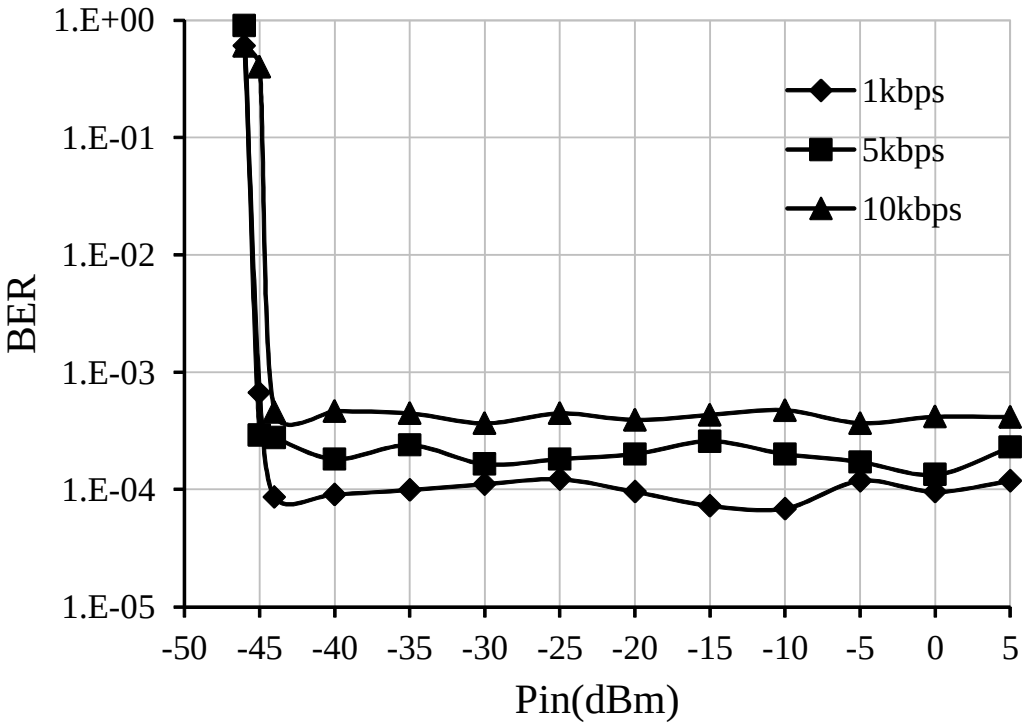

Figure 5.14: Measured BER performance.

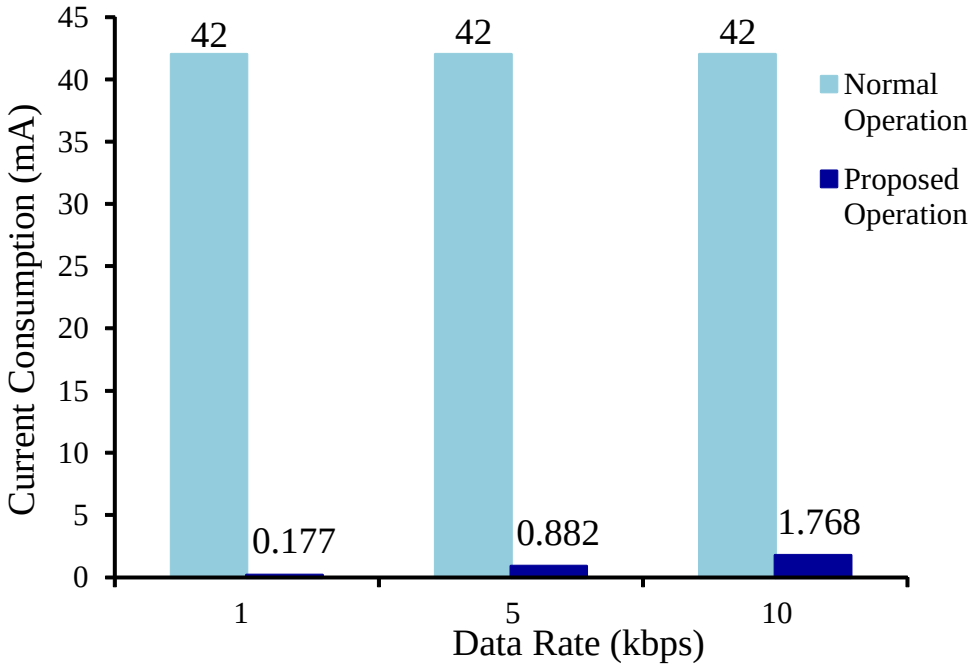

Figure 5.15: Current consumption of the RF front-end.

The digital circuit as described in Figure 5.7 is designed using standard-cell libraries. *SYSCLK* is 25 MHz; the *RFENA* window has the width of 360 ns. The data rate can be set to 100 kbps, 50 kbps or 10 kbps. The digital circuit of the receiver is supplied a voltage of 0.6 V, smaller than the supply voltage of the RF front-end to save power. It consumes a current of 0.98 μA. Figure 5.17 is the layout picture of the receiver. The active core occupies an area of 385 x 188 μm^2. The transient analysis result at 100 kbps data rate with input power of -70 dBm is shown in Figure 5.18. It can be seen that *RFENA*, *ODATA* and *DCLK* are generated properly, agreeing with the timing charts in Figure 5.8 and Figure 5.2. The graph in Figure 5.19 lists up the power consumption of the receiver at different data rates based on physical layout simulation. At the data rate of 10 kbps, the power consumption of the RF front-end is reduced to be comparable with that of the digital circuit, resulting in total 1.36 μW power consumption of the receiver. Similar to Chapter 4, we can compare the power consumption of the proposed S-OOK receiver with the conventional OOK receiver as shown in Figure 5.20. At the data rate of 10 kbps, the proposed architecture provides 98.6% power reduction in comparison with the conventional receiver.

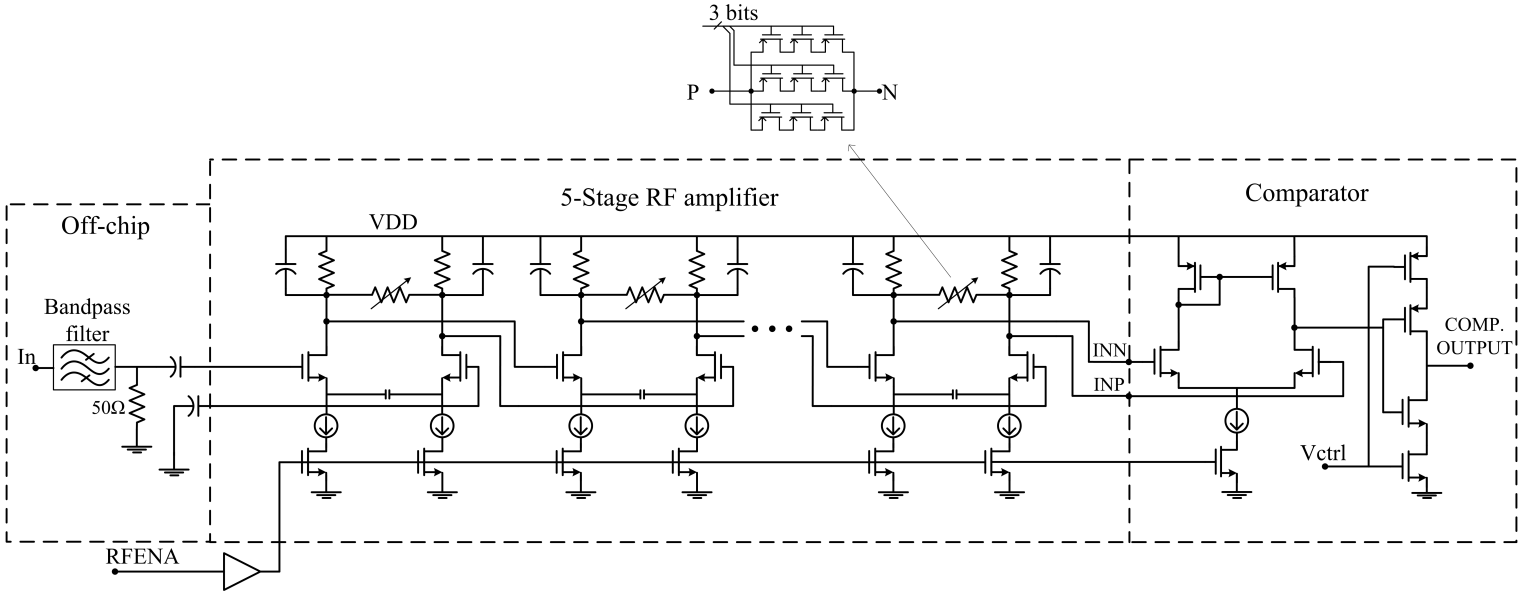

Figure 5.16: Schematic of the receiver front-end (biasing not shown).

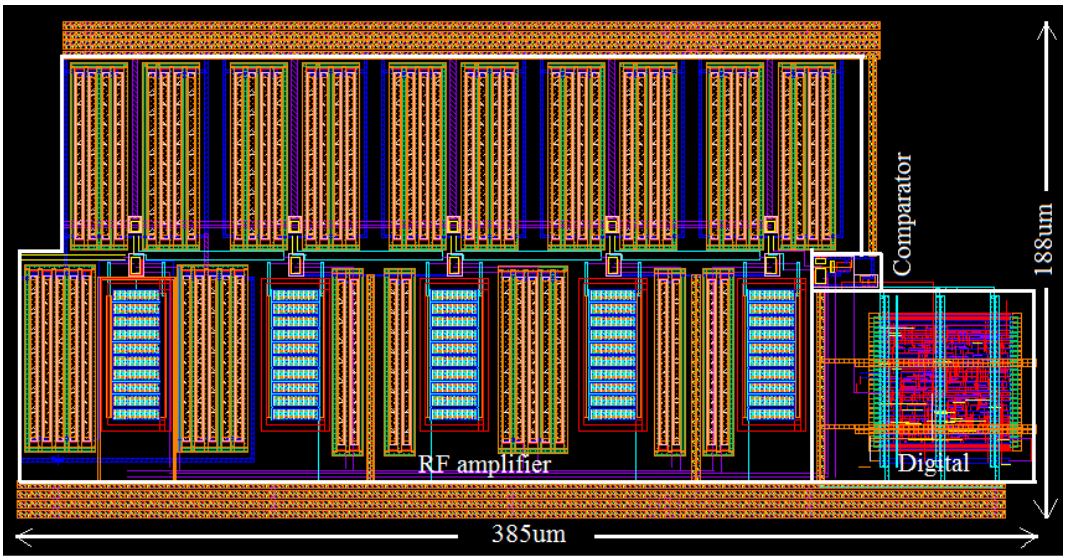

Figure 5.17: Layout picture of the receiver.

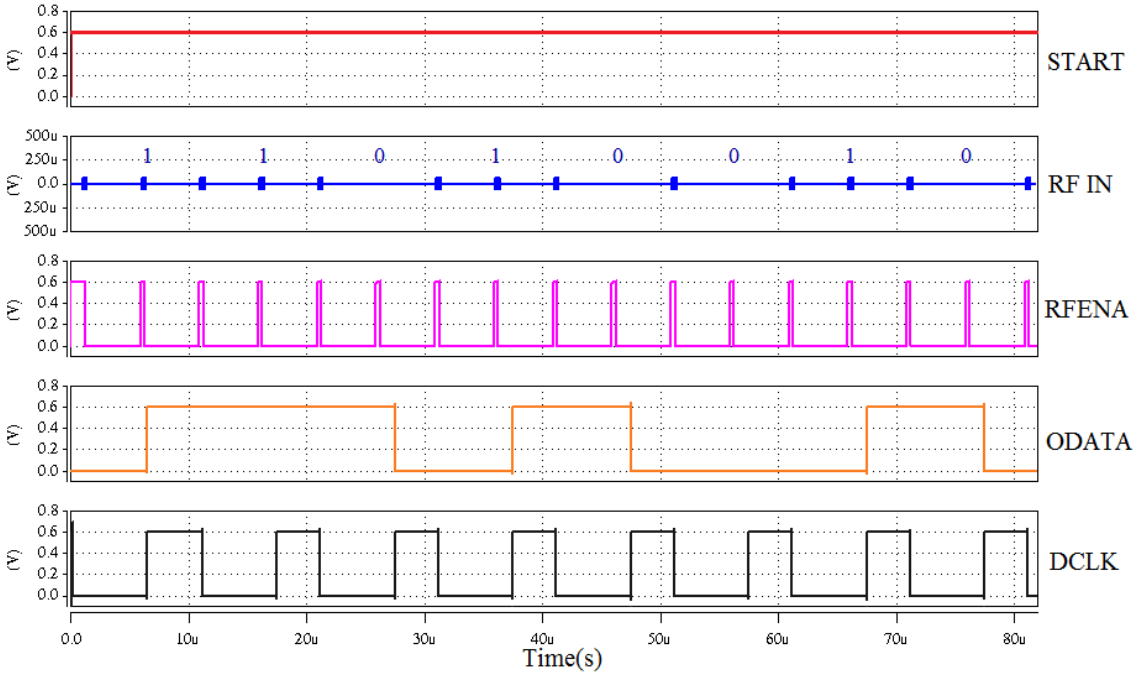

Figure 5.18: Transient analysis with -70 dBm input power, data rate 100 kbps.

Table 5.1 shows performance comparison between the proposed S-OOK receiver together with the OOK receiver presented in Chapter 4 and state-of-art receivers for the short-range applications. It should be noticed that the S-OOK receiver and the

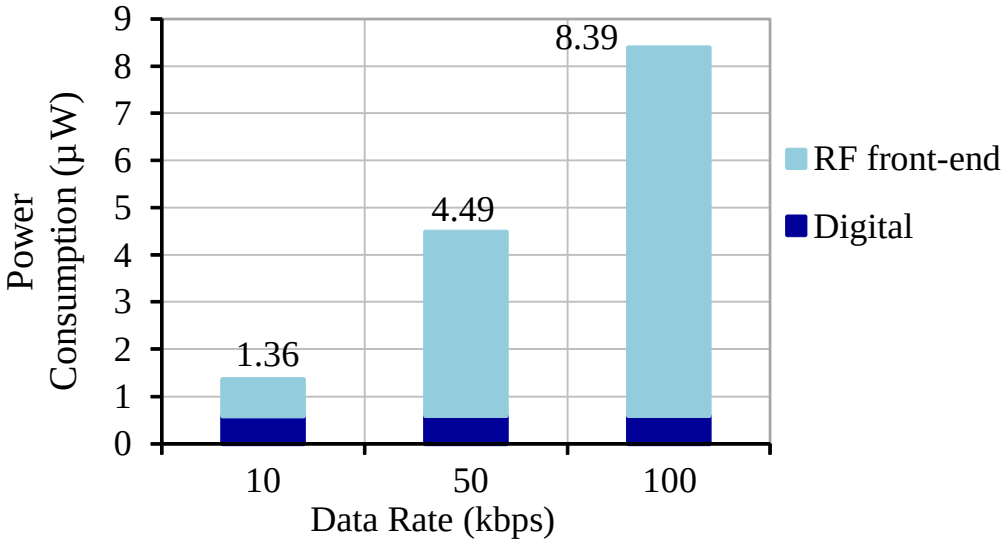

Figure 5.19: Simulated power consumption of the receiver.

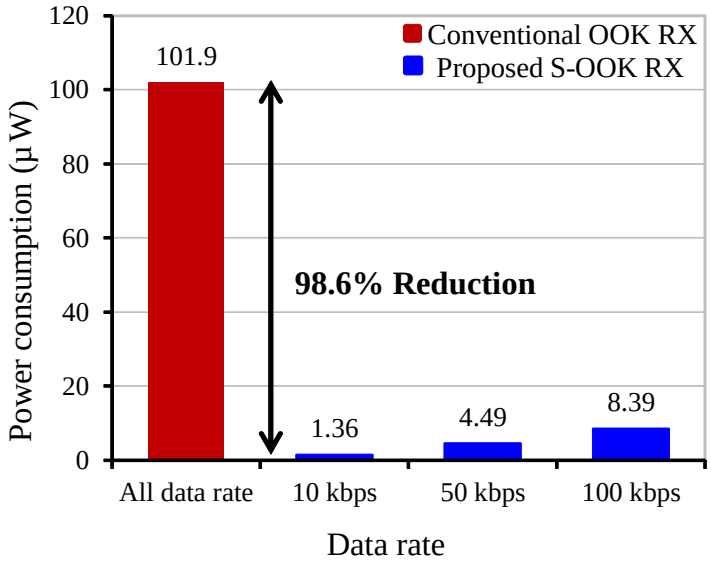

Figure 5.20: Power consumption of the S-OOK receiver and conventional OOK receiver.

OOK receiver with the proposed architectures consume much smaller power than that of others in the table. Especially, the power consumption of the S-OOK receiver is less than 10 μW with the data rate up to 100 kbps. Moreover, it does not require an additional circuit for clock and data recovery.

Table 5.1: Performance comparison

Parameter	**Ref[54]**	**Ref[55]**	**Ref[56]**	**Ref[57]**	**This work***	
					Chapter 4	Chapter 5
CMOS Technology	65 nm	90 nm	130 nm	90 nm	65 nm SOTB	
Supply (V)	0.3	0.5	1	0.8	1	
Frequency (MHz)	2460	2000	402	402-405	315	
Modulation	BFSK	OOK	FSK	OOK	OOK	S-OOK
With CDR	No	No	No	No	No	**Yes**
Data rate (kbps)	200	100	200	500	200	100/50/10
Sensitivity (dBm)	-91.5	-72	-70	-80	**-76.4**	**-76.4**
Power (μW)	1600	52	120	180	**27.6**	**8.39/4.49/1.36**
Energy/bit (nJ/bit)	8	0.52	0.6	0.36	**0.138**	**0.083/0.089/0.136**

*Simulation results

5.5 Conclusion

In this chapter, the S-OOK receiver operating the 315 MHz frequency band was presented. This is the first time S-OOK modulation scheme for narrow band applications was proposed. It allows to eliminate a complicated clock and data recovery circuit in the receiver. Furthermore, the RF circuits in the receiver can be heavily duty-cycled using a narrow window, which is generated in the digital part without a close loop and calibration thank to the presence of the synchronization pulse in every data bit.

The proposed receiver has some disadvantages, such as data rates can be set to only some predetermined values. With the S-OOK modulation, the data rate is also limited since one data bit needs two RF pulses. However, the proposed receiver can solve the trade-off between sensitivity and power consumption. High sensitivity can be achieved by using a high gain RF amplifier, but the power consumption of the RF amplifier and other analog circuits is minimized because of low duty-cycled operation. In this case, the power consumption of the digital part contributes a significant portion in total power dissipation of the receiver. It suggests that the power consumption of the receiver can be optimized by reducing supply voltage of the digital circuits. Because, in general, digital circuits can work reliably at supply voltage lower than that of analog circuits.

The proposed architecture was verified using some discrete components. The prototype was tested at data rates of 1 kbps, 5 kbps and 10 kbps. The experiment shows that the prototype operates reliably with the range of input power from -44 dBm to more than +5 dBm. Finally, VLSI design was carried out on 65 nm SOTB CMOS technology. By simulation, the proposed receiver achieves -76.4 dBm sensitivity, the data rate can be set to 100 kbps, 50 kbps and 10 kbps, consuming power 8.39 μW, 4.49 μW and 1.36 μW, respectively. It can be use with energy sources harvested from human temperature, human vibration or in-door light.

Chapter 6

Conclusion

6.1 Estimation of Communication Distance and Lifetime

In this section, we will estimate the communication distance for the proposed OOK receivers and S-OOK receiver. Following the Friis formula [58], the link budget equation can be written:

$$P_R = P_T + G_T + G_R - (L_P + L_T + L_R + L_M) \tag{6.1}$$

where:

- P_R = received power (dBm)
- P_T = transmitter output power (dBm)
- G_T = transmit-antenna gain (dBi)
- L_T = transmit-chain losses (coax, connectors, matching...) (dB)
- L_P = path loss (dB)
- L_M = misc losses (fading margin, body loss, polarization mis-match...) (dB)
- G_R = receiver antenna gain (dBi)

- L_R = receive-chain losses (coax, connectors, matching...) (dB)

In order to estimate possible communication distance, we assume that antennas of the transmitter and receiver have the gain of 0dBi, receive-chain loss, and transmit-chain loss are 3dB, fading margins are 15 dB and 20 dB for 315 MHz signal and 920 MHz signal, respectively. In free space, the path loss is calculated:

$$L_P = 20 \log \frac{4\pi d}{\lambda} \tag{6.2}$$

where d is the communication distance. In the 920 MHz band, the maximum transmission power is 24 dBm, with P_R = -82 dBm sensitivity, based on Equation (6.1) we have:

$$-82 = 24 - (20 \log \frac{4\pi d}{\lambda} + 26)$$

or

$$\log \frac{4\pi d}{\lambda} = 4,$$

Yielding d = 259 meters. In the 315 MHz band, the maximum transmission power is -6 dBm (Figure 4.1), with sensitivity = -76.4 dBm, similarly, we have d = 19 meters. Those distances meet the targets of this study.

The lifetimes of the receivers with corresponding batteries are shown in Table 6.1. It shows that the 920 MHz OOK receiver and the 315 MHz OOK receiver can last 1.45 years and 2.8 years respectively with the coin battery CR2032. Whereas, the 315 MHz S-OOK receiver with the minimum power consumption of 1.36 μW is suitable for batteryless systems.

Table 6.1: Lifetime of the proposed receivers

Receiver	**Power (μW)**	**Battery**	**Lifetime (year)**
920 MHz OOK Receiver	53	CR2032	1.45
315 MHz OOK Receiver	27.6	CR2032	2.8
315 MHz S-OOK Receiver	1.36	Batteryless	

6.2 Conclusion

With the objective is to look for solutions to minimize power consumption of receivers for extending the lifetime of sensor nodes while guaranteeing high sensitivity, this study proposed the novel receiver architectures, which help reduce power consumption significantly. In general, RF circuits are recognized as the parts that consume vast majority of the power of the receivers. Therefore, the proposed solutions focus on reducing power consumption of the RF circuits.

Taking advantages of low data rate of the WSN applications, the RF front-ends of the receivers are switched to operate intermittently, resulting in considerable power reduction. According to applications, a 920 MHz receiver and 315 MHz receivers were designed for long-range and short-range WSNs, respectively. Figure 6.1 and Figure 6.2 show the views of the performance of the proposed receivers with some state-of-art works in the same application areas.

In the 920 MHz OOK receiver, the RF amplifiers are applied a switched bias for intermittent operation. The baseband signal is recovered by the sample & hold circuit. In the 315 MHz OOK receiver, the RF front-end also operates intermittently for power reduction. In addition, the comparator and a simple digital circuit is used for demodulation without the envelope detector and baseband amplifier. The intermittent speed in those receivers must be higher than data rate several times because of asynchronization between transmission and reception. Furthermore, duty-cycle of the clocks that control the intermittent operation of the RF front-ends is limited by the time constant of the RF circuits. Therefore, power consumption cannot be reduced further at the same data rate.

Chapter 5 of this study proposed the receiver with S-OOK modulation, which allows to reduce intermittent speed to double data rate, minimizing active time of the RF front-end and eliminating the need of a clock and data recovery circuit. At 10 kbps data rate, the S-OOK receiver consumes 1.36 μW, which is the smallest power

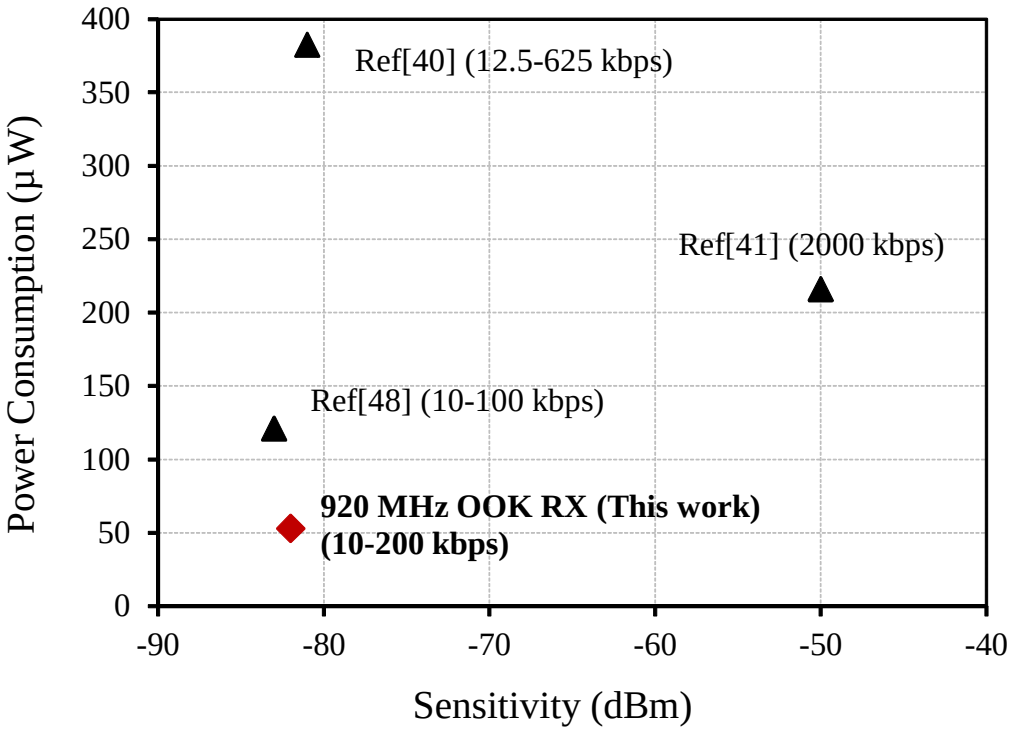

Figure 6.1: Power consumption vs. Sensitivity of Receivers for Long-Range WSNs.

consumption of receivers ever reported at the same data rate and sensitivity, suitable for batteryless sensor nodes. The sensitivity analysis indicates that the receiver can achieve -76 dBm sensitivity, which guarantees about 19 meters communication distance at the 315 MHz frequency band.

6.3 Future Work

Although the trade-off between power consumption and sensitivity is circumvented, however, the proposed receivers have some issues need to be improved in future.

For the 920 MHz OOK receiver, some off-chip high-Q inductors were used for the LC loads and the matching circuit. For high integration, they should be implemented on-chip. But the Q factor of the on-chip inductor is limited. In that case, the redundant low frequency signal caused by the bias clock may degrade the noise performance

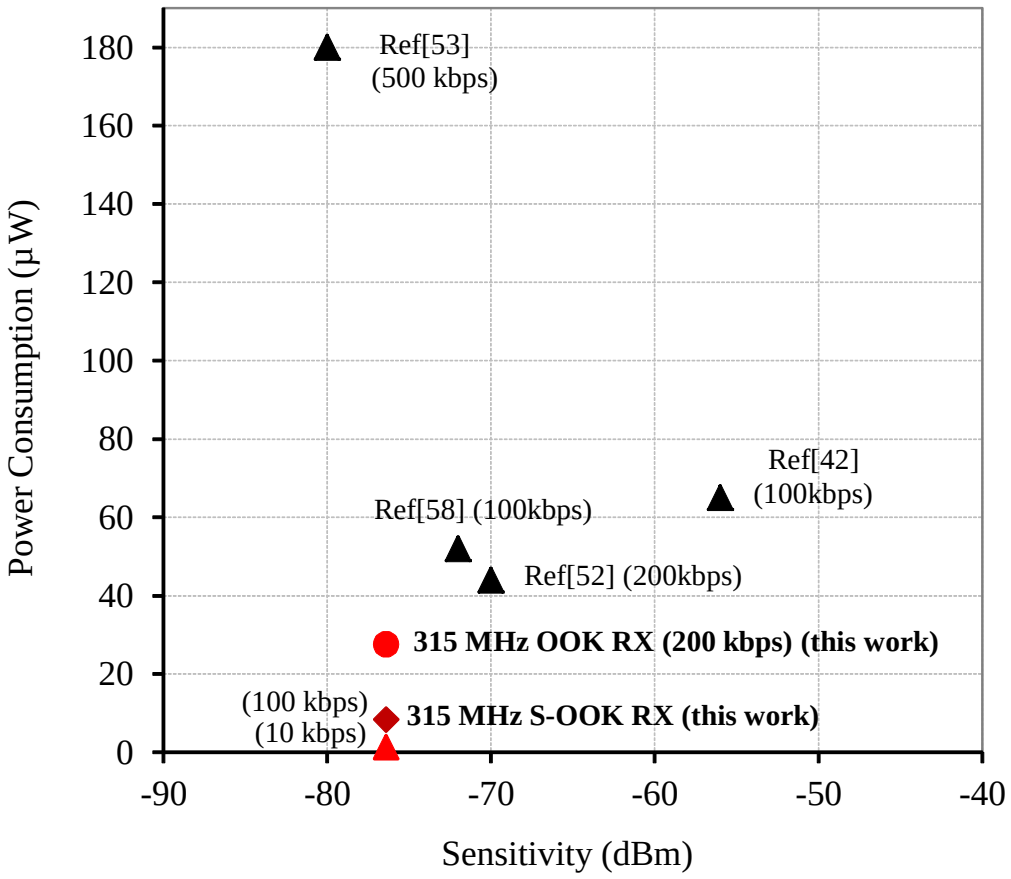

Figure 6.2: Power consumption vs. Sensitivity of Receivers for Short-Range WSNs.

of the receiver. In order to cancel that signal, the differential RF amplifier should be used instead of the current topology.

With the 315 MHz OOK receiver and the 315 MHz S-OOK receiver, the sensitivity is not so high. The high noise figure of the RF amplifier is a result of the shunt-resistor matching method. For the better sensitivity, other matching techniques should be employed to improve noise figure of the RF amplifier.

The RF amplifiers of the receivers have variable gains, which are adjusted when calibrating. In future, an Automatic Gain Control (AGC) circuits should be added to adjust gains automatically. Also, the power consumption of the receivers can be scalable with sensitivity for further power reduction.

In addition, the S-OOK modulation provides the great advantage in power reduction. Especially, the S-OOK receivers do not need a separate clock and data recovery circuit, which may consume the significant power. Therefore, using this kind of modulation scheme for other receiver architectures at different frequency bands should be considered in the future.

Appendix A

Characteristics of SOTB CMOS

This section is devoted to present some characteristics of the SOTB CMOS device. They are derived according to NMOS with L = 60 nm, W = 1 μm.

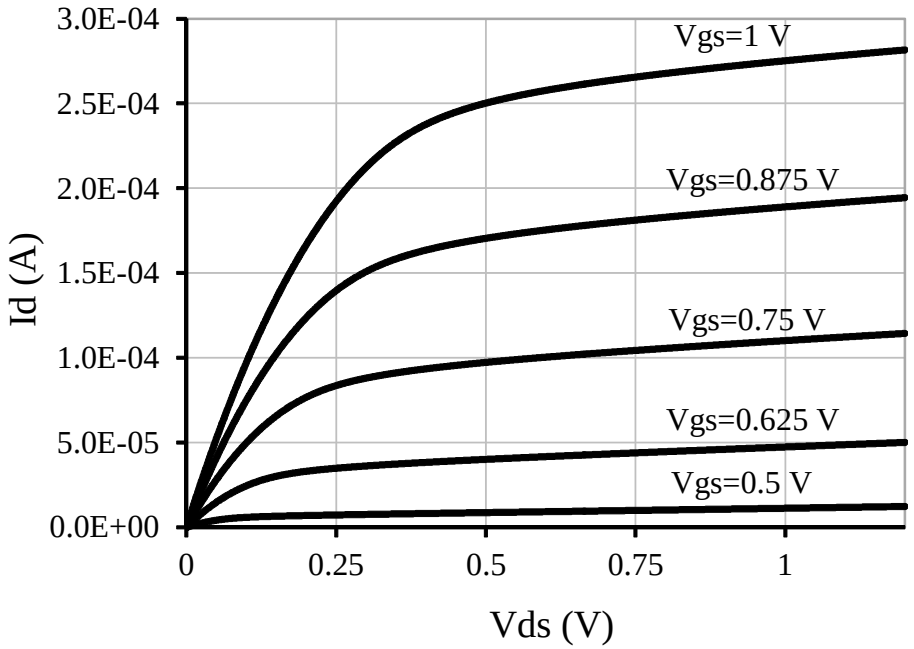

Figure A.1: I_d vs. V_{ds} Characteristic

It can be seen that, I_d and g_m of SOTB CMOS transistors can be changed by adjusting the body bias V_b, allowing to optimize performance of the circuits after fabrication.

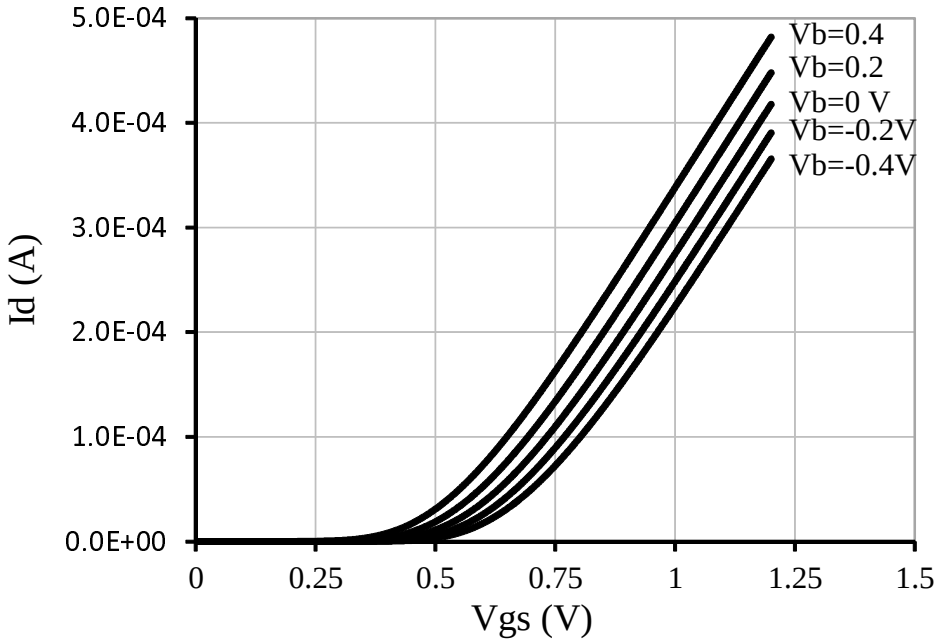

Figure A.2: I_d vs. V_{gs} Characteristic

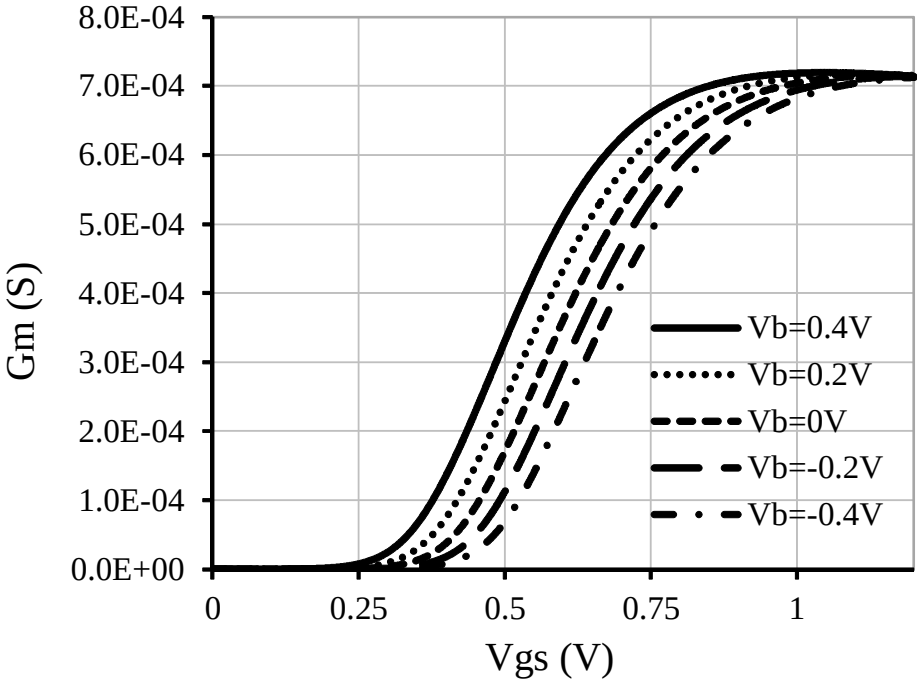

Figure A.3: g_m vs. V_{gs} Characteristic

Appendix B

List of Publications

B.1 Journal Papers

1. Minh-Thien Hoang, Nobuyuki Sugii and Koichiro Ishibashi, "A 27.6 μW 315 MHz Low-Complexity OOK Receiver with On-Off RF Front-End," IEICE Electronics Express, Vol. 12, No. 7, April 2015 (Published).

B.2 International Conference Presentations

1. Minh-Thien Hoang, Nobuyuki Sugii and Koichiro Ishibashi, "Ultra-Low Power LNA Design Using SOTB CMOS Devices," Thailand Japan Micro Wave (TJMW), Bangkok, Thailand, Dec. 2013.

2. Minh-Thien Hoang, Nobuyuki Sugii and Koichiro Ishibashi, "A 53 μW -82 dBm sensitivity 920 MHz OOK Receiver Design Using Bias Switch Technique on 65 nm SOTB CMOS Technology," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference, San Francisco, USA, Oct. 2014.

3. Minh-Thien Hoang, Nobuyuki Sugii and Koichiro Ishibashi, "A 0.75 V 0.574 mW 2.16 GHz - 3.2 GHz Differential Multi-pass Ring Oscillator on 65 nm SOTB

CMOS Technology," Integrated Circuits, Design, and Verification (ICDV), Hanoi, Vietnam, Nov. 2014.

4. Minh-Thien Hoang and Koichiro Ishibashi, "A 303 μW, 315 MHz OOK Receiver on 0.18 μm CMOS technology for wireless sensor networks," ASEAN-UEC symposium, Bangkok, Thailand, June 2015.

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