Synthesis and characterization of p-type $CuAlO_2$ by digitally processed DC sputtering (DPDS)

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This thesis marks the culmination of my journey at UEC Japan, encompassing both the roles of a dedicated student and a passionate researcher. At this moment, I wish to extend my deepest gratitude to my supervisor, Dr. Isshiki Sensei, whose guidance and support have been invaluable throughout my academic and research endeavors.

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In particular, I dedicate this work to my mom, whose untimely departure left a void that will forever be felt. I miss you, Mom, and this thesis stands as a testament to the enduring impact you had on my life.

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Abstract

The research focuses on synthesizing $CuAlO_2$ (CAO), a p-type transparent conducting oxide (TCO), using a novel approach called digitally processed DC sputtering (DPDS). This method employs a layer-by-layer (LBL) approach, offering precise control over deposition, which is crucial for achieving high-quality films. The study aims to enhance CAO film quality and field-effect mobility, addressing the increasing demand for wide-band gap metal oxides with high mobility in large-area electronic and optoelectronic devices.

The research first synthesizes Al-substituted $CuMnO_2$ via the sol-gel auto-combustion technique, examining its structural and dielectric behavior. It is observed that the dielectric constant increases with Al substitution, but the final CAO sample exhibits a polycrystalline nature. To improve the quality of CAO films, DPDS is employed for deposition on Si(100) and SiO_2/Si substrates, achieving a deposition rate of 0.57 nm/cycle. During deposition, non-radical oxidation is prioritized to prevent surface damage, and oxygen supply is synchronized with sputtering for saturation adsorption/oxidation. X-ray diffraction confirms the dominant CAO phase with highly oriented c-axis orientation for annealed CAO at 990°C. SEM analysis reveals morphological changes, with annealed samples showing larger grain sizes post-annealing. Bottom gate top contact thin-film transistors (TFTs) are fabricated using CAO thin films on SiO_2/Si substrates, employing shadow masking for precise patterning. Electrical characterization demonstrates p-type behavior in both annealed and as-deposited CAO TFTs, exhibiting a field-effect mobility of $4.1\,cm^2V^{-1}s^{-1}$.

The study highlights the feasibility and efficacy of DPDS-assisted LBL deposition for growing highly oriented CAO thin films, indicating their potential for application in p-type TFTs and addressing the need for wide-bandgap metal oxides with high mobility in large-area electronic and optoelectronic devices.

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Chapter 1

Introduction

This chapter explores the fundamental role of metal oxides in this dynamic field, particularly focusing on transparent conducting oxides (TCOs). Additionally, the chapter provides an overview of thin film transistors (TFTs) and their applications, highlighting their pivotal role in modern electronic devices.

1.1 Metal oxides and their importance in opto-electronics

Metal oxides (MOs) are compounds containing a metal cation and an oxide anion. MOs thin film and in bulk form exhibit wide functional properties, making them applicable in optoelectronic devices, solar cells, corrosion protection, transparent conductive oxides (TCOs), photonic integrated circuits, and many other applications as mentioned in Figure 1.1. It has been investigated that their properties strongly depend on crystal geometry, composition, doping, native defects, and synthesis techniques [1]. Metal oxide compounds usually have wide band gaps and localize electrons/holes, making them insulators. MOs are being investigated as a substitute for silicon electronics. The advancement of electronic and optoelectronic devices increases the demand for new features like high resolution, quick response, and transparency. In such context, semiconductor metal oxides (SMOs) such as zinc oxide (ZnO), aluminum-doped zinc oxide (AZO), indium-doped zinc oxide (IZO), and indium gallium zinc oxide (IGZO) are candidate materials for transparent, costless fabrication and high-performance electronics [2].

In TFTs, the mobilities in the SMOs channel layer are mostly higher than $10\,\mathrm{cm^2V^{-1}s^{-1}}$. On the other hand, the field effect mobility in a-Si can hardly reach anything higher than $1\,\mathrm{cm^2V^{-1}s^{-1}}$. Moreover, the SMOs present higher-film uniformity, lower-processing temperatures, and large-area applications [2].

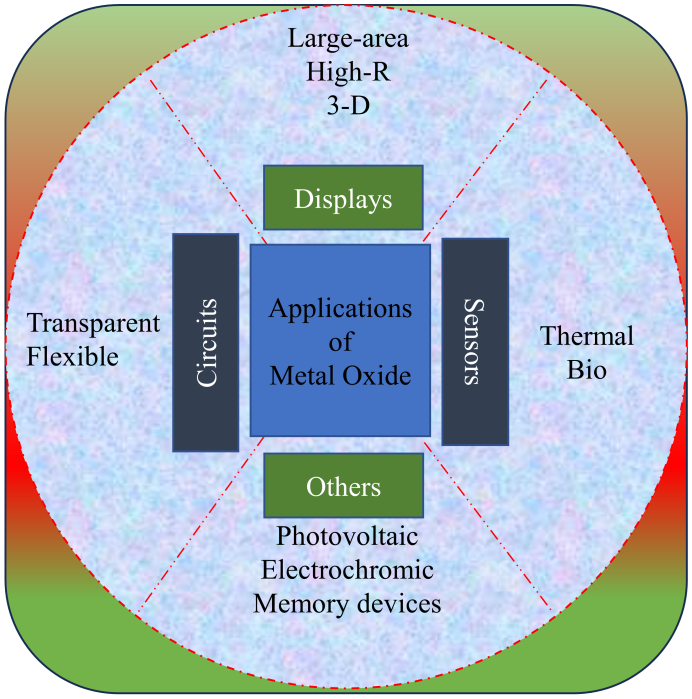

Fig. 1.1 Applications of metal oxide

1.1.1 Transparent conducting oxides (TCOs)

Oxide compounds with good electrical conductivity and high optical transparency are termed TCOs. Usually, they are extrinsically or intrinsically doped to minimize the resistive nature of high band gap (>3 eV) TCOs [3]. The first TCO was observed in Badeker's thermal oxidation of cadmium in 1907 [4]. The toxic nature of cadmium oxide (CdO) minimizes its interest in researchers. During the past decades, transparent electronics have been an exciting candidate for researchers and have made tremendous progress in such areas. TCOs have broad applications, from solar cells to transparent electronics; past and recent application of TCOs is depicted in Fig 1.2. The physics behind TCOs is their wide bandgap, which makes them transparent in the visible region. Most of the research has been focused on n-type TCOs. Due to the lack of a p-type counterpart as to n-type, the application of TCO became restricted, especially in developing p-n heterojunction devices. The first p-TCO was reported in CAO thin film by Kawazoe et al. in 1997 [5, 6]. TCOs can be classified into families based on their structure features as shown in the table 1.1 [7]. In addition, some essential criteria in the selection of TCO materials are tabulated as in 1.2.

Table 1.1 Examples of materials with different structural features and carrier types

Structural Feature	**Carrier Type**	**Examples**
Tetrahedrally-coordinated cations	n-type	ZnO
Octahedrally-coordinated cations	n-type	CdO, SnO_2, $CdIn_2O_4$, etc.
Linearly-coordinated cations	p-type	$CuAlO_2$, $SrCu_2O_2$, etc.
Cage framework	n-type	$12\,CaO \cdot 7\,Al_2O_3$

Table 1.2 Criteria for material selection in optoelectronics

General Criteria	**Optoelectronic Criteria**	**Processing Criteria**
Cost-effective	Transparent in the optical region	Compatibility with vacuum or non-vacuum processing
Nontoxic	Good conductivity	Green processing
Easy availability	High mobility with low carrier concentration	Temperature, and atmosphere sensitivity
		Chemical stability

Fig. 1.2 a) The concept of transparent display: early vision in 1936, b) LG Showcases Power of Transparent Displays at InfoComm 2023

1.1.2 Physics behind TCOs

Transparency and electrical conductivity are antagonistic to each other. Metallic materials with high electrical conductivity cannot transmit visible light; on the other hand, perfect transparent materials like glass are insulators. Conductivity is strongly coupled to the lossy part of the refractive index n. TCOs usually have a mid-range band gap.

Conductivity and electronic structure

Both metals and semiconductors express their electrical conductivity based on the electron-gas model. The electrical conductivity (σ), according to Boltzmann's relation, directly depends on carrier mobility (μ) and concentration (n) as follows,

$$\sigma = ne\mu \tag{1.1}$$

Here, the letter e represents the elementary charge. The n determines the carriers created by dopants or defects. While the mobility linearly depends on free carrier scattering time, τ (the time between resistive scattering events), and contrariwise on carrier effective mass (m^*) related by,

$$\mu = \frac{e\tau}{m^*} \tag{1.2}$$

The τ significantly depends on extrinsic factors (i.e., defects, dopants, etc.). At the same time, the intrinsic properties of materials can be determined from the electronic band structure while examining the changes in energy (ε) with momentum (k). High dispersive Valence Band Maximum (VBM) or Conduction Band Minimum (CBM) causes smaller effective mass, consequently giving rise to higher mobility [8].

In the case of indium tin oxide (ITO) (one of the renowned TCOs), the high conductivity is attributed to the shallow-donor/impurity states present close to the CB of the host In_2O_3, where the carriers undergo the host conduction band due to thermal ionization at room temperature. As a consequence of further doping numbers of current-carrying carriers, which enhance the conductivity, the band gap of the host is left intact so it doesn't lose its optical transparency [9].

Optical transparency

UV-vis spectroscopy determines the optical properties of TCOs by transmittance, absorptance, and reflectance spectra. Due to the wide optical bandgap, TCOs transmit light in visible and near-infrared regions. The free carriers in the Valence Band (VB) or Conduction Band (CB) for n-type TCOs oscillate with an applied field, like the free electrons in metals (plasma oscillations), significantly affecting absorption and reflection in the near-infrared region. Such phenomena in the near-IR region are explained based on classical Drude theory, where plasmon frequency (ω_p) is given by,

$$\omega_p^2 = \frac{ne^2}{m^*\varepsilon(\infty)\varepsilon_0} \tag{1.3}$$

where n is the free carrier density, m^* is the electron effective mass, $\varepsilon(\infty)$ is the high-frequency dielectric constant, and ε_0 is the permittivity of free space. For a particular electrical conductivity, the plasmon frequency of the free carriers sets a range of optimum transparency regions.

The insertion of additional holes in VB or electrons in CB causes higher concentration. As a result, in n-type TCOs, the electrons, after the absorption of photons, transition to higher states, and in p-type TCOs, the electrons in lower states transition up and recombine with the existing holes in the VB [8]. Such an optical transition is schematically shown in Fig 1.3. The new gap transitions also affect the transparency of TCOs.

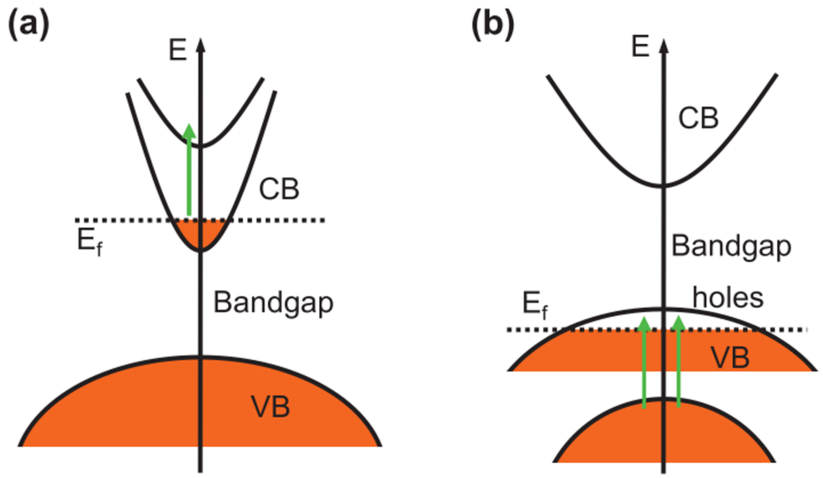

Fig. 1.3 New transitions in highly doped TCOs, as marked by green arrows; a) for n-TCOs, b) for p-TCOs [8].

n-type and p-type transparent conducting oxides

Emerging n-type TCOs include n-type Ga_2O_3, which is in demand for extensive bandgap applications. $BaSnO_3$ possesses the highest mobility ever measured, exceeding $120\,\mathrm{cm}^2/\mathrm{Vs}$ at room temperature, making it a desirable n-type material. Meanwhile, n-type amorphous-indium Gallium Zinc Oxide (a-IGZO) has become a good choice for Thin-Film Transistors (TFTs) due to its superior electrical features. Nomura and Hosono improved its performance, including high mobility of more than $15\,\mathrm{cm}^2/\mathrm{Vs}$, high I_{on}/I_{off}, and low subthreshold swing of less than $0.2\,\mathrm{V}$/decade, making it applicable as an active matrix in the display industry [10].

The n-type Transparent Conductive Oxides (TCOs) have revolutionized commercial applications. P-type TCOs were reported almost 100 years later than n-type TCOs, with NiO

Table 1.3 Properties of n and p-type TCOs

Material	Band Gap (eV)	Transparency (%)	Carrier Conc. (cm^{-3})	Mobility (cm^2 V^{-1} s^{-1})	Ref.
n-type					
SnO_2	3.6	∼80	$< 10^{20}$	5–50	[11]
In_2O_3	3.5	∼80	$< 10^{21}$	10–50	[12]
ZnO	3.2	∼80	$< 10^{21}$	5–50	[13]
IGZO	3.5	∼85	$\sim 10^{19}$	∼80	[10]
p-type					
$SrCu_2O_2$: K	3.30	∼80	6.1×10^{17}	0.46	[14]
$CuGaO_2$	3.36	80	1.7×10^{18}	0.23	[15]
$CuCrO_2$	2.58	>80	1.2×10^{19}	0.25	[16]
$CuAlO_2$	3.75	∼80	4.4×10^{17}	< 1	[17]

being the first reported p-type TCO. Some of the n and p-type TCOs notable properties have been compared in Table 1.3.

1.1.3 TFT Overview

The invention of the transistor can be attributed to three scientists at Bell Laboratories: John Bardeen, Walter Brattain, and William Shockley [18]. In 1947, they developed the first working transistor, known as the point-contact transistor.

Later advancements led to the development of the bipolar junction transistor (BJT) and the field-effect transistor (FET). The BJT is characterized by its two pn-junctions, and it operates by controlling the current flowing between the emitter and collector terminals through the base terminal. The FET, on the other hand, utilizes an electric field to control the conductivity of a channel and is commonly categorized into two types: the junction field-effect transistor (JFET) and the metal-oxide-semiconductor field-effect transistor (MOSFET).

TFTs belong to the field effect transistor (FET) family, differing from FETs in terms of active and passive substrates. While FETs utilize silicon wafers as active elements, TFTs leverage glass and plastic substrates that play no active role in the device. With three terminals - source (S), drain (D), and gate (G) - TFTs primarily serve as electronic switches. The control of carrier flow between the drain and source is achieved by altering voltages between the gate and source through the field effect phenomenon. Source and drain electrodes are deposited on the substrate/semiconductor using techniques like lift-off photolithography or shadow masking. The separation between the D and S electrodes defines the channel length (L), while the overlapping distance of the electrodes determines the channel width (W).

In 1962, the first TFT was successfully developed by Weimer at RCA Labs in cadmium sulfide (CdS) [19]. Two years later, the first oxide TFTs using SnO_2 were fabricated. The SnO_2 : Sb was the first transparent oxide TFT [20]. In 2003, ZnO TFT exhibited electron mobilities greater than $1\,cm^2\,V^{-1}\,s^{-1}$ [21]. That makes oxide TFTs a potential replacement for the *a*-Si employed in TFT display backplanes. As a consequence of further studies, the performance of transparent ZnO TFT improved, and it exhibited mobility of more than $2.5\,cm^2\,V^{-1}\,s^{-1}$ mobility. A breakthrough occurred in 2003 when Nomura [22] demonstrated an IGZO single-crystalline active layer, a TFT having an electron mobility of $80\,cm^2\,V^{-1}\,s^{-1}$ and an on/off ratio of 10^6 [22]. This high-performance TFT justified the use of MOs and demonstrated their potential [23].

Device structure of the TFTs

TFT consists of electrodes, active channels, and dielectric layers. All the thin film layers are developed on the substrates. A semiconducting active layer is placed between S and D metallic electrodes, whereas a dielectric layer is in between the active layer and G electrode. TFTs are classified as staggered and coplanar structures on the base of the position of S-D electrodes w.r.t semiconductor-dielectric interface. In a staggered structure, the source-drain electrodes are opposite to the semiconductor-dielectric interface, whereas in coplanar, they are on the same side of the interface. Based on the position of S and D electrodes to the channel layer, TFTs can be categorized as TGBC, TGTC, BGBC, and BGTC configurations as shown in Fig.1.4. The structural architectures are chosen based on deposition conditions and application. If the deposition temperature of the semiconductor is high, then the top gate is preferable, and vice versa.

Operating principle

The operating principle of TFTs parallels that of traditional MESFETs, where the gate terminal governs the current flow through the active channel region. The device is biased by applying two voltages: V_{gs} between gate and source, and V_{ds} between drain and source. These voltages control the channel current between the drain and source by varying the height of the gate-depletion region and the longitudinal electric field.

Three cases can be recognized for the I_{ds}-V_{ds} characteristic curve of the TFT, if V_{gs} is larger than the threshold voltage:

1. Low V_{ds} voltage where I_{ds} is linearly proportional to V_{ds}.

2. High V_{ds} where the current is almost constant.

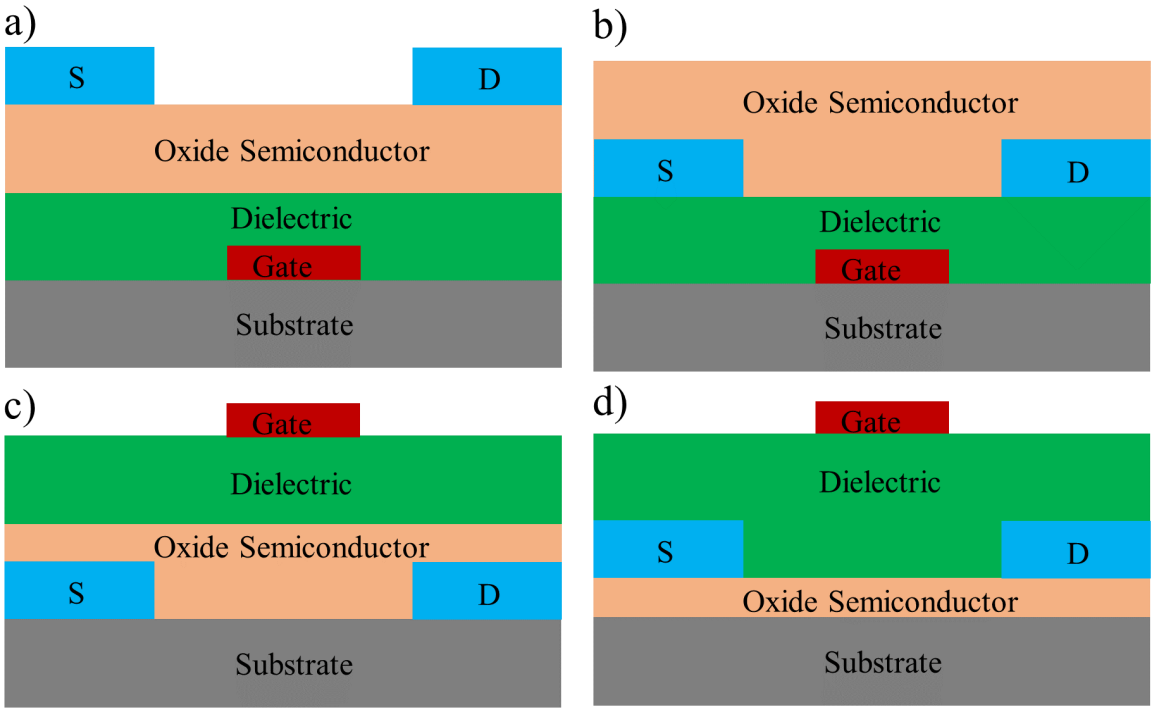

Fig. 1.4 TFT device structure: (a) BGTC, (b) BGBC, (c) TGBC, and (d) TGTC

3. Moderate V_{ds} where I_{ds} has a nonlinear relationship with V_{ds}.

Figure 1.5(a) illustrates the progression of drain current with an increasingly negative drain-source voltage, with each curve obtained at a constant negative gate-source voltage. This method of measurement is recognized as "output characteristics."

Initially, when $V_{gs} = 0$ and V_{ds} is raised from zero to a low value as shown in Fig.1.5(b), a longitudinal electric field and current are established in the channel. However, due to the wide space charge region, there will be no carrier modulation between the source and drain terminals, resulting in full depletion.

When V_{ds} exceeds the threshold voltage, the depletion region shrinks, forming a channel layer for carrier transportation as shown in Fig.1.5(c). Furthermore, due to V_{ds}, the voltage across the depletion region is greater at the drain end than at the source end, causing the depletion region to become wider at the drain end. The narrowing of the channel and the increased V_{ds} increase the electric field near the drain, causing the electrons to move faster. When V_{ds} is low, the current is approximately proportional to V_{ds}. In this regime, where both V_{gs} and V_{ds} strongly affect the drain current, the TFT is said to be in its linear region.

As V_{ds} is raised further, the channel current increases, the depletion region deepens at the drain end, and the conductive channel narrows, leading to pinch-off as shown in Fig.1.5(d). The current must be constant throughout the channel. As the conductive channel near the

drain narrows, the electrons must move faster. However, the electron velocity cannot exceed a limit called the saturated drift velocity.

When V_{ds} is increased beyond the value that causes velocity saturation, the hole concentration rather than velocity must increase to maintain current continuity. Accordingly, a region of hole accumulation forms near the end of the drain, and a depletion region is formed. This region is called a charge domain. Eventually, a point is reached where further increases in V_{ds} are dropped entirely across the charge domain, and the drain current does not substantially increase, as shown in Fig.1.5(e). At this point, the carrier moves at saturated drift velocity.

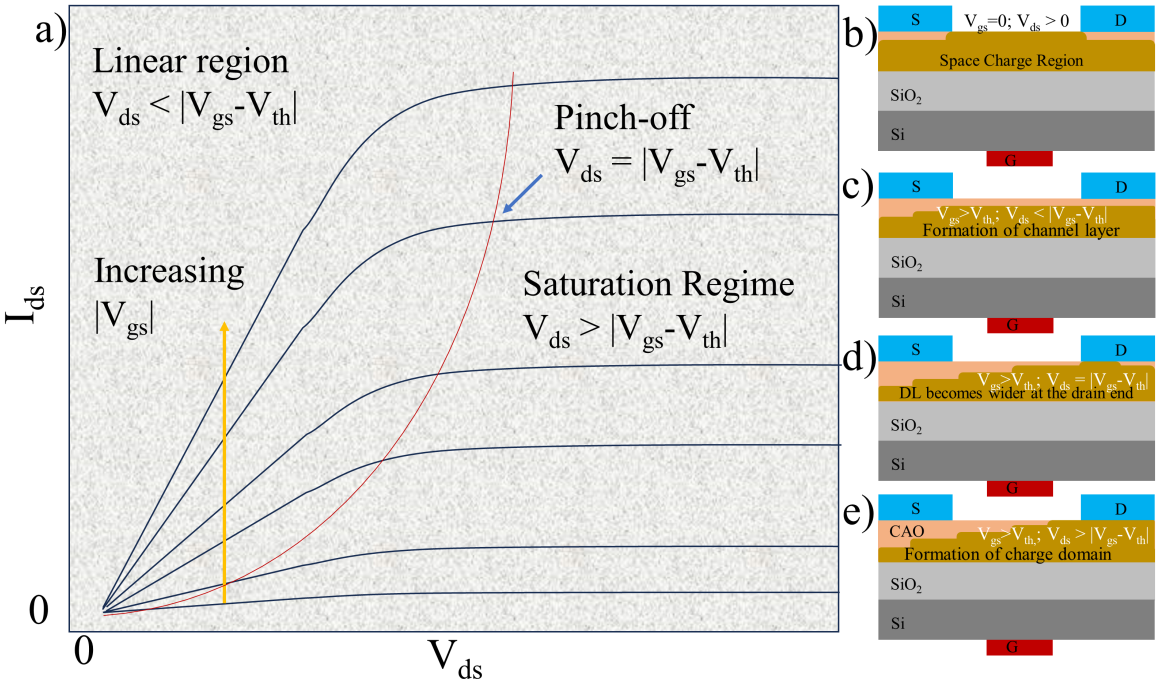

Fig. 1.5 TFT output and transfer characteristics

Advancements in TFT Technology: Materials, Processes, and Scalability

1. Channel Material for the TFT

The "channel material" in the context of a TFT refers to the semiconductor material used as the active channel through which charge carriers (electrons or holes) flow to control the current in the transistor. The channel material, either n-type or p-type semiconductor, is typically a thin film deposited on the substrate and is essential in achieving efficient and reliable operation of TFT-based electronic devices.

In an n-channel TFT, the active channel region is made of a material with excess negatively charged carriers known as electrons. The flow of electrons through this channel is controlled by the electric field generated by the gate voltage. By applying a positive voltage to the gate electrode, the electric field attracts the electrons. It allows them to move through the channel, resulting in a conductive path between the source and drain terminals of the transistor. In this configuration, the n-channel TFT operates as an enhancement mode transistor, where the application of a gate voltage enhances the current flow through the channel. Some important n-type channel materials for TFT transistors include IGZO, ZnO, In_2O_3, etc [24].

On the other hand, in a p-channel TFT, the active channel region is made of a material with an excess of positively charged carriers, known as holes. The flow of holes through this channel is controlled by the electric field generated by the gate voltage. By applying a negative voltage to the gate electrode, the electric field attracts the holes. It allows them to move through the channel, creating a conductive path between the source and drain terminals of the transistor. Some important p-type channel materials for TFT transistors include Cu_2SnS_3, $CuAlO_2$, CuO, Sn-doped Ga_2O_3, etc [25], [26].

2. Dielectric Materials in TFT

The gate dielectric material of a TFT is typically an insulating material that separates the gate electrode from the semiconductor channel. It acts as the gate insulation layer, providing electrical isolation between the gate electrode and the semiconductor layer. This isolation prevents leakage of current, ensuring proper transistor operation [27]. Common materials used as gate dielectrics in TFT transistors include SiO_2, HfO_2, Y_2O_3 etc. The choice of gate dielectric material can significantly influence the performance characteristics of the TFT, including threshold voltage, carrier mobility, and operational stability.

3. Low temperature <400°C processing

Keeping the fabrication process at a low temperature is crucial for compatibility with flexible substrates and sensitive materials [28]. High temperatures can degrade or damage these substrates and materials, limiting the flexibility and functionality of the TFTs. Low-temperature fabrication techniques also enable integration with other components or layers that may have temperature restrictions [29].

4. Large area

TFTs often need to be fabricated over large areas, especially in applications like displays and sensors where a high-resolution and sizable viewing area is required [30]. Fabrication

techniques should be scalable to accommodate the production of TFT arrays with thousands to millions of individual transistors while maintaining uniformity and performance across the entire area [29].

5. Simple process

A simple fabrication process is essential for the cost-effective manufacturing and scalability of TFT-based devices [31]. Complex processes increase production costs and reduce yield rates, making mass production challenging [29, 31]. Therefore, employing simple and reproducible fabrication methods reduces manufacturing time and costs while improving overall device reliability and performance.

CAO p-TFT fabrication and their reported results

Shuang Li [26] prepares thin $CuAlO_2$ films under spin coating using copper nitrate trihydrate and aluminum nitrate nonahydrate as starting materials. The films are annealed at various temperatures. The study systematically investigates the effect of post-annealing temperature on the microstructure, chemical compositions, morphology, and optical properties of the thin films. The annealing temperature influences the phase conversion from a mixture of $CuAl_2O_4$ and CuO to nanocrystalline $CuAlO_2$ as shown in Fig.1.6(a).

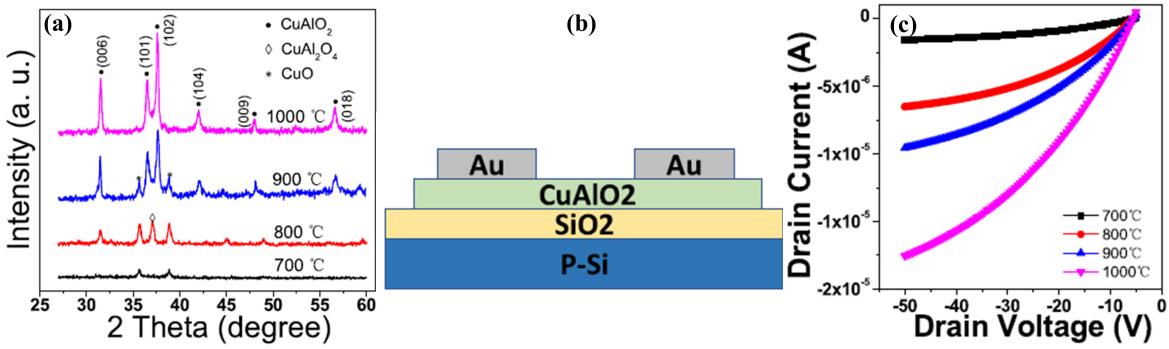

Fig. 1.6 a) XRD patterns of the $CuAlO_2$ thin films b) Schematic diagram of the $CuAlO_2$ TFTs c) Summarized output curves annealed at different temperatures [26].

Bottom-gate p-type TFTs with $CuAlO_2$ channel layers are fabricated on SiO_2/Si substrates as shown in Fig.1.6(b). The output curves are shown in Fig.1.6(c). The TFT performance is found to be strongly dependent on the physical properties and chemical. The optimized nanocrystalline $CuAlO_2$ TFT properties are mentioned in Table 1.4. Their work represents a significant step towards the development of low-cost CMOS logic circuits.

Chunfeng Wang et al.[32] explore the fabrication and integration of ternary p-type $CuAlO_2$ semiconductor thin films using the sol–gel method and annealing at various temperatures to optimize their properties. The annealing temperature significantly influences the phase conversion of the films, resulting in the formation of nanocrystalline $CuAlO_2$. X-ray diffraction (XRD) patterns reveal the evolution of crystalline phases. The optical transmittance of the $CuAl_xO_y$ thin films increases with higher annealing temperatures. The band gap energy of the $CuAlO_2$ thin films is determined, showing values beneficial for transparent electronics. These films are further incorporated as channel layers in thin-film transistors

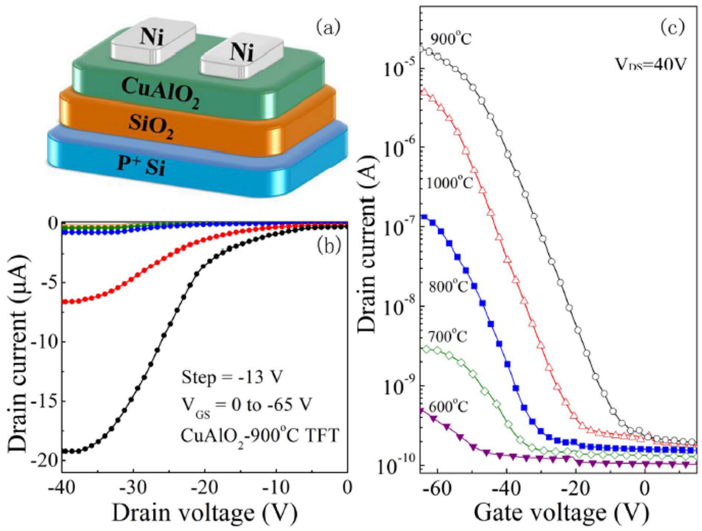

Fig. 1.7 a) Schematic of the TFT structure, b) Output curves of $CuAlO_2$ TFTs annealed at 900 °C, and c) Transfer characteristics of $CuAl_xO_y$ TFTs annealed at various T_a. [32].

(TFTs). Bottom-gate p-type TFTs with $CuAlO_2$ channel layers are fabricated and characterized as shown in Fig.1.7. The electrical performance of the optimized nanocrystalline $CuAlO_2$ TFT is mentioned in Table 1.4.

Yao[33] deposited $CuAlO_2$ films using magnetron sputtering with variations in working pressure and oxygen content. XRD patterns and X-ray photoelectron spectroscopy (XPS) were employed to characterize the films as shown in Fig.1.8(a-b). The electronic structure was modified by alloying nonisovalent Cu-O with the $CuAlO_2$ host. Through the incorporation of Cu-O dimers into the $CuAlO_2$ lattice, the study achieves a synergistic effect, leading to the delocalization of $Cu^{2+}3d^9$ orbitals and improved p-type conduction. The films demonstrated tunable wide direct bandgaps ranging from approximately 3.46 eV to 3.87 eV. Hall measurements confirmed the highest hole mobilities reported for $CuAlO_2$ films, ranging from 11.3 to 39.5 cm²/Vs.

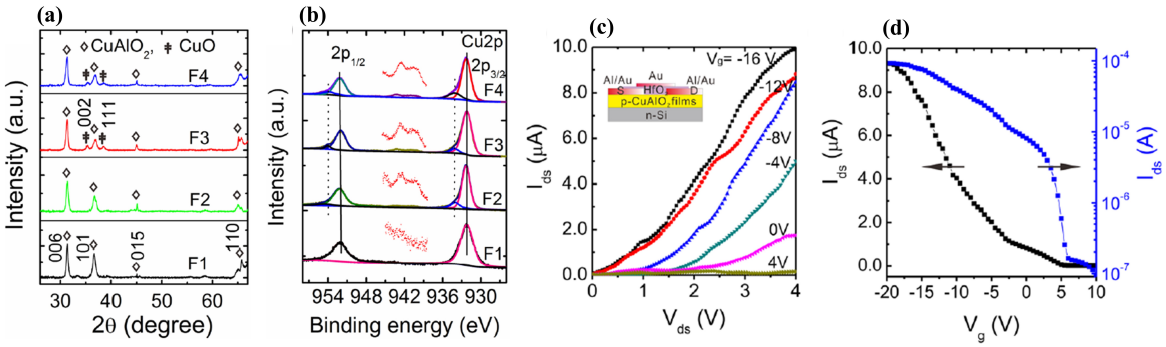

Fig. 1.8 (a) XRD patterns, (b) XPS spectra, (c) V_g-dependent I_{ds}-V_{ds} characteristics, (d) I_{ds}-V_g plots at $V_{ds} = 3$ V, and the inset in (c) depicts the schematic device structure of the $CuAlO_2 - based TFTs$[33].

Top-gate thin film transistors (TFTs) constructed on p-$CuAlO_2$ films, as shown in Fig.1.8(c-d) that exhibited pronounced performance, as tabularized in the Table 1.4. The findings suggest a promising strategy for advancing transparent electronic and optoelectronic devices.

Table 1.4 Summarized properties of the reported CAO p-TFTs

Method	Phase	Type	Sub.	Tdep (°C)	Tpda (°C)	Vth	μFE ($cm^2/V/s$)	Ion/Ioff	T (%)	Eopt (eV)	Year	Ref
RFMS	$CuAlO_2$:CuO	TFT	SiO_2/n-Si	940		-5	0.97	8×10^2		3.46	2012	[33]
solgel	Cu_2O, $CuAlO_2$	TFT	SiO_2/p-Si	350	1000	-1.3±0.5	0.098±0.009	10^3	80	3.8	2018	[26]
solgel	$CuAlO_2$	TFT	SiO_2/p-Si	400	900	-34.65±4.5	0.33±0.05	10^5	80	3.68	2019	[32]

1.2 Motivation and Objectives

1.2.1 Motivation

Wide-bandgap ($>$ 3 eV) metal oxides exhibiting high mobility and reliable optical transparency above 80% address the growing demand for large-area electronic and optoelectronic device applications. However, in commercial usage, n-type metal oxides are more prevalent than p-type counterparts[34].

A notable advancement in n-type metal oxides (MOs) was accomplished by Nomura et al. in 2003, with their demonstration of a thin-film transistor (TFT) incorporating an indium gallium zinc oxide (IGZO) single-crystalline active layer. This TFT exhibited an electron mobility of 80 $cm^2V^{-1}s^{-1}$ and an on/off current ratio of 10^6 [10, 35]. However, the challenge of fabricating high-performance devices at lower processing temperatures was first addressed in 2004 with the introduction of an amorphous oxide semiconductor TFT

utilizing amorphous In-Ga-Zn-O (a-IGZO) [36]. Nomura et al. [37] deposited a-IGZO at room temperature, exhibiting field effect mobility in the saturation region of 8.3 $cm^2V^{-1}s^{-1}$ and in the linear region of 5.6 $cm^2V^{-1}s^{-1}$[37]. In industrial applications, a-IGZO TFT devices are desirable. As, the a-IGZO films can be deposited using various techniques such as sputtering, ALD, or CVD which offer greater flexibility in manufacturing processes, allowing for the fabrication of TFTs on diverse substrates, including flexible or large-area surfaces for the flexible electronics [38]. Additionally, amorphous IGZO can be processed at lower temperatures compared to its crystalline counterpart. This lower processing temperature is beneficial for compatibility with temperature-sensitive substrates or for reducing thermal stress on the device during fabrication. In such a way, practical IGZO devices often utilize the amorphous phase due to their superior uniformity, manufacturing flexibility, stability, and transparency, which are critical for real-world applications [39]. Hence, the high-performance n-type TFT justified its potential application in electronic devices. On the other hand, the quest for p-type MOs TFTs having comparable performance to n-type counterparts continues to face formidable challenges [40].

The availability of equally efficient p-type Transparent oxide semiconductors (TOS) could revolutionize the fabrication of transparent devices and circuits, enhancing energy efficiency and enabling greater complexity. The development of p-type TOS with robust performance could serve as a pivotal enabler for various applications requiring transparency, power efficiency, and advanced circuitry. For instance, the realization of a transparent Complementary Metal Oxide Semiconductor (CMOS) device with commendable performance could facilitate the fabrication of circuits parallel to those in silicon technology, promising a new era of transparent electronic gadgets poised to impact numerous aspects of daily life [41]. CMOS circuits offer several advantages over unipolar transistors, including low power consumption, minimal waste-heat generation, high noise margin, robust logic swing output, dense circuit integration, and architectural simplicity [17]. Moreover, p-n junctions serve as fundamental components enabling diverse semiconductor functionalities such as current rectification. These applications encompass transparent electronics, displays, sensors, photovoltaics, memristors, and electrochromics. For instance, the utilization of high-performance TOS could lead to transparent displays boasting higher pixel density (resolution) and enhanced refresh frequencies.

The obstacle in achieving p-type TOS with performance comparable to their n-type counterparts stems from the unique electronic configuration inherent in oxide materials. In n-type oxides, oxygen vacancies generate a sufficient supply of electrons, forming the primary electron-transport pathway in the conduction-band minimum (CBM) mainly through metal *s* orbitals. These orbitals, characterized by spatial dispersion, facilitate significant hybridization

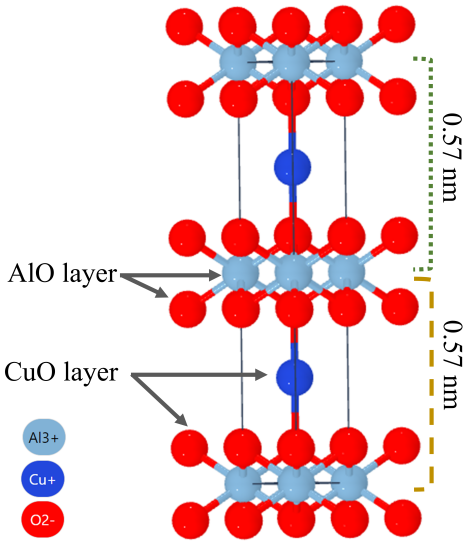

Fig. 1.9 The hexagonal crystalline structure of $CuAlO_2$ was calculated in the Materials Project[43].

even in amorphous structures by incorporating heavy-metal cations. Consequently, the highly dispersed and delocalized CBM fosters a low electron-effective mass, resulting in high mobility [37]. Conversely, the generation of positive carriers (holes) in p-type oxides encounters constraints due to the high formation energy of native acceptors (e.g., cation vacancies) and the low formation energy of native donors (e.g., anion vacancies) that neutralize holes [42]. Even in the presence of a certain hole concentration, the transport pathway for holes, situated at the valence-band maximum (VBM), primarily consists of anisotropic and localized oxygen 2*p* orbitals, leading to a large hole-effective mass and low mobility. Kawazoe et al.[6] realized that modifying the energy band structure would alleviate such localization behavior. In this regard, the Cu^+ cation is an intriguing choice due to the highest energy for the d^{10} closed shell electrons, which is expected to overlap with the 2p electrons of oxide ions. The tetrahedral coordination of oxide ions mitigates the localization behavior of 2p electrons. However, the direct interaction between d^{10} electrons of neighboring Cu^+ ions reduces the bandgap. CAO has been identified as a potential candidate due to its ability to reduce the dimension of Cu^+ ions, leading to a consequent enlargement of the bandgap [6].

The current research has chosen CAO due to its p-type nature and potential application as a transparent conductive oxide (TCO) material[44]. CAO is composed of AlO_6 octahedra spread out, forming a basal layer and alternating stacking layers of O-Cu-O dumbbells structure vertically [45] as shown in Fig. 1.9.

Along with poor film quality, the deficiency of Cu-O-Cu lattice connectivity[26] in the CAO structure is also accountable for the low field effect mobility. Addressing such issues requires a layer-by-layer (LBL) deposition approach that enables the c-direction stacking of CuO and AlO, focusing on the d-spacing of CAO. Recently, digitally processed DC sputtering (DPDS) has been proposed as an atomically precise deposition method [46, 47]. This research comprises two main objectives, as shown in Fig.1.10.

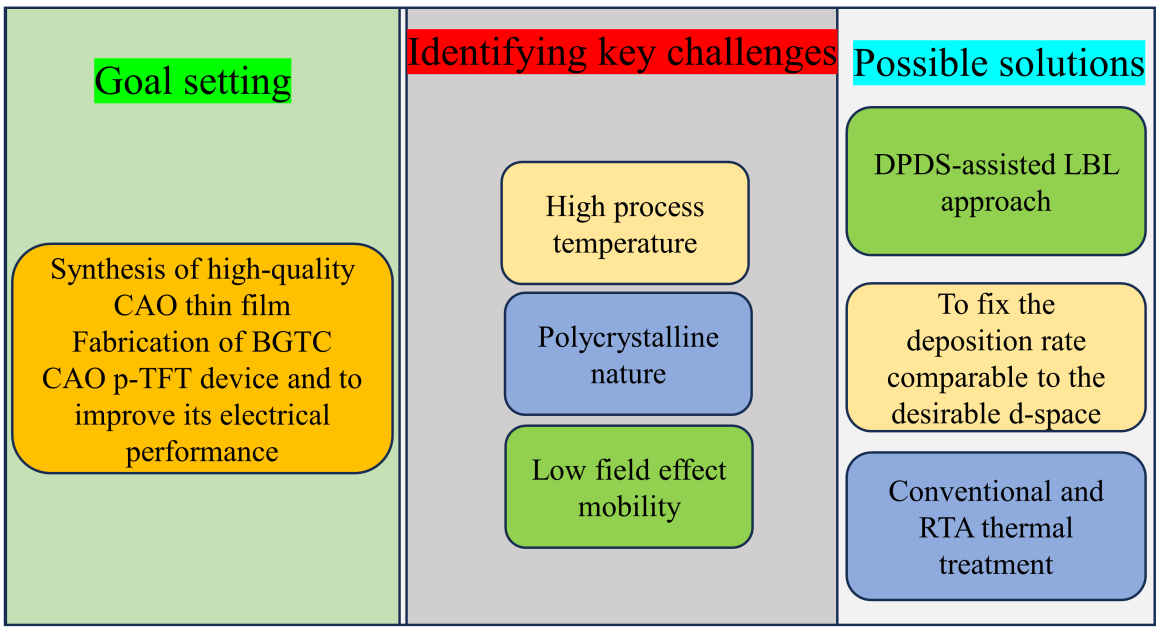

Fig. 1.10 Thesis objective and overview

1.2.2 Objective-I

The 1st main objective is the layer-by-layer deposition of $CuAlO_2$ thin film by Digitally Processed DC Sputtering technique (DPDS). This study utilized the DPDS-conducted LBL approach for CAO thin film growth for the first time. The LBL approach enables precise control of the growth process, leading to ordered CuO, AlO stacking, and formation of long-range structural integrity, which is believed to facilitate carrier transport increase. There is no scattering, and it contributes to the improvement of mobility. Moreover, the LBL deposition facilitates better control over the growth process, which minimizes the formation of grain boundaries in CAO and also contributes to higher mobility. The DPDS allows the deposition rate to be 0.57 nm/cycle under the d-spacing of the (002) plane for good CAO crystallinity. In the growth of CAO by DPDS-assisted LBL, non-radical oxidation was prioritized to avoid possible surface damage [47].

Moreover, transparent amorphous semiconductors (TAS), fabricated at low temperatures, are pivotal materials for practical applications in transparent flexible electronics. However, current transparent amorphous oxide semiconductors (TAOS) are predominantly restricted to n-type conductivity. Although several crystalline p-type TOS such as $CuAlO_2$ and SnO have been identified, their amorphous thin films lack p-type conduction characteristics. Orderly stacking by DPDS facilitates carrier transport without scattering even in its amorphous nature.

1.2.3 Objective-II

A p-TFT with comparable performance as to n-type is demanding in CMOS technology, both p-type and n-type transistors are necessary to form logic gates and other electronic components. P-type TFTs are responsible for implementing the complementary logic functions alongside n-type TFTs. Without p-type conductivity, it would be impossible to fabricate CMOS circuits, which are fundamental to modern integrated circuit design. Moreover, high-performance p-type material is essential for the p-n junction to make good current rectifiers.

In p-TFT, p-type conductivity and field-effect mobility are fundamental parameters that need to be improved. High field-effect mobility is desirable in TFTs because it directly influences the switching speed and overall performance of the transistor. Faster mobility allows for quicker response times and improved efficiency in electronic devices such as displays, sensors, and integrated circuits. The field-effect mobility is typically lower than the Hall mobility in semiconductor materials [48]. This is primarily because the Hall mobility measures the mobility of charge carriers in the bulk of the material, unaffected by external electric fields. In contrast, field-effect mobility considers the mobility of charge carriers under the influence of an electric field generated by an external gate voltage in a transistor structure [29]. To improve FE mobility, it's essential to enhance the crystalline quality of the semiconductor material, reduce defects and impurities, optimize the device structure, and minimize scattering mechanisms that hinder the movement of charge carriers.

In TFTs, high carrier concentration, good conductivity, and high transparency are also essential, especially in applications such as display technology [41][17]. A high carrier concentration ensures sufficient charge carriers are available for conducting current, which is vital for achieving fast response times and efficient operation. High conductivity allows for reduced power consumption and improved signal integrity in electronic devices. Where, transparency is a critical requirement for certain applications of TFTs, particularly in transparent display technologies like OLED and LCD [41].

The 2nd main objective is to fabricate both amorphous and crystalline CAO p-type TFTs utilizing shadow masking techniques and enhance the field-effect mobility to surpass $1\,\mathrm{cm}^2/\mathrm{V}s$, aligning with the performance of previously reported amorphous n-type TFTs.

1.3 Summary of Chapter 1

The first chapter of the research work delves into the introduction, motivation, and objectives behind the selection of $CuAlO_2$, highlighting the aim to fabricate p-type transistors and addressing the need for improved performance parameters in thin film transistors (TFTs).

It begins by exploring the significance of metal oxides in optoelectronics, particularly emphasizing the role of transparent conducting oxides (TCOs) in various applications. The chapter elucidates the physics behind TCOs, discussing conductivity, electronic structure, and optical transparency, while distinguishing between n-type and p-type TCOs.

Detailed insights are provided into the device structure, operating principles, and key electrical parameters essential for evaluating TFT performance, including threshold voltage, carrier mobility, and current on/off ratio. Additionally, the chapter delineates the requisite performance criteria for TFTs, emphasizing the importance of p-type conductivity, high field effect mobility, and carrier concentration for achieving enhanced device performance. Moreover, the need to improve field effect mobility relative to Hall mobility is identified as a critical point for advancement.

Chapter 2

Experimental methodology

This chapter outlines the comprehensive experimental framework employed in the study, beginning with a detailed exploration of various techniques used in sample processing and characterization. A focus is then placed on sputtering, including the specific needs of digitally processed DC sputtering (DPDS). Moreover, the motivation and objectives of this comprehensive experimental endeavor are elucidated.

2.1 Techniques used in the samples processing

Different techniques have been reported in the growth of thin films and bulk samples, as mentioned in FIg. 2.1. Solution-base, CVD, and PVD are leading techniques widely employed in thin film growth [49], while sol-gel is mostly used for bulk sample preparation. Brief reviews on all the techniques and detailed discussion are as follows.

2.1.1 Solution-base techniques

a) Sol-Gel

Sol get is an economical and easiest technique for the preparation of thin film, powder, xerogel, etc. This method is based on the phase conversion of hydrolyzing a mixture of precursors that passes sequentially through a solution state and a gel state before being dehydrated to a substrate, as shown in Fig. 2.2. The sol-gel technique is advantageous due to the usage of small amounts of precursors and in a coating of complex shapes [50].

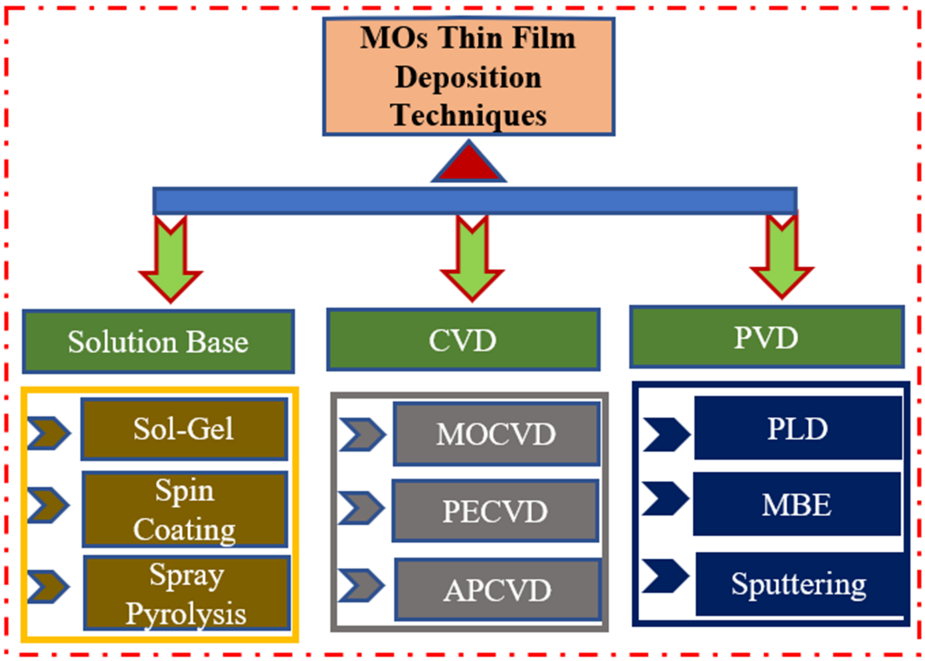

Fig. 2.1 MOs deposition techniques.

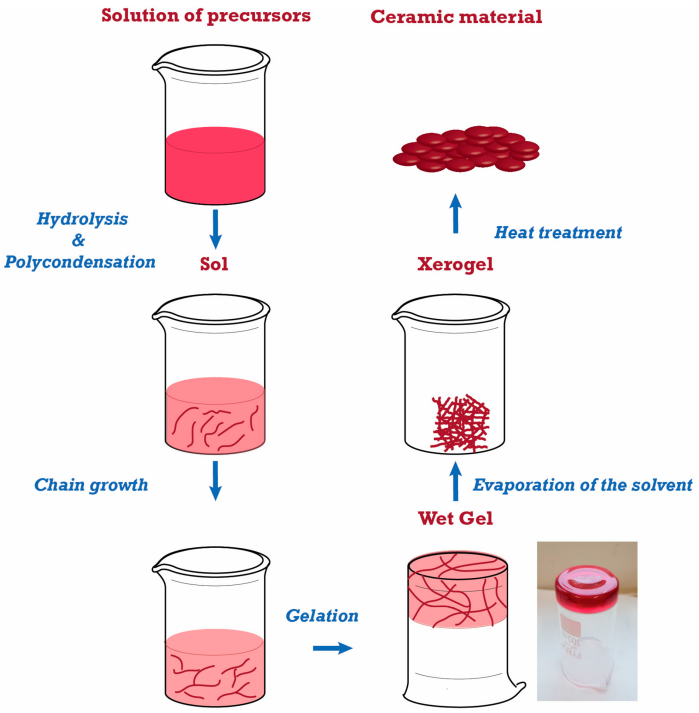

Fig. 2.2 Sol-gel Method [51].

b) Spin coating

The spin coating technique is employed for uniform thin films of thickness in micro/nanometre ranges. The spin coating technique is based on the spreading of Newtonian fluid on a circular substrate with constant angular velocity and thin film formation as in Fig. 2.3. The key stages that spin coating undergo are deposition, spin-up, spin-down, and evaporation of solvents [52].

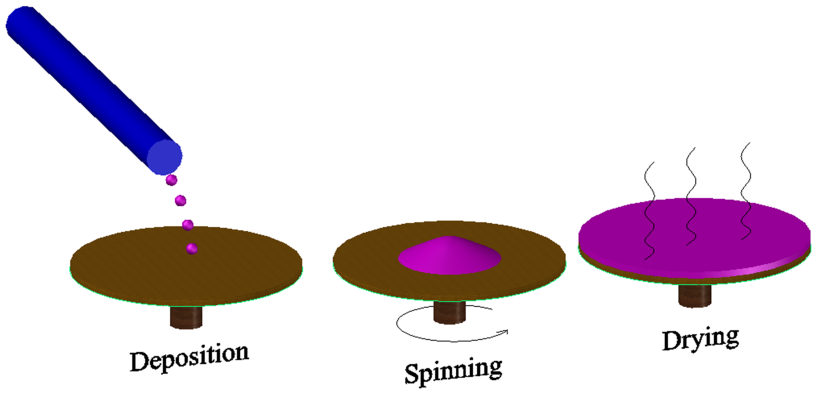

Fig. 2.3 Spin Coating.

c) Spray pyrolysis

It is a relatively cost-effective and versatile method for the growth of thin and thick films of metal oxide, ceramic coatings, and powder production [53]. In spray pyrolysis, a disk-like thin film is formed when the metallic solutions are sprayed onto a heated surface as in Fig. 2.4. Then, the solution's components are sprayed after a reaction with a chemical compound. The three essential components are precursor solution atomization, aerosol transportation, and decomposition of precursors on the substrate. The quality of the film depends mainly on the substrate surface temperature. At higher temperatures, the grown film becomes porous and has a rough texture; at low temperatures, it cracks, so determining the substrate temperature is more critical [54].

2.1.2 Chemical vapor deposition (CVD)

CVD is a common deposition technique where a sample is deposited by chemically reacting volatile compounds with other gasses, producing a non-volatile solid and depicting it atomistically on a substrate [55]. The CVD process is shown in Fig. 2.5. CVD is desirable to grow film at lower substrate temperature.

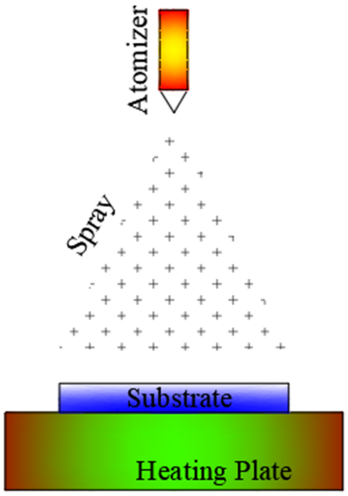

Fig. 2.4 Spray pyrolysis.

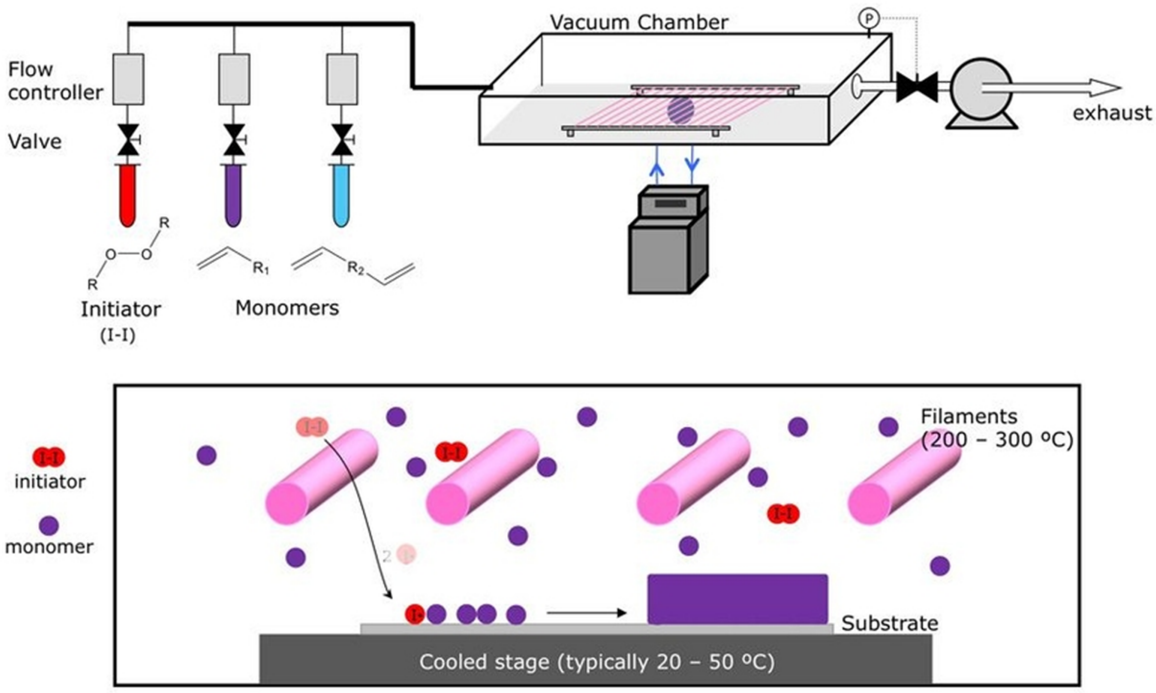

Fig. 2.5 Schematic of the CVD process: where an initiator material (red) and one or more monomers (purple and blue) are used for the desired polymer coating. These are vaporized and then introduced into a vacuum chamber containing the material to be coated (source: MIT News Office).

a) Metalorganic chemical vapour deposition (MOCVD)

MOCVD, known as metalorganic vapor-phase epitaxy (MOVPE), is a vapor-phase epitaxial growth technique for organometallic precursors. Today, this technique is widely used commercially due to low manufacturing cost and mass production for a wide range of devices [56].

b) Plasma-assisted chemical vapour deposition (PACVD)

PACVD is widely used in microelectronics to deposit nitride and metallic oxide compounds. PACVD is a modified conventional CVD system where electric power is supplied to the reactor, and plasma is generated. DC power supply for conducting and RF (13.56 MHz) is applied for non-conducting targets. The biasing voltage of more than 50V is applied to induce ion bombardment. When the arriving ions collide with the target, it transfer momentum; as a result, neutral species eject from the surface and are then collected on a suitable substrate [57].

c) Atmospheric pressure chemical vapor deposition (APCVD)

APCVD is a chemical synthesis process at atmospheric pressure where the substrate is exposed to the gas-phase precursors at controlled reaction conditions [58]. In APCVD, the reaction chamber's pressure is very close to atmospheric pressure. Low melting or volatile precursors are used, which can be easily transported to the reaction area by the carrier gas. Such a technique undergoes eight stages: mass transportation of the reactant, the reaction of precursors, diffusion of gas molecules, adsorption of the precursor, dispersion of precursor into a substrate, surface reaction, desorption of the product, and the removal of by-product [59]. Homogeneous reactions occur in the vapor phase, while heterogeneous reactions occur at the vapor solid surface interface inside the reaction chamber [60]. It has high deposition rates of several micrometers of film on wafers or other substrates.

2.1.3 Physical vapor deposition (PVD)

a) Pulsed laser deposition (PLD)

Singh and Narayan proposed the PLD deposition technique for the first time, which is extensively used in the deposition of alloys and/or compounds [61]. A powerful ultraviolet pulsed laser ($1\,J/cm^2$) is irradiating through a quartz window (quartz window intensifies the energy density) on the target. The evaporated atoms/particles from the surface of the targets are collected while placing the substrate and forming a thin film. The weightage of PLD is

due to its simple design, and the target may be used in powder, single crystal, and sintered pellets. The sputtering rate depends on the optical absorption depth (L_0) of the UV laser and the thermal diffusion depth (L_t) of the target source. Wide band gap semiconductors and insulators possess small L_t values and cause weak absorption. In contrast, narrow bandgap semiconductors and metals with strong absorption melt the target material and thermally evaporate it.

b) Molecular beam epitaxy (MBE)

MBE is the most reliable deposition technique for the controlled deposition of alloys and compounds. In device physics, MBE brought revolution due to the use of superlattice structures [62]. A computerized process control unit controls the target source in situ. MBE is used for producing high-quality epitaxial (atomic layer) thin film. The film thickness, composition, and morphology are precisely controlled in MBE deposition. In the effusion cell of MBE, the target material is heated and the vapor can move toward a substrate. The vapor can condense at the substrate, forming an epitaxial, thin, and highly pure thin film [63].

c) Sputtering

Sputtering is a physical vapor deposition (PVD) technique in which energetic particles, often ions, are directed at a solid target material within a vacuum environment. The impact of these high-energy particles on the target surface results in the ejection of atoms or ions. These ejected atoms or ions then deposit onto a nearby substrate, forming a thin film. The current work employs sputtering deposition in the growth of CAO thin film so we will discuss the sputtering process in detail.

2.2 Sputtering overview

2.2.1 Types of sputtering techniques

There are several sputtering techniques, including DC sputtering, RF sputtering, magnetron sputtering, and reactive sputtering, each offering unique advantages in thin film deposition processes. These methods employ different mechanisms to dislodge and deposit atoms or molecules onto a substrate, enabling precise control over film properties in various industrial applications.

I. RF sputtering

RF sputtering works in the same fashion as DC sputtering with different power sources. In RF sputtering, alternating high frequency (approximately 13.56 MHz) and large potential voltage is applied at the cathode. On the negative half cycle, ions are attracted toward the cathode, so a sputter occurs. However, electrons reach the surface and neutralize the accumulated charges on the positive half cycle. Under such a systematic approach, deposition of the insulator and the metallic targets is possible [64] [65]. It has a comparatively lower deposition rate compared to DC sputtering.

II. DC sputtering

The DC sputtering system consists of two planar electrodes. Metallic target materials are covered on the cathode, and substrates are placed on the anode. The Argon gas (as an ion source) is filled in the main chamber, and glow discharge (i.e., current flow) is maintained under the application of DC voltage between two electrodes. The charge accumulation limit DC is only applicable for depositing a conducting target [66].

III. DC reactive sputtering

In reactive sputtering, a reactive gas is introduced into the sputtering chamber in addition to inert gas during the deposition. With the addition of reactive gas, it is possible to form oxides, carbides, nitrides, etc. [67]. Reactive sputtering with a metal cathode has gained much attention from researchers due to controlled deposition and high deposition rate. The behavior of the sputtering process, including the deposition rate and composition of the film, will be significantly changed with the addition of sputtering gas. At a reactive gas supply that is too low, the deposited film's under-stoichiometric composition is due to a higher rate of metallic deposition. At a much higher supply of reactive gas, the stoichiometric can be maintained, but due to cathodic oxidation, the deposition rate falls significantly. The behavior point is desirable where the deposition and film stoichiometric may exist optimally.

At first sight, the reactive sputtering process may seem very simple by adding a reactive gas with the sputtered material, but the reaction mechanisms exhibit complex behavior. The operation of this system can be expressed by the deposition rate and the discharge voltage plotted as a function of the reactive gas flow rate, as shown in 2.6.

There is a constant inert gas of mTorr pressure in the chamber. The figure is categorized into three regions: metallic deposition, reactive deposition, and cathodic oxidation. In a metallic deposition, the cathode is sputtered with pure inert gas and a pure metallic-grown film. In the reactive deposition region, the reactive gas flow (f_r) is introduced and increases,

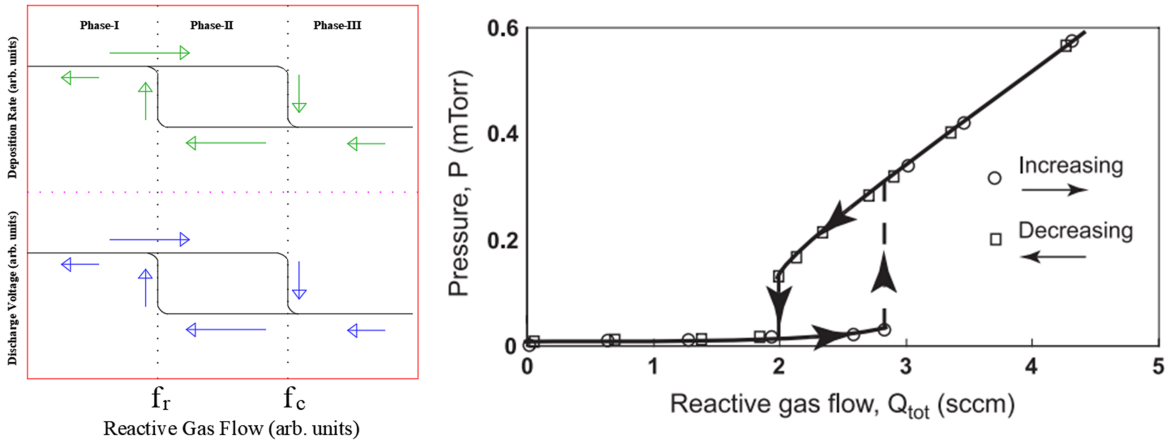

Fig. 2.6 DC Reactive Sputtering.

which is absorbed by the deposited films, and fully stoichiometric oxide is formed. After reaching the saturation point (critical flow point f_c), where the deposited film cannot absorb further reactive gas, the unused reactive gas starts to react with the cathode. It forms an oxidized layer, stopping the supply of metallic atoms toward the film. In a one-way transition, the conversion of metallic to reactive mode significantly discharges voltage changes and drops the deposition rate. After the transition, when the reactive gas is reduced, the system is not restored to the same flow due to a residual oxide layer on the target. It takes some time for the metallic mode to clear the oxide on the surface of the cathode. When a plot is drawn for a reactive system, it forms a hysteresis loop [68]. The hysteresis effect is also observed for the partial pressure with the reactive gas. The above figure illustrates the change with increasing and decreasing the gas supply. For increasing the supply of reactive gas, the partial pressure of the reactive gas varies from a low level to an upper limiting value. For the decreasing sequence of reactive gas, the partial pressure remains dominantly higher than the increasing sequence as more gases are consumed during the initial flow of reactive gas for compound formation [69]. Reactive sputtering exhibits hysteresis effects in response to different processing parameters. The general outcome behavior in the reactive sputtering process is commonly referred to as a renowned Berg's model [70] [71]. The hysteresis effect is one of the key problems associated with reactive sputtering.

Digitally processed DC sputtering (DPDS) is the central technique for the deposition of CAO. At Isshiki-Lab, sputtering is performed by DPDS using the p-RAS system.

2.3 Needs of digitally processed DC sputtering (DPDS)

PLD, ALD, and RS are suitable techniques for synthesizing metal oxide compounds. PLD is for small areas with low deposition rates, and droplet formation is undesirable. While in ALD, the choice of material is limited, and the deposition rate is also relatively low. The hysteresis behavior of the deposition rate of the Conventional RS tool makes it unsuitable for layer-by-layer deposition. Digital switching pulse DC sputtering is desirable to overcome the hysteresis problem with the idea of space-separation and surface reaction process. Programmable radical-assisted sputtering (p-RAS) precise deposition systems developed by Shincron Co., LTD are extensively used for ultra-thin metallic oxide compound growth with mass production. The p-RAS for DPDS is shown in Fig. 2.7.

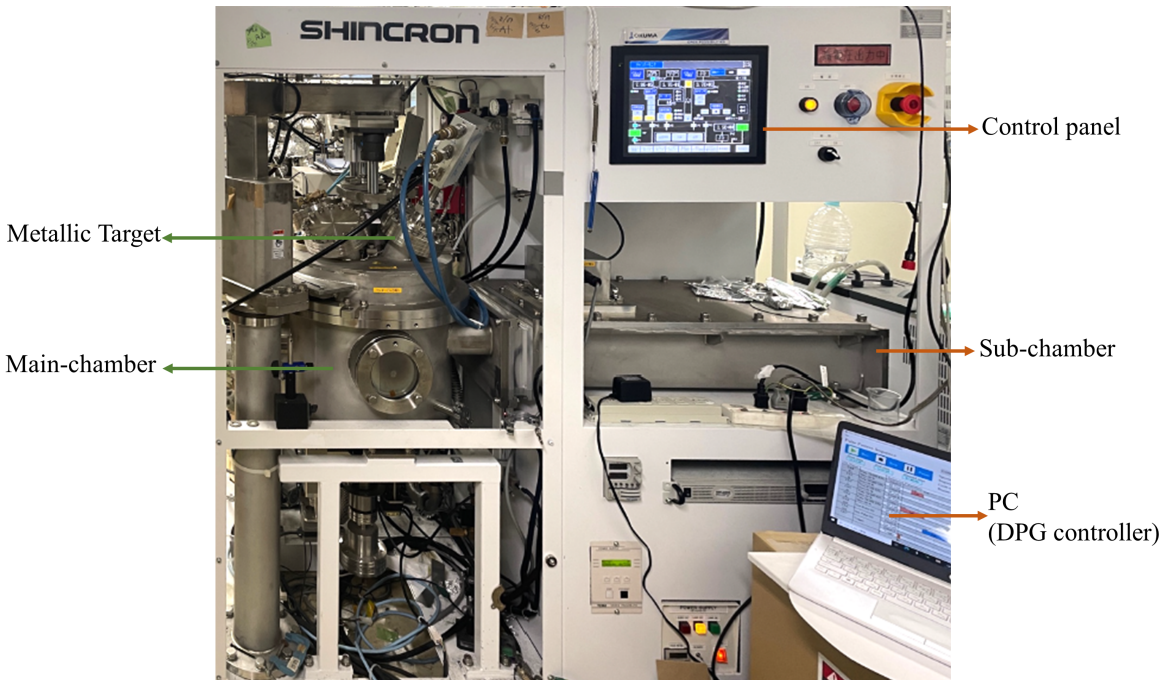

Fig. 2.7 DPDS setup in the Isshiki-lab UEC.

2.3.1 Working of DPDS

Digitally processed DC sputtering (DPDS) is based on the pulsed-DC sputtering technique. RAS allows time separation between desired metal sputtering and radical reaction. Pulsed DC sputtering in a sequential deposition is controlled via a digital pattern generator (DPG). The sample rate of DPG is 100 MS/s, and the high voltage switch (HV-SW) response time is 40 ns. The DC power supply generates pulsed-DC plasma on each cathode via the HV-SW under one of the three basic modes (i.e., cp, cv, and cc) controlled by DPG. Argon gas is

uninterrupted at a constant flow rate and introduced in the sputtering chamber as a sputter ion source. It follows metallic mode and then reactive mode. Under metallic mode, a certain metal sputter is performed. In reactive mode, reactive gas (i.e., oxygen gas) is fed into the main chamber driven by DPG. A vent-and-run approach is needed to stabilize the reactive gas supply in the reactive mode. Then, the chamber pressure is controlled automatically by an automatic pressure controller (APC). The schematic od DPDS setup located in Isshki-lab is shown in Fig. 2.8. In the reactive mode, the deposition rate significantly decreased. While switching the supply, the hysteresis behavior can be avoided.

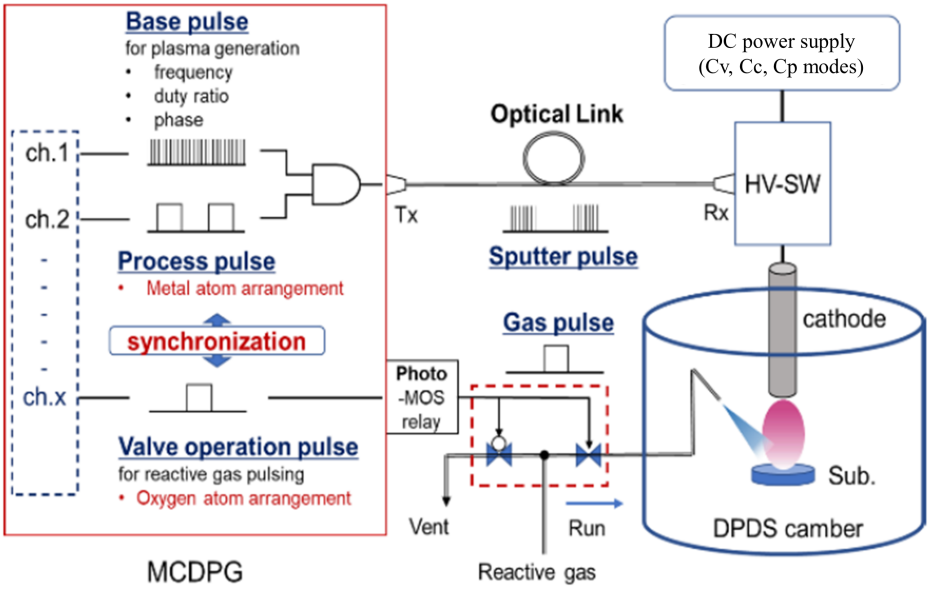

Fig. 2.8 Schematic of the DPDS process.

2.4 Heat treatment (Post-annealing)

Post-annealing is a critical technique in thin film engineering, enhancing microstructural integrity, reducing defects, and improving functional properties [72]. Through controlled thermal treatments, it optimizes crystal growth, reduces grain boundaries, and rectifies intrinsic defects. It enables tailored material composition, relieves residual stresses, and enhances thin film quality for electronics, optics, and energy conversion applications [73].

Furnace annealers are utilized for post-annealing thin film samples in scenarios requiring precise temperature control, thermal uniformity, scalability, controlled atmospheres, and longer annealing durations. These annealers are particularly beneficial for large-scale production, ensuring high throughput and uniform treatment of multiple samples. The controlled temperature profiles offered by furnace annealers enable accurate heat treatments, while

their superior thermal uniformity ensures consistent microstructural evolution across the samples. The furnace annealer is shown in Fig. 2.9. Additionally, introducing specific gases or oxidizing atmospheres facilitates desired chemical reactions, such as forming protective oxide layers. Furthermore, furnace annealers accommodate prolonged heat treatments when necessary, allowing for achieving desired transformations or diffusion processes in thin films.

Fig. 2.9 Furnace anneal-er.

2.5 Samples characterization

2.5.1 Field-emission scanning electron microscopy (FE-SEM)

FE-SEM is an imaging technique with exceptional resolution and surface characterization capabilities. In materials science and semiconductor research, FE-SEM allows for the characterization of thin film coatings, layers, and interfaces, contributing to developing advanced devices and materials. This cutting-edge microscopy method utilizes a finely focused electron beam to examine the topography and morphology of solid samples at the nanoscale.

FE-SEM is used for precisely determining cross-sectional dimensions in thin films, as shown in Fig. 2.10. A finely focused electron beam is directed onto the sample surface, allowing for detailed visualization of the film's profile. The high-brightness electron source employed in FE-SEM generates an electron beam with superior energy and brightness, enabling the observation of fine details and subtle variations in thickness.

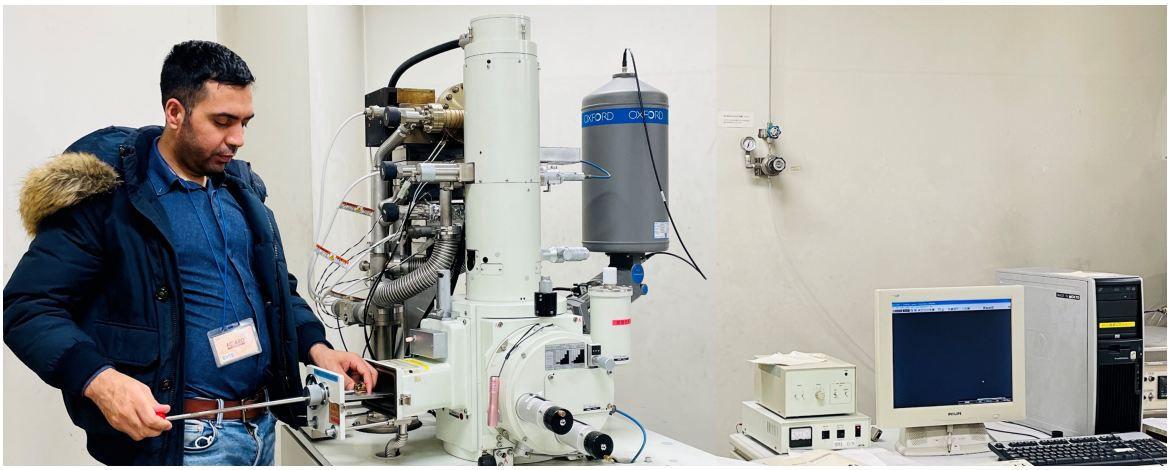

Fig. 2.10 Working on FESEM setup located in UEC.

2.5.2 Electron probe microanalyzer (EPMA)

The electron probe microanalyzer (EPMA) is an advanced scientific instrument that precisely characterizes and analyzes solid materials. Regarding sample characterization, EPMA offers flexibility and accommodates a wide range of specimen types, such as polished sections, thin films, or bulk materials. EPMA is also compatible with non-conductive specimens through specialized sample holders and coating techniques, ensuring accurate measurements even for insulating materials. A Schematic of EPMA and basic working principle is shown in Fig.2.11.

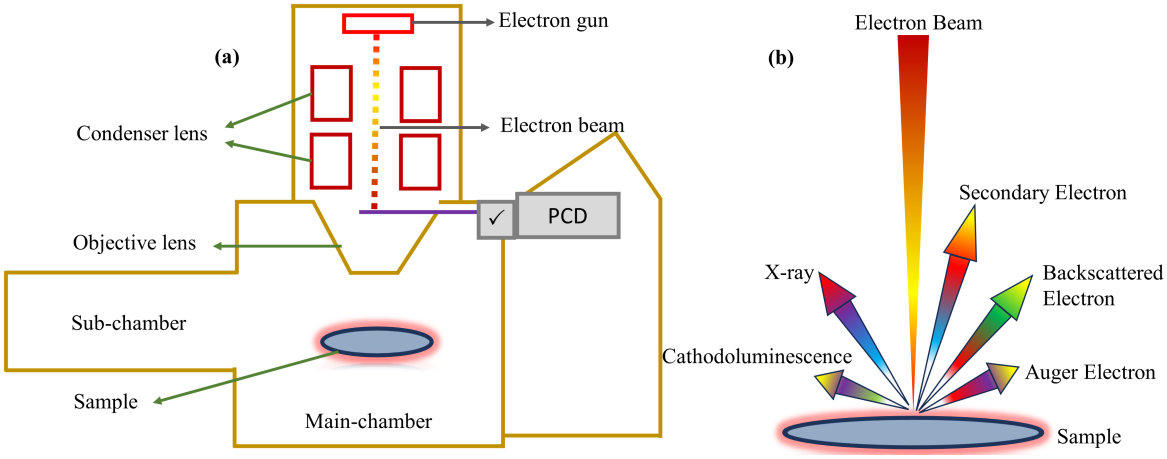

Fig. 2.11 a) Schematic of EPMA b) signals generated by electron irradiation.

At the heart of the EPMA lies an electron gun that generates a high-energy electron beam. This beam is focused onto the sample using electromagnetic lenses, producing a tiny spot size of a few micrometers. The incident electrons interact with the atoms in the sample,

leading to various physical phenomena. These interactions give rise to secondary signals, such as characteristic X-rays and backscattered electrons, vital for elemental analysis. By tightly focusing the electron beam, EPMA allows a detailed investigation of minute features and intricate microstructures. EPMA facilitates quantitative analysis, allowing researchers to measure elemental concentrations accurately. This capability is precious when determining elements accurately and is crucial for research interpretations.

EPMA possesses superior analytical sensitivity, enabling the detection of elements down to the parts-per-million level. EPMA also offers various analytical techniques to extract detailed information from a sample. Energy-dispersive X-ray spectroscopy (EDS) is commonly employed, where the characteristic X-rays emitted by the sample are collected and analyzed to determine the elemental composition. This data can be further utilized to generate elemental maps, illustrating the distribution of different elements across the sample surface. Additionally, wavelength-dispersive spectroscopy (WDS) can be utilized, providing enhanced spectral resolution and precise identification of elements and isotopes. Moreover, EPMA can have specialized detectors to extend its analytical capabilities. For instance, a cathodoluminescence (CL) detector can be integrated, enabling the characterization of luminescent properties in minerals and semiconductors. This facilitates the study of defect structures, crystal growth, and optical properties, opening new avenues for materials science and solid-state physics research.

2.5.3 X-ray diffraction (XRD)

X-ray diffraction (XRD) is a highly advanced analytical technique to characterize and analyze crystalline materials. This advanced method leverages the principles of wave-particle duality to probe the atomic structure and arrangement within a material. By directing X-rays toward a sample and measuring the resulting diffraction pattern, XRD enables researchers to unravel intricate details about crystallographic properties, phase composition, and lattice parameters.

The fundamental principle behind XRD lies in the interaction of X-rays with a material's crystal lattice. When monochromatic X-rays of a specific wavelength (λ) impinge upon a crystalline sample, they are diffracted by the crystal lattice planes. This diffraction occurs due to constructive interference between the X-ray waves scattered by the atoms in the crystal are determined by Fig. 2.12. Geometric considerations allow us to demonstrate that constructive interference occurs at specific angles, denoted as θ_B, depending on the interplanar spacing, d, as described by the Bragg Equation 2.1:

$$n\lambda = 2d_{hkl}\sin\theta_B \tag{2.1}$$

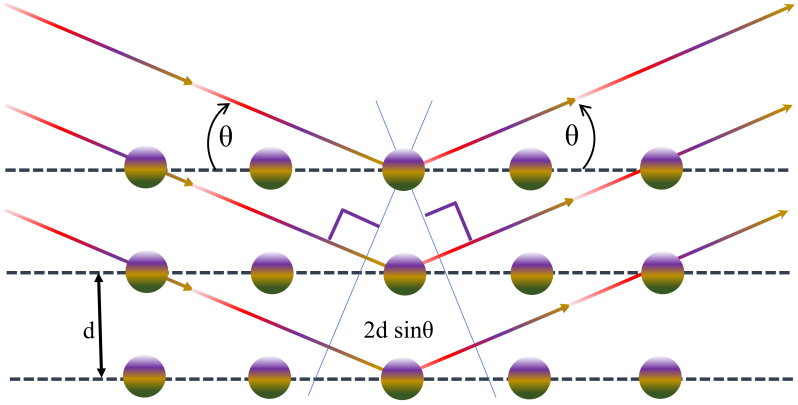

Fig. 2.12 Visualisation of Bragg's Equation.

Here, θ_B is referred to as the Bragg angle, d represents the interplanar spacing, and hkl refers to the Miller indices of the crystallographic plane. n is an integer and is known as the order of the diffraction maxima, with $n = 1$ being the first order, $n = 2$ being the second order, and so forth.

The diffracted X-rays then form a distinct pattern of intensity peaks, known as a diffraction pattern. It contains valuable information about the crystal structure and its properties. The positions, intensities, and shapes of the diffraction peaks provide insights into the lattice spacing between crystal planes, crystallite size, preferred orientation, and the presence of crystal defects. By analyzing the diffraction pattern, researchers can determine the crystal structure, identify the crystalline phases in a sample, and quantify their relative abundances.

XRD utilizes advanced X-ray sources, such as rotating anode generators or synchrotrons, to produce high-intensity and highly collimated X-ray beams. These intense X-rays enhance the signal-to-noise ratio and enable the measurement of weak diffraction signals. Additionally, XRD instruments are equipped with highly sensitive detectors capable of capturing diffraction patterns with high precision and accuracy.

X-ray diffraction (XRD) scanning modes

2θ Scanning

2θ scanning is a fundamental and widely used technique in XRD. It involves rotating the sample stage while fixing the incident and diffracted X-ray angles. Researchers can obtain a complete diffraction pattern by measuring the intensity of diffracted X-rays as a function of the 2θ angle. This scanning mode is beneficial for phase identification, as each crystalline phase has a unique pattern of diffraction peaks. By comparing the experimental diffraction pattern with known reference patterns, researchers can determine the crystalline phases

present in the sample. The precise measurement of 2θ angles is crucial for quantitative analysis and accurate determination of lattice spacing.

Rocking Curve (ω) Scanning

Rocking curve (ω) scanning involves tilting the sample or the detector to vary the incident angle while keeping the diffracted angle fixed as shown in Fig. 2.13. By measuring the intensity of the diffracted beam as a function of the rocking angle (ω), researchers can obtain information about the crystalline quality, crystal tilt, and the presence of defects in the crystal lattice. This scanning mode is advantageous in analyzing epitaxial films and determining the degree of crystallographic alignment. Rocking curve scanning allows for the assessment of crystal mosaicity, which refers to the distribution of crystal misorientations within a sample.

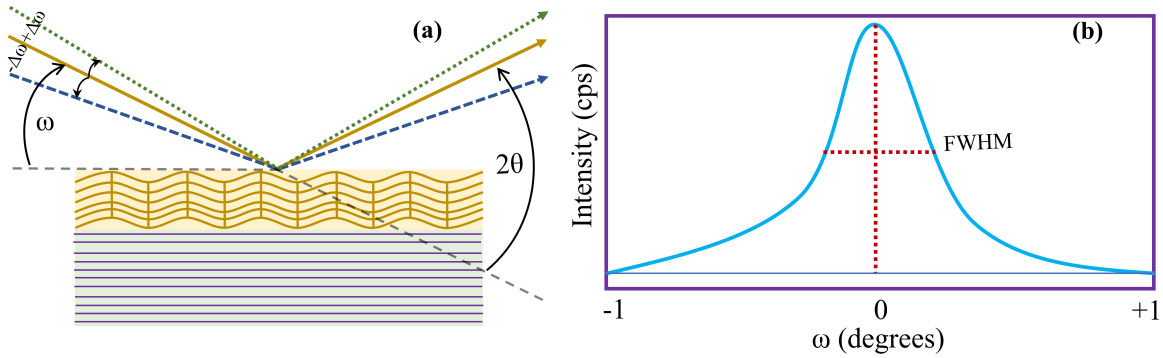

Fig. 2.13 (a) Schematic of a rocking curve measurement and (b) schematic resultant rocking curves from a film and substrate diffraction peak.

These different scanning modes in XRD offer complementary information and are chosen based on specific research objectives. The current work uses CuK_α for X-ray generation. The 2θ was set from 10° to 65°. Then, an omega scan was performed to check the c-axis orientation of the grown CAO thin film.

2.6 Device Characterization

2.6.1 Shadow Masking and Thermal Evaporation in TFT Fabrication

Requirements for TFT fabrication include deposition on insulator/dielectric substrates for electrical isolation, low-temperature processing for compatibility with flexible materials, and the ability to fabricate over large areas with a simple, cost-effective process.

Thermal evaporation represents a widely recognized technique for depositing a thin layer [74]. In this method, the source material undergoes evaporation within a vacuum induced

by high-temperature heating [75]. This process facilitates the movement of vapor particles, allowing them to reach a substrate directly, where they undergo a transition back to a solid state. The method employs a charge-holding boat or resistive coil, typically in the form of a powder or solid bar. To achieve the high melting points required for metals, the resistive boat or coil is subjected to a substantial direct current (DC). The use of a high vacuum, maintained below 10^{-4} Pa, supports the metal's evaporation and directs it towards the substrate. This technique is particularly well-suited for materials characterized by low melting points. Refer to Fig.2.14 for a schematic representation of the thermal evaporation system.

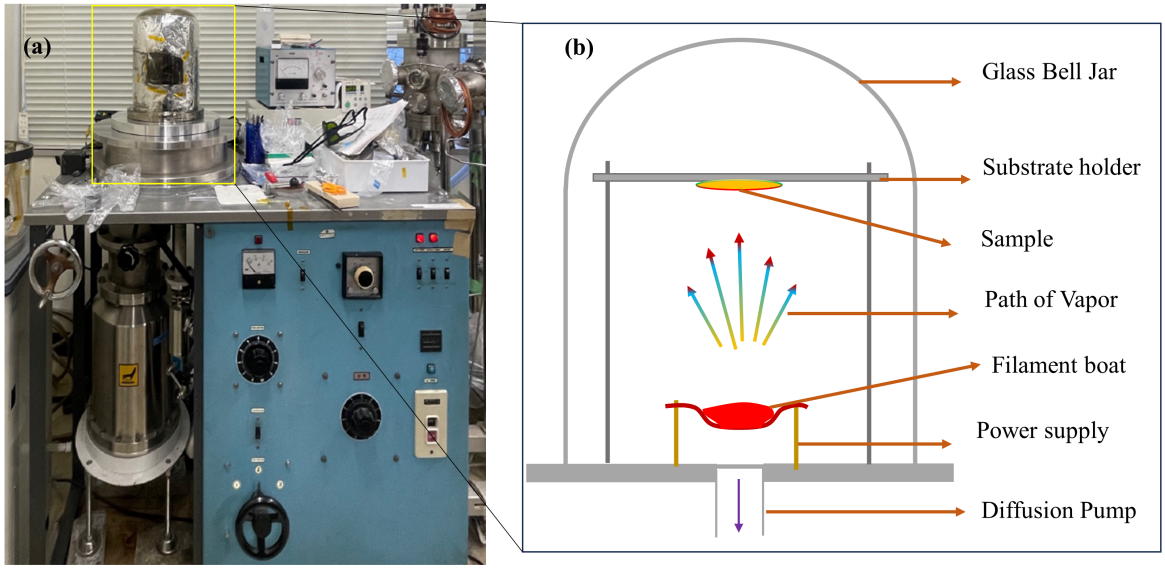

Fig. 2.14 (a) Thermal evaporation coating unit at Isshiki lab and (b) Schematic view of thermal evaporation.

Figure 2.15 illustrates the meticulous fabrication process employed in creating the CAO p-TFT device. The initial step involved thorough cleaning of the surface p-Si/SiO_2 substrate (2.15 (a)) to eliminate contaminants through ultrasonic cleansing with acetone and isopropyl alcoholic solutions, complemented by UV-ozone cleaning. Subsequently, the treated substrate underwent deposition of the CAO thin film in a vacuum evaporation system, followed by the growth of Al electrodes in a thermal evaporation system. First of all, put the Al wire in the tungsten boat, close the glass lead, and switch on the power supply. Meanwhile, run the rotary pump and then TMP to produce the required vacuum in the chamber. After evacuation, the heater was run for about 10 minutes, then rotate the current knob from 5A to 20A with 5 A intervals while waiting for 5 seconds at each interval. To increase the current from 20A to 26A, the interval was set to 2A to avoid any possible current overshooting and to protect the heater. Hence, the thermal evaporation of the front and back electrodes was done. The

CAO thin film was precisely deposited using a DPDS-assisted LBL approach with the aid of a shadow mask (1), as shown in Fig. 2.15 (b). The samples then underwent annealing at an optimized temperature within a furnace annealer. The shadow mask (1) had line and space patterns. Subsequently, Al electrodes were grown by a thermal evaporator using a shadow mask (2), as shown in Fig. 2.15 (c). The shadow mask (2) used for the deposition of source and drain electrodes had line and space patterns in a direction that differed by 90 degrees from those of the mask used for CAO deposition. Finally, the required patterning formed, as shown in Fig. 2.15 (d).

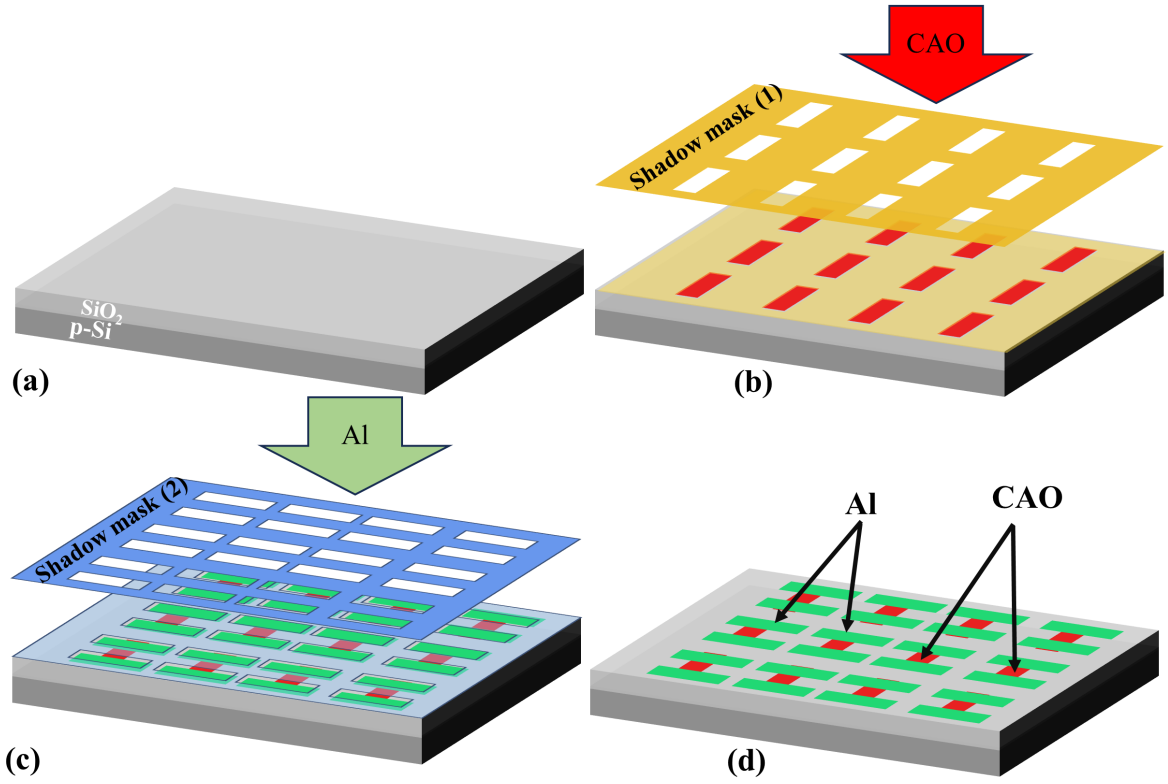

Fig. 2.15 (a) Si-substrate (b) Deposition of CAO channel layer using shadow mask (c) Deposition of Al electrodes using another shadow mask (d) finally deposited TFT structure.

2.6.2 Current-Voltage (IV) measurement for TFTs

In this study, field effect measurements were conducted employing a small, fixed drain-source voltage while monitoring the current in response to variations in gate voltage. The input/output terminals, utilizing shielded cables with BNC connectors, were meticulously constructed. Within the chamber, a copper block served as the substrate holder, maintained in insulation from the enclosure. Electrical connections to the device under test were estab-

lished using three probes within the compartment, connected to the input/output terminals via coaxial cables. Ground terminals of all instruments were interconnected to ensure a common reference. The circuit diagram is schematically shown in Fig. 2.16. Gate-source measurements were performed using a Keithley model 2400b electrometer, while the Keithley source meter facilitated current measurements across the source-drain. For each gate voltage setting, the source-drain current I_{ds} was recorded. A TFT device is biased by applying two voltages: V_{gs} between gate and source and V_{ds} between drain and source. These voltages control the channel current between the drain and source by varying the height of the gate-depletion region and the longitudinal electric field. The operation of a TFT can be divided into different regions based on the output (I_D vs. V_{ds}) and transfer (I_D vs. V_G) characteristic curves: CAO TFT exhibited full depletion for $V_{gs} = 0\,V$ due to the space charge region as shown in Fig. 2.17(a). For increasing gate voltage even less than the threshold voltage, the depletion region begin shrinkage as shown in Fig.2.17(b). For gate voltage greater than the threshold voltage (V_T), a carrier transport layer is formed between the source and drain within the CAO semiconductor due to the shrinkage of the depletion layer as in Fig. 2.17(c). In this region, the depletion region under the gate is relatively narrow, and as V_{ds} increases, a longitudinal electric field is established in the channel, causing the electrons to move faster. The current increases approximately linearly with V_{ds}, making the TFT behave like a voltage-controlled resistor. When V_{ds} is further raised, because of V_{ds}, the voltage across the depletion region is greater at the drain end than at the source end, so the depletion region becomes wider at the drain end as shown in Fig. 2.17(d). The narrowing of the channel and the increased V_{ds} increase the electric field near the drain, causing the electrons to move faster. Although the channel depth, and in turn, the channel's conductive cross-section, is reduced, the net effect is increased current. In this state, the conductive channel is effectively closed off, and both V_{gs} and V_{ds} strongly influence the drain current, leading to a sharp transition from the linear to the saturation region. When V_{ds} is increased beyond the value that causes velocity saturation, the electron velocity cannot increase indefinitely and reaches a saturated drift velocity. In this region, further increases in V_{ds} result in a larger portion of the voltage drop occurring across the electron depletion region near the drain as shown in Fig. 2.17(e). This region, known as a dipole layer or charge domain, maintains current continuity by increasing carrier concentration rather than velocity. Consequently, the drain current becomes almost constant, as any further increases in V_{ds} do not significantly affect I_D.

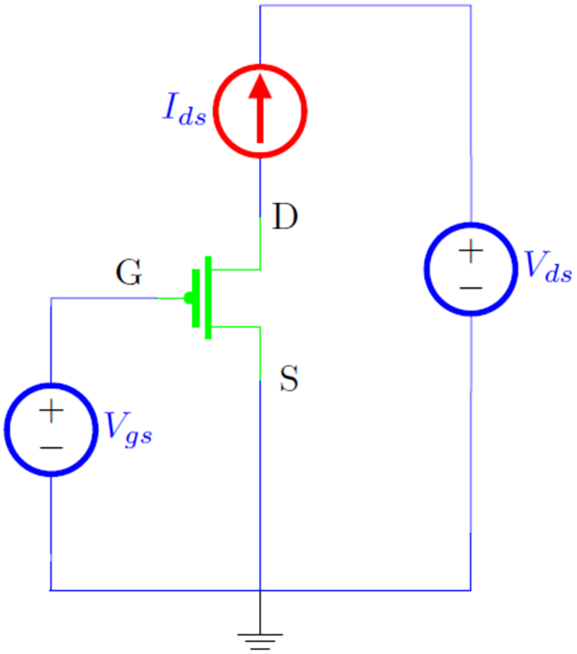

Fig. 2.16 Schematic circuited diagram for electrical evaluation of CAO p-TFT.

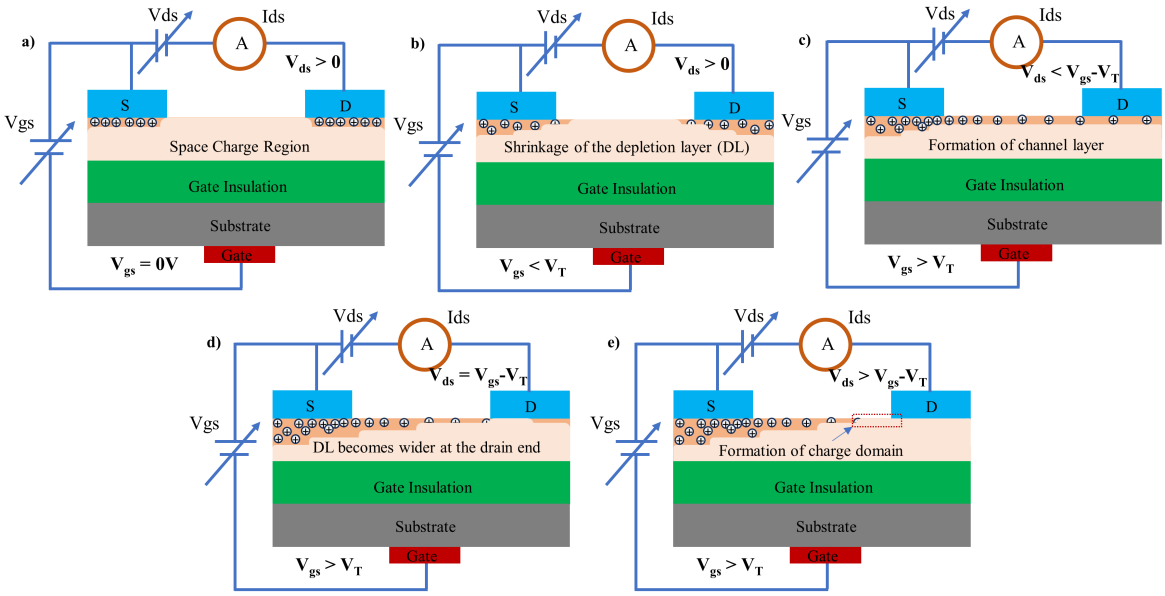

Fig. 2.17 Schematic cross-section of a CAO p-TFT DUT structure and operation Under different V_{ds} biasing a) full depletion, b) shrinkage of depletion region with V_{gs} greater than 0V, c) linear region, d) pinch-off, and e) saturation region.

2.7 Summary: Methodological Approaches for Goal Achievement

Chapter 2 of the thesis addresses the experimental methodologies for synthesizing and characterizing $CuAlO_2$ thin films. The discussion encompasses various preparation techniques. The chapter delves into the complexities of sputtering, elucidating different techniques and the specific requirements of DPDS, while also addressing post-annealing as a crucial step in the synthesis process. Additionally, characterization techniques are discussed, along with device characterization methodologies including shadow masking for thin-film transistor (TFT) fabrication and IV measurements using Keithley electrometers in evaluating the electrical properties of the fabricated TFT devices.

The primary objective of the research is to fabricate high-quality CAO thin films and integrate them as a channel layer in TFT transistors to enhance their electrical performance. Initially, attempts were made to prepare Al-substituted $CuMnO_2$ using the sol-gel auto-combustion technique. However, achieving satisfactory crystalline CAO proved elusive, as even at high calcination temperatures of 1200°C for 1 hour, the film exhibited a polycrystalline nature. Furthermore, addressing deficiencies in Cu-O-Cu lattice connectivity through layer-by-layer improvement under the sol-gel method was challenging.

In response, this study adopted the DPDS-conducted LBL approach for CAO thin film growth, marking the first instance of such an approach being utilized to address these challenges. This method enabled layer-by-layer deposition, facilitating *c*-direction stacking of CuO and AlO to focus on achieving the desired *d*-spacing of the (002) plane for optimal CAO crystallinity. XRD analysis confirmed the *c*-axis dominance of the (004) plane of CAO. The EPMA analysis validated Cu/Al stoichiometry, while FESEM revealed an increase in grain size with annealing due to coalescence. Through shadow masking, the channel on the gate dielectric and electrodes on the CAO channel layer was successfully deposited, resulting in a CAO p-TFT fabrication.

The LBL approach allowed precise control over the growth process, facilitating ordered stacking of CuO and AlO and the formation of long-range structural integrity, which is believed to enhance carrier transport efficiency. This method yielded a mobility improvement of $4.1\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ in the saturation region, with TFT characteristics also observed in the as-deposited CAO transistor.

Chapter 3

Growth of $CuAlO_2$ by sol-gel auto-combustion method

Chapter 3 focuses on the synthesis and characterization of $CuAlO_2$ utilizing the sol-gel auto-combustion method and exploration of the synthesis limits using the sol-gel process.

3.1 Fundamental properties of the $CuAlO_2$

3.1.1 Crystalline structure

$CuAlO_2$, a ternary oxide, is one of the prominent members of the delafossite family having the composition formula ABO_2, where the letter A represents a monovalent metal cation (i.e., Cu^+, Ag^+, Pd^+, etc.) linearly two-fold coordinated to two oxygen ions. In contrast, the letter B represents a trivalent metal cation (i.e., Al^{3+}, Ga^{3+}, etc.) octahedrally coordinated with oxides. Being a part of the delafossite family, $CuAlO_2$ is composed of AlO_6 octahedra spread out, forming a basal layer and alternating stacking layers of the $O-Cu-O$ dumbbell structure vertically. The Cu atom is linearly linked with two O atoms along the c-axis, and the Al atom is octahedrally linked with six O atoms. In the context of stacking, two polytypes are reported: rhombohedral 3R type with R3m space group symmetry and hexagonal 2H type with space group symmetry of P63/mmc. The two structures arise as a consequence of the different orientations of the triangular metallic plane along the c-axis. Whenever two consecutive A layers rotate by 180° to each other, they form a hexagonal structure, as shown in Fig. 3.1(b). In contrast, when they stack in the same direction as one another, they form a rhombohedral structure, as depicted in Fig. 3.1(a). Rhombohedral primitive cells consist of one formula unit of ABO_2 with four atoms giving 12 vibrational modes. In contrast, the

hexagonal structure consists of two formula units per primitive cell, resulting in 24 modes of vibration at the zone center [76].

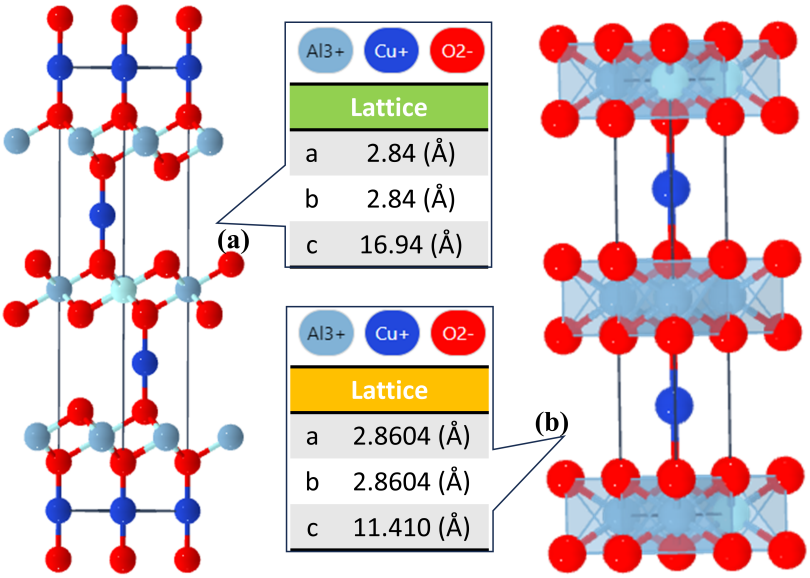

Fig. 3.1 The crystal structure of $CuAlO_2$ a) rhombohedral structure, b) hexagonal structure

3.1.2 Electronic properties

The electronic structure of $CuAlO_2$, by the density of state (DOS), is shown in Fig 3.2 where the blue line denotes the Fermi level was fixed at 0 eV. The VB is mainly consistent in O; 2p, Cu; 3d orbit, which is responsible for p-d coupling, and the CB consists of Cu; 3p and O; 2p orbit [77]. The chemical bonding properties are calculated by Mulliken atomic population and bound population in order to estimate the bond strength and charge transfers.

3.1.3 Optical properties

$CuAlO_2$ exhibits intriguing optical properties that stem from its unique crystal structure and electronic configuration. The compound manifests a remarkable bandgap in the visible region of the electromagnetic spectrum, rendering it highly relevant for optoelectronic applications. When subjected to incident light, $CuAlO_2$ undergoes intricate interactions, giving rise to many optical phenomena that merit comprehensive investigation. Significance transparency is desirable in the visible spectrum to make CAO applicable in optoelectronic technology. In CAO, oxygen vacancy raises an absorbed band of 1.65 eV-2.10 eV, significantly reducing its transparency in the visible region [78]. $CuAlO_2$ exhibits a fascinating array of optical properties owing to its distinctive band structure, transparent characteristics, dispersive

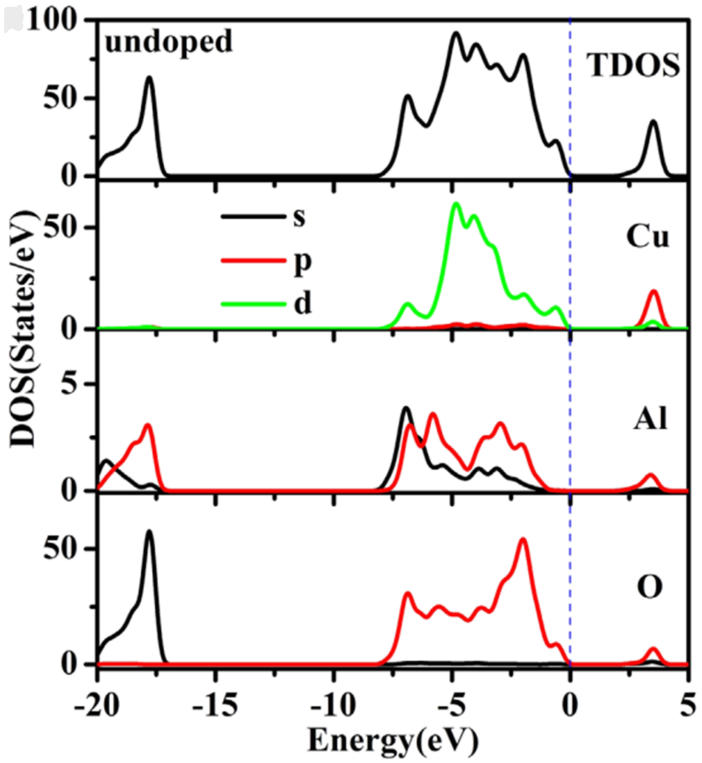

Fig. 3.2 The electronic structure of $CuAlO_2$, by the density of state (DOS) [77].

behavior, optical anisotropy, and luminescent phenomena. These attributes make $CuAlO_2$ a promising material for optoelectronic applications, including photovoltaics, displays, and sensors.

3.1.4 Phase diagram

Such a graph depicts the limiting physical condition of compound materials at which one or more phases can show their existence in thermodynamic equilibrium. Copper oxide with alumina forms two compounds, $Cu(AlO_2)_2$ and $CuAlO_2$, with different ranges of temperature stability. Misra [79] prepared copper oxide-alumina systems by solid-state reaction and examined the formation of $Cu(AlO_2)_2$ at about 800 °C. Till 1000 °C, it was stable. Then, it converted into $CuAlO_2$, which was stable at 1260 °C as in Fig.3.3. Moreover, the coexistence of Cu_2O and CuO is noticed in the temperature ranges of 900-1000 °C [79].

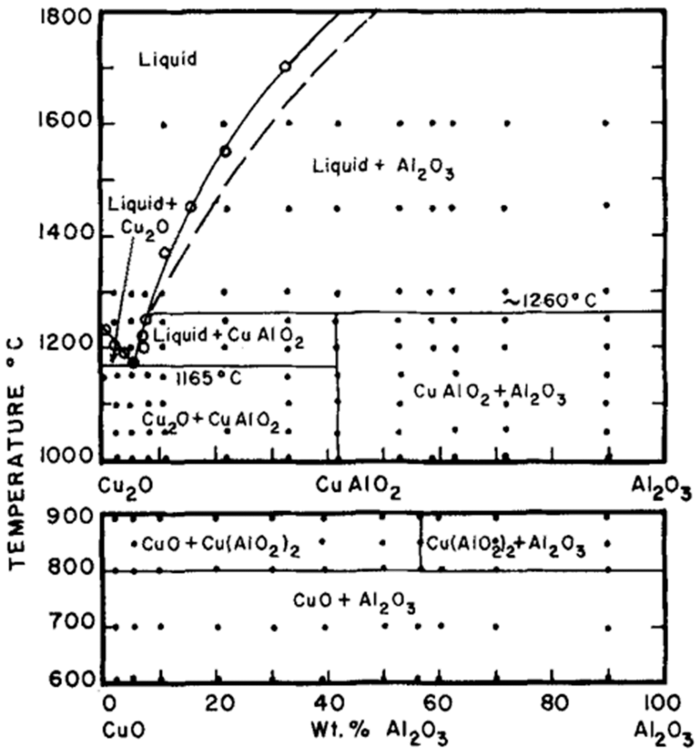

Fig. 3.3 Phase diagram of CuO-Al_2O_3 and Cu_2O-Al_2O_3 [79].

3.2 Synthesis of CAO by using sol-gel method and characterization

Sol-gel is a wet chemical technique. The term Sol-gel is the combination of the words Sol and Gel. Sol represents the liquid state of a colloidal solution, while gel represents the semi-solid state of this colloidal solution. Sol-gel involves the formation of a homogeneous solid-liquid network where both liquids and solids are dispersed in each other. It is a wet chemical technique that facilitates the conversion of monomers into colloidal form.

In the sol-gel method, all the required individual materials are mixed to form a homogeneous solution. This solution is then subjected to heat treatment on a hotplate. Heating continues until the critical temperature is reached, triggering auto-combustion, leading to the final burnout of the gel, resulting in a fine powder.

Sol-gel techniques are typically attempted before sputtering due to several advantages. Firstly, it is a simple and user-friendly process that does not require an expert to operate. Additionally, the precursors used in sol-gel are relatively low-cost compared to the metallic targets used in sputtering. The process is also completed in a shorter timeframe. Furthermore, sol-gel offers excellent stoichiometric control and allows for the homogeneous mixing of

multiple components. Auto-combustion in sol-gel occurs at a lower temperature compared to other techniques.

Moreover, solution-based techniques have been successfully employed in the fabrication of the $CuAlO_2$ and integrated as a channel layer for TFT transistors. Drawing inspiration from the success of sol-gel techniques in previous studies, I decided to fabricate my samples using the sol-gel synthesis technique.

3.2.1 Sample preparation

Al-substituted compositions of $CuMn_{1-x}Al_xO_2$ ($x = 0.00, 0.20, 0.40, 0.60, 0.80, 1.00$) were synthesized using a cost-effective sol-gel auto-combustion route. In this method, Copper nitrate trihydrate ($Cu(NO_3)_2 \cdot 3H_2O$, $\geq 98\%$), Manganese nitrate tetrahydrate ($Mn(NO_3)_2 \cdot 4H_2O$, $\geq 97\%$), and Aluminium nitrate nonahydrate ($Al(NO_3)_3 \cdot 9H_2O$, $\geq 98\%$) served as precursors. Glycine ($C_2H_5NO_2$) and urea ($CO(NH_2)_2$) were employed as fuel agents in a 2:1 ratio with metal nitrates. The preparation process is illustrated stepwise in Fig. 3.4. Initially, the required metal nitrates were sequentially dissolved in deionized water to form a homogeneous solution. This solution was then placed in a 100 ml beaker and heated on a hot plate within an Esco fume hood. The temperature was gradually increased below the boiling point of water until a viscous solution (xerogel) formed. Subsequently, the temperature was raised to 230 °C-300 °C, initiating an exothermic reaction leading to auto-combustion. After combustion, the samples in ash form were collected and ground using an Ager Mortal pestle. The resulting powder underwent calcination at 1200 °C for one hour to ensure phase purity and optimal crystal growth. The finely calcined powder was pelletized using an Apex hydraulic press with a 30 kN force application, yielding smooth circular pellets with a 7 mm diameter and a thickness of 1.08 mm to 1.16 mm.

3.2.2 Structural analysis

X-ray diffraction (XRD) patterns play a crucial role in indexing peaks, lattice parameters, unit cell volume, crystallite size, X-ray density, bulk density, and the porosity of the samples. XRD was employed to verify the crystalline nature of the synthesized samples. The obtained XRD patterns were meticulously compared with JCPDS cards using PANalytical X'Pert High Score Plus software, confirming the phase purity of the synthesized samples.

For the case of $x = 0.00$, the diffraction peaks at 2Θ values of 31.31°, 35.32°, 36.96°, 37.52°, 39.92°, 44.56°, 48.81°, 56.85°, 59.55°, 61.02°, 64.58°, 66.32°, 67.73°, 73.52°, 77.09° were corresponding to the planes (002), (110), (-111), (11$\bar{1}$), (-202), (-112), (003), (-113), (-311), (310), (020), (-202), (-401), (022), (410), respectively. These peaks aligned well

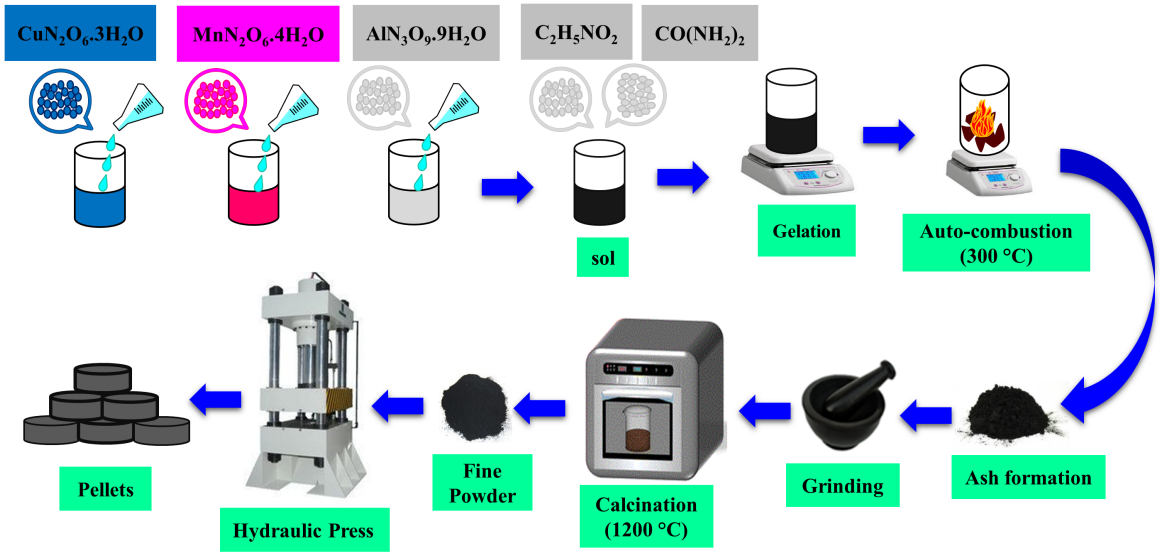

Fig. 3.4 Schematic diagram of the synthesis of $CuMn_{1-x}Al_xO_2$ by the sol-gel technique.

with ICSD file No. 03-065-2308, confirming the monoclinic crystal structure for $CuMnO_2$ [80].

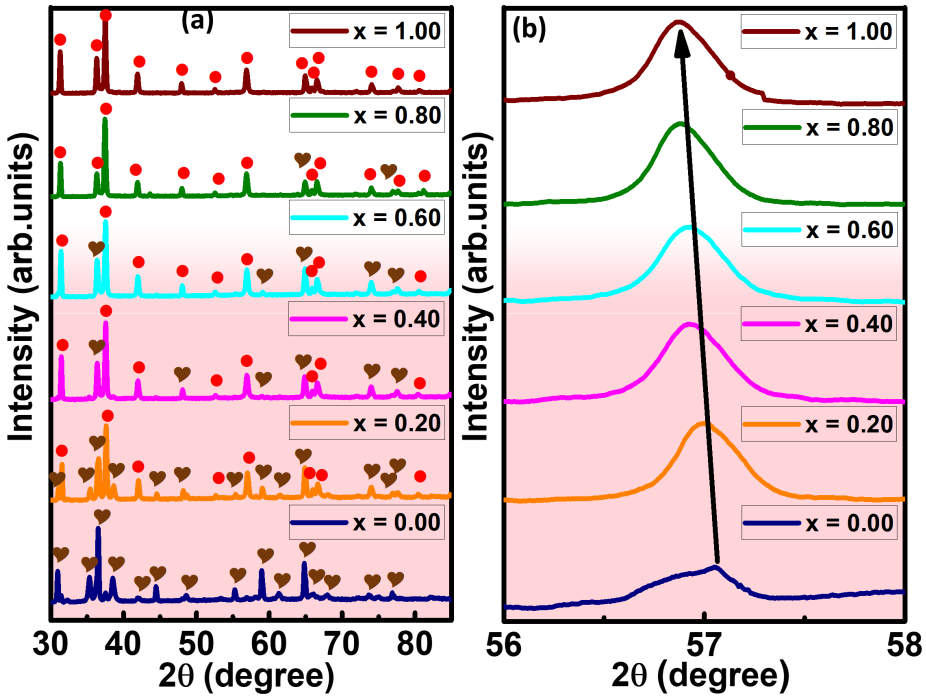

Fig. 3.5 XRD pattern of Al-substituted $CuMn_{1-x}Al_xO_2$; monoclinic peaks indicated by the heart symbol and hexagonal peaks by the red ball symbol.

As the aluminum substitution content (x) increased, mixed phases, including hexagonal phases, were observed. In Fig. 3.5, an increase in x resulted in the elimination of the monoclinic phase and the simultaneous formation of the hexagonal phase. The X-ray diffraction peaks for the Al composition with $x = 1.00$ were observed at 2Θ angles of 31.67°, 36.69°, 37.85°, 42.28°, 48.31°, 52.87°, 57.22°, 65.26°, 66.12°, 66.87°, 74.35°, 77.97°, 80.89°. These peaks corresponded to the crystallographic planes (006), (101), (012), (104), (009), (107), (018), (110), (0012), (1010), (116), (202), (024), respectively. The observed patterns align with the ICSD file No. 01-075-1792, indicating that the sample $CuAlO_2$ possesses a hexagonal structure in space group P63/mmc [81]. Moreover, a noticeable shift of peaks towards lower angles was observed with an increase in the aluminum content. This shift, depicted in Fig. 3.5, supports the interpretation of an enlargement of the unit cell.

a) Structural parameters evaluation

Various analytical techniques, formulations, and software were utilized to calculate structural parameters. The crystallite size (D) was determined using the Bragg's law [82] from eq. 3.1

$$D = \frac{0.9\lambda}{\beta \cos\theta} \tag{3.1}$$

where θ is Bragg's angle, λ is the wavelength of CuK_α, and β is full-width half maximum (FWHM). Changes in crystal structure were assessed by considering volume-mass density.

The bulk density (ρ_b) was calculated using the relationship as in eq.3.2

$$\rho_b = \frac{m}{\pi r^2 h} \tag{3.2}$$

Where m, r, and h represent the mass, radius, and thickness of the pellets. The X-ray density (ρ_x) was calculated by eq. 3.3

$$\rho_x = \frac{zM}{N_A V} \tag{3.3}$$

where z, M, N_A, and V represent the formula unit, molar weight, Avogadro's number, and volume of the pellets, respectively.

Porosity (P), a measure of sample porosity, was calculated by eq. 3.4.

$$P = 1 - \frac{\rho_b}{\rho_x} \tag{3.4}$$

The summarized values of these structural parameters are presented in Table 3.1.

Table 3.1 Structural parameters of $CuMn_{1-x}Al_xO_2$ ($x = 0.00$ & 1.00)

Parameters	$CuMnO_2$	$CuAlO_2$
Crystal system	Monoclinic	Hexagonal
Space group	C2/m	P63/mmc
Lattice constant (Å)		
a	5.5300	2.8567
b	2.8840	2.8567
c	5.8980	11.293
Angles (°)		
α	90	90
β	104.6	90
γ	90	120
Volume of unit cell ($Å^3$)	91.02	119.7
Crystallite size (Å)	62.245	64.219
X-ray density: ρ_x (g/cm^3)	5.490	5.045
Bulk density: ρ_B (g/cm^3)	1.699	1.781
Porosity	0.69	0.64

3.2.3 Morphological analysis

The morphological analysis of Al-substituted $CuMnO_2$ was conducted using a FESEM. Grain sizes were measured using Java-based ImageJ software. Figure 3.6 illustrates the morphology of samples at magnifications of 10,000, with an operating voltage of 10 kV. SEM images reveal that the crystallites exhibit nonuniform, irregular, and porous shapes with different grain sizes at various Al contents. For Al content ($x = 0.00$), nearly circular and tube-like grains were uniformly distributed. As the Al content increased to 20 wt.%, grain size enlarged due to coalition and the formation of agglomerated clusters of smaller particles. At 40 wt.% Al content, most grains transformed into layers, coexisting with small grains. Additionally, at 60 wt.% Al content, samples predominantly consisted of uniform layers, accompanied by a reduction in grain size. This reduction is associated with suppressed oxygen vacancies, contributing to enhanced crystallinity by limiting oxygen contents.

For Al contents up to 80 wt.%, uniform layers began to decompose into larger grains and nonuniform layers. In this case, grain size increased again when the Al content reached 100 wt.%, featuring uniformly distributed layers. The uniformity in layers is attributed to thermal treatment, where oxygen vacancies are compelled for motion, exerting a significant influence on grain growth [83]. The variation in average grain sizes based on substituent contents is presented in Table 3.2.

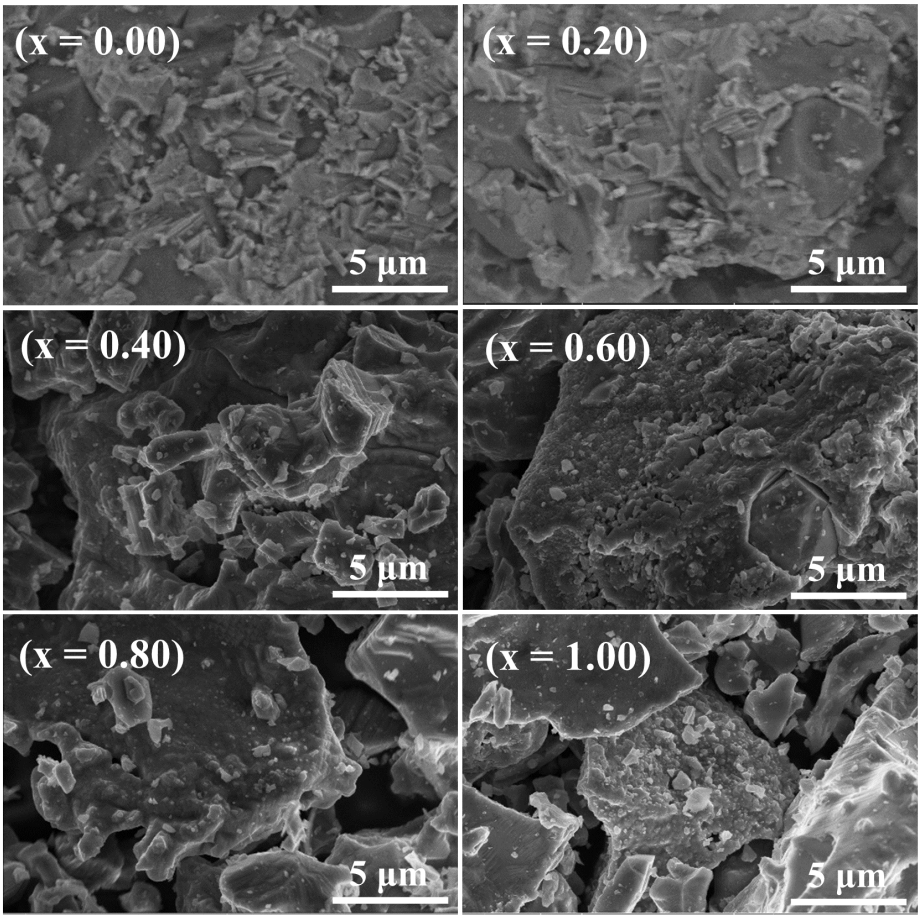

Fig. 3.6 Morphology of Al-substituted $CuMnO_2$ at 10,000 magnification, 10 kV.

3.2.4 Energy dispersive X-ray (EDX) analysis

EDX analysis provides insights into the actual elemental composition of the samples. The elemental percentage of each constituent can be determined by analyzing the graph plotted between the intensity of emitted X-rays and energy as illustrated for $CuMn_{1-x}Al_xO_2$ in Fig. 3.7. The recorded weight percentage for all the samples is summarized in Table 3.3. The EDX spectra confirm that the samples consist of Cu, Mn, Al, and O in stoichiometric ratios, aligning with their respective empirical formulas. For Al content ($x = 0.00$), Mn and Cu exhibit their highest elemental concentration. As the substituent content increases, there is a

Table 3.2 Variation in grain size with the substituent content of Al in $CuMn_{1-x}Al_xO_2$

x	0.00	0.20	0.40	0.60	0.80	1.00
Grain size (nm)	200	363	203	108	156	126

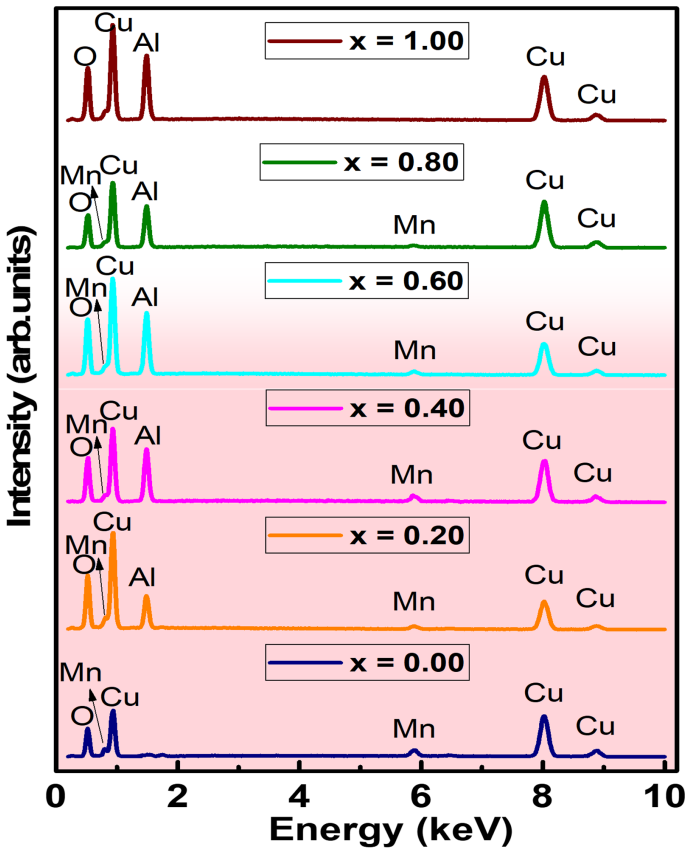

Fig. 3.7 EDX analysis of Al-substituted $CuMnO_2$.

slight decrement in Mn peaks, accompanied by the appearance of a new peak, signifying the presence of Al. With increasing Al substitution (i.e., $x = 0.20, 0.40, 0.60, 0.80$), a clear and distinct decrease in Mn peaks is observed. Finally, for Al content ($x = 1.00$), the elimination of the Mn peak indicates the successful replacement of Mn by Al. The EDX spectra thus confirm a perfect elemental composition as mentioned in Table 3.3.

3.2.5 Frequency-dependent dielectric analysis

Frequency-dependent dielectric analysis was conducted using the Wayne Kerr 6500B precision impedance analyzer over a frequency range from 20 Hz to 20 MHz at room temperature. Pellets of the synthesized material were carefully positioned between two metal electrodes, and an alternating current (AC) signal was applied. Through this procedure, the values of parallel capacitance (C_p) and parallel resistance (R_p) were systematically determined. This method allows for a comprehensive examination of the dielectric properties of the material under varying frequencies.

Table 3.3 Weight %age of all the elements in $CuMn_{1-x}Al_xO_2$ ($x = 0.00, 0.20, 0.40, 0.60, 0.80, 1.00$) by EDX

Substituent	x=0.00	x=0.20	x=0.40	x=0.60	x=0.0	x=1.00
Formula Unit	wt.%	wt.%	wt.%	wt.%	wt.%	wt.%
Cu	67.1	55.95	58.50	55.00	64.35	54.59
Mn	6.07	4.89	3.57	1.93	0.96	0.00
Al	0.00	9.59	15.26	16.20	17.36	19.18
O	26.83	29.57	22.67	26.87	17.33	26.23

a) Complex dielectric constant

Dielectric materials are unique insulating materials that exhibit charge-storing capability for an applied electric field. These materials are fundamental building blocks of a capacitor and essential components of electronics. The dielectric constant is a measure of electrostatic energy per unit volume. The dielectric behavior depends on the frequency of the applied electric field, temperature, elemental composition, and crystal structure of the samples.

The dielectric response of materials is described by $\varepsilon = \varepsilon' + i\varepsilon''$, where ε' represents the real component, and ε'' represents the imaginary component of the dielectric constant. The quantity of stored energy is described in terms of the real dielectric constant, while the amount of energy lost during polarization phenomena can be quantified via the imaginary dielectric constant.

Dielectrics are comprised of random charged particles. When an electric field is applied, these charged particles orient in a way that induces polarization phenomena. In response to a sinusoidal electric field, these polarized particles reverse their polarity in accordance with the electric field. Using the eq. 3.5 the real part of the dielectric constant (ε') was calculated.

$$\varepsilon' = \frac{Cd}{A\varepsilon_0} \tag{3.5}$$

where C, d, A, and ε_0 represent the capacitance of the capacitor, the thickness of the pellet, the flat surface area of the pellet, and the permittivity of free space, respectively. The real dielectric component of all compositions as a function of log frequency and with substituent contents is plotted in Fig. 3.8a) and in Fig. 3.8b), respectively.

In Fig. 3.8(a), ε' initially shows the maximum value, but there is a sharp decrement with increasing frequency at a lower frequency range. The dielectric constant for each sample at lower frequencies is high due to enough relaxation time; the carriers easily accumulate at the interface, contributing to the polarization of the materials. In the context of time relaxation (τ),

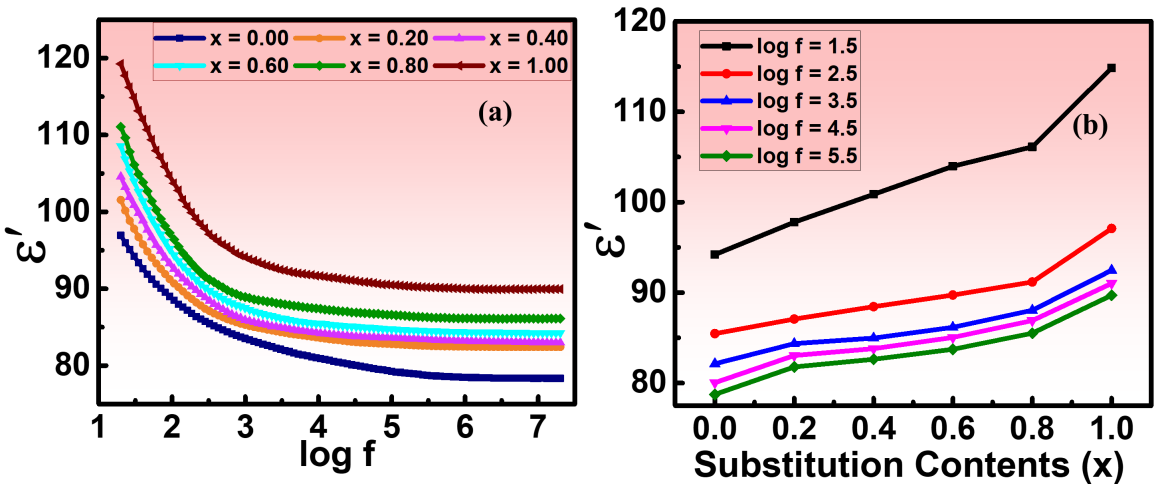

Fig. 3.8 a) ε' as a function of log frequency, b) ε' as a function of substituent content.

which may be expressed by $\tau = \frac{1}{2\pi f}$ where f is the applied frequency. According to Koop's theory, the dielectric material is made up of a double layer. In the case of heterogeneous structures, the grain core acts as a conductive layer, while the grain boundaries act as an insulator due to defects and higher density. Charges accumulate on the interfaces, i.e., between core and grain boundaries. At the nano level, the increment in the surface-to-volume ratio of different grains makes materials favorable for interfacial polarization. In addition, the localized growth of charges will be induced on the high-conducting phases of the grain boundaries with the application of an electric field [84].

It is also reported that all types of polarization mechanisms, i.e., electronic, ionic, orientation, and space charge, occur at lower frequencies [85]. As a result, the sample shows a high dielectric constant. However, the value of dielectric constants decreases with the increments in frequency due to the difficulties faced by the carriers in accumulation at interfaces due to too short a time to align itself following frequency. In such cases, only certain types, i.e., electronic and atomic polarization, occur; as a result, the polarization in a sample decreases. It was noticed that the dielectric exhibits nearly constant behavior at higher frequencies.

The real part of permittivity in terms of substituent content is shown in Fig. 3.8(b). Mn is a magnetic element, while Al is a non-magnetic metal element. Magnetic material always shows low polarizability. In this way, the replacement of the Mn site with Al substituent causes a gradual increment in ε' for the compositions.

b) Tangent loss

The power dissipation factor is termed as a dielectric loss. Dielectric loss is related as $\varepsilon'' = \varepsilon' \tan\delta$. This equation reveals that the imaginary part of the dielectric linearly depends

on tangent loss as well as on real parts of the dielectric constant. ε'' and $\tan\delta$ can also be explained on the basis of Koop's phenomenological theory. This theory states that at lower frequencies, the resistive nature of the grain boundary is active and requires high energy for the hopping mechanism, and vice versa at higher frequencies. Tangent loss of the compositions was calculated by eq. 3.6.

$$\tan\delta = \frac{1}{2\pi f R_P C_P} \tag{3.6}$$

where f, R_P, and C_P represent the applied frequency, resistance, and capacitance of the parallel circuit, respectively. The calculated tangent loss factor was plotted in Fig. 8(c) as a function of frequency.

The phase difference between applied current-voltage and induced I-V causes the power loss in a thermal form, which is attributed to the tan loss. Whenever an AC signal passes through a resistance, both the current (I) and voltages (V) will remain in phase. However, in the case of the capacitor, the currents and voltages will be out of phase. When dielectric materials are subjected to an AC signal, due to capacitive behavior, the voltage inside the material always lags behind the applied voltage. During this mechanism, most of the electrical energy will be stored; however, some of the energy will be dissipated. The energy that dissipates in the form of heat is termed as tan loss.

At lower frequencies with enough relaxation time, most of the dipoles can rotate as well as flip. In this way, almost all kinds of polarization mechanisms occur. The contributions of these polarization mechanisms maximize the value of real as well as imaginary dielectric constant. In addition, I-V phases can easily follow the alternating E-field if they have enough time. As a result, at lower frequencies, the contribution of tangent losses is maximum.

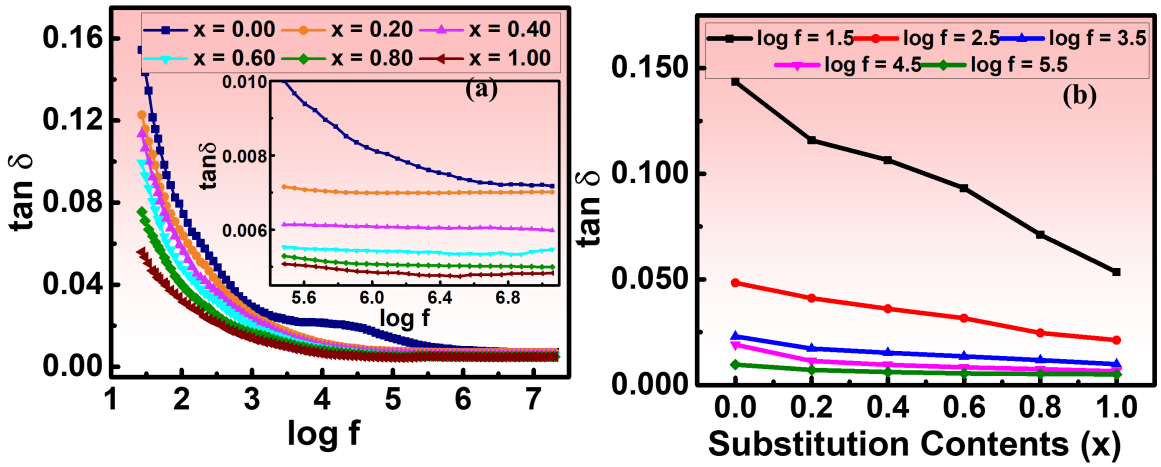

Fig. 3.9 a) $\tan\delta$ as a function of log frequency, b) $\tan\delta$ as a function of substituent content.

At upper frequency, due to the negligible contribution of polarization and difficulties in following the E-field, the tangent losses seem to be seized up. Figure 3.9(b) shows the variation caused by the Al substituent contents to the Mn site. It has been reported that the chemical composition, sintering temperature, structural homogeneity, stoichiometry, and substituent concentrations have an important effect on $\tan\delta$ [86]. In our case, the graphs revealed that with increasing Al contents, tan-loss consistently decreased. Hence, it is concluded that the Al substituent minimized the resistive behavior and improved the capacitive nature of the compositions.

c) Complex impedance analysis

Impedance represents the total opposition faced by mobile charge carriers as they traverse a material. It proves instrumental in studying particle-to-particle interactions and the microstructure of the material and indicating potential impurities [87]. Total impedance comprises real and imaginary components, expressed as $Z(\omega) = Z'(\omega) + iZ''(\omega) = 1/(i\omega\varepsilon C_0(\omega))$, where $Z'(\omega)$, $Z''(\omega)$, and C_0 represent the real component of impedance, imaginary component of impedance, and capacitance of free space, respectively.

In Fig. 3.10(a) and 3.10(b), the real and imaginary parts of impedance contributed by grain and grain boundaries of any sample are depicted, drawing an analogy with the RC (Resistance-Capacitance) circuit. At lower frequencies, owing to the resistive nature of grain boundaries, a negligible amount of carrier hopping occurs, resulting in maximum impedance for all compositions. As the frequency increases, a decreasing trend of Z' for all samples is observed, indicative of an enhanced conduction mechanism. The rise in conduction at higher frequencies is attributed to the hopping of localized ions and the transport of charge carriers through grain boundaries. Fig. 3.10(a) reveals that the substitution of Al at the Mn site causes a sequential decrease in the impedance of the compositions. This suggests an improvement in the resistive nature of the sample with increasing Al substituent contents.

In Fig. 3.10(b), the imaginary part of the impedance, Z'', is presented. Z'' elucidates the capacitive reactance of the sample. The decreasing trends in Z'' with increasing frequency are associated with enhanced capacitance. This augmentation of capacitance in heterogeneous material is attributed to space charge polarization [88].

d) Nyquist plot

Nyquist plots provide valuable insights into impedance data, particularly in understanding the resistance and reactance offered by a sample. The complex impedance data is associated with the resistance and reactance, depicting the flow of alternating current within the material,

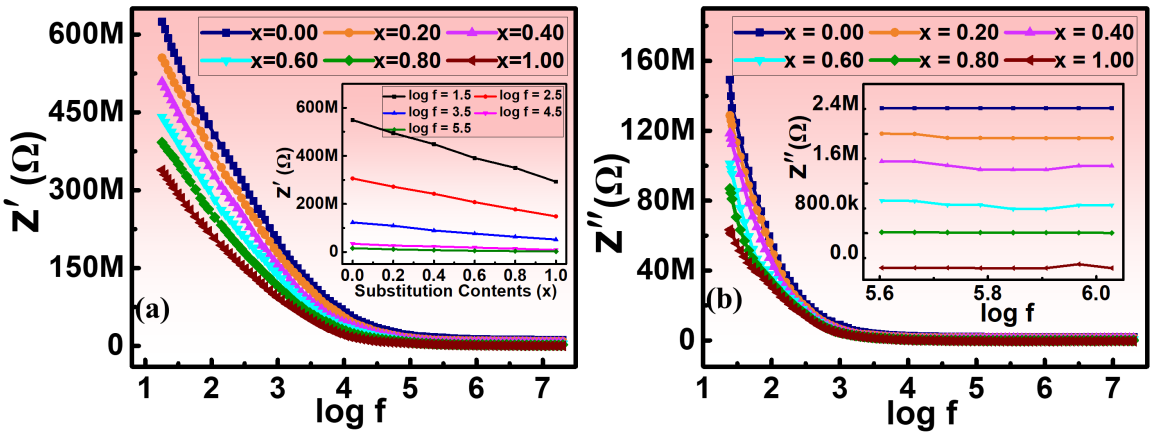

Fig. 3.10 a) Z' as a function of log frequency, b) Z'' as a function of log frequency.

which experiences a shift in phase angle and amplitude. The Nyquist graph is plotted between real impedance (along the x-axis) and imaginary impedance (along the y-axis), as illustrated in Fig. 3.11(a), following the RC parallel equivalent electrical circuit.

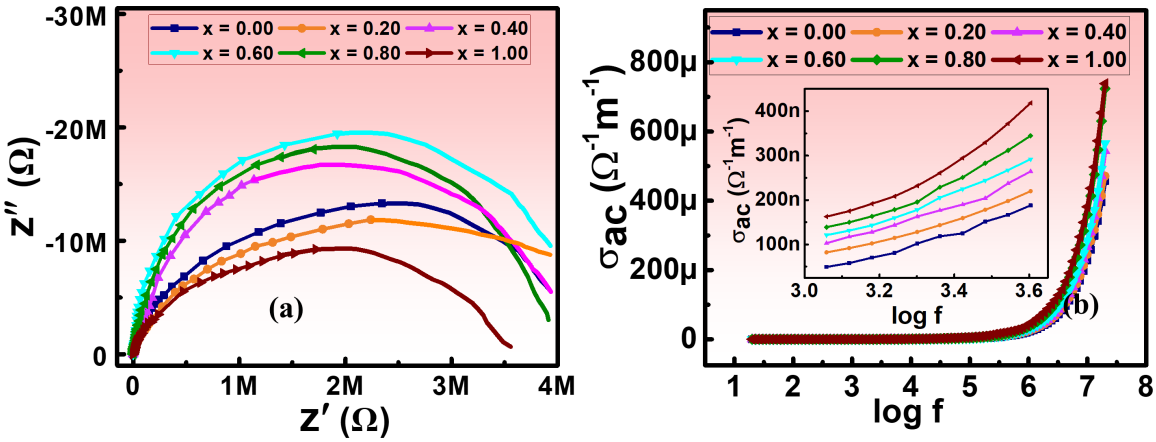

Fig. 3.11 a) Z' vs. Z'', b) conductivity as a function of log frequency.

In Fig. 3.11(a), all samples exhibit a single semicircle arc, indicative of non-Debye relaxation with different time constants [89]. These semicircles are correlated with microstructure, reflecting the influences of grain, grain boundary, and electrode effects. Each semicircle arc corresponds to a parallel RC combination. With an increase in Al substituent content, the diameter of the arcs decreases, suggesting a transition from resistive to conductive behavior. From the topmost point of the arc, the value of capacitive reactance (X_c) is obtained, while from the point of intercept at the x-axis, the value of grain resistance (R_g) is calculated [90]. The R_g values were found in the range of 3.6 MΩ to 4.9 MΩ. Furthermore, the grain

capacitance (C_g) was calculated using the eq. 3.7.

$$C_g = \frac{1}{2\pi f X_C} \tag{3.7}$$

where C_g was found in the range of 31.3 pF to 85.5 pF. The calculated values of R_g and C_g for all compositions are tabulated in Table 3.4.

Table 3.4 (R_g) and (C_g) of $CuMn_{1-x}Al_xO_2$ samples

x	0.00	0.20	0.40	0.60	0.80	1.00
R_g (MΩ)	4.9	4.5	4.3	3.9	3.7	3.6
C_g (pF)	48.5	62.6	49.9	33.5	31.3	85.4

e) Conductivity

Ideal dielectric materials, characterized by closed-packed atomic structures, act as perfect insulators. However, conduction phenomena arise from impurities and minor charge carriers, leading to leakage currents.

The AC conductivity of dielectric materials was calculated using the relation $\sigma_{AC} = \varepsilon' \varepsilon_0 \omega \tan\delta = 2\pi f \varepsilon' \varepsilon_0 \tan\delta$, where ω is the angular frequency. This relationship clarifies that σ_{AC} linearly depends on frequency. Jonscher's relation, introduced in 1977, further describes AC conductivity: $\sigma_{AC}(\omega, T) = A\omega^n$, where A is a constant with units of conductivity and n is a dimensionless quantity in the range of $0 < n < 1$. The calculated AC conductivity response to alternating frequency is plotted in Fig. 3.11(b). At lower frequencies, AC conductivity is almost constant and minimal, whereas at higher frequencies, an exponential increase is observed. At higher frequencies, hopping occurs more easily. Maximum conductivity is reported when the applied frequency equals the frequency of hopping carriers [91]. In conclusion, at the upper-frequency range, the resonance effect of both frequencies results in maximum conductivity. Increasing trends in Fig. 3.11(b) with substituent content are attributed to the hopping of electrons between localized states [92].

3.3 Limitations of the Sol-Gel method in synthesizing $CuAlO_2$

The synthesis of Al-substituted $CuMn_{1-x}Al_xO_2$ samples through the sol-gel auto-combustion route using nitrate precursors demonstrated various challenges and limitations associated with the sol-gel method.

To integrate the CAO as a channel layer in TFT demands high-quality films. However, the structural analysis with a Bruker D8 advanced diffractometer revealed a polycrystalline nature for CAO as the sol-gel does not facilitate direct crystallization of the sample materials. Moreover, the SEM images exhibited irregular and non-homogeneous grains for CAO. Channel layer with huge porosity and distorted grains due to nonuniformity and disorder layering causes significant scattering for the carriers that affects the electrical performance of the device.

For electronic applications controlling the film thickness, bringing uniformity in thin films, and achieving precise deposition are essential; however, these are not possible in the case of the sol-gel synthesis method. The sputtering technique, in contrast, offers precise control over film thickness and composition, making it a more suitable alternative for achieving high-quality thin films. Subsequently, (CAO) was deposited on Si-substrate by DPDS sputtering for further investigation.

3.4 Summary of Chapter 3

Chapter 3 of the thesis delves into the growth of $CuAlO_2$ utilizing the sol-gel auto-combustion method, comprehensively exploring the fundamental properties of the synthesized material. The chapter scrutinizes various aspects including crystalline structure, electronic properties, optical properties, and phase diagram of CAO. Furthermore, it elucidates the synthesis process through the sol-gel method and subsequent characterization techniques employed. These techniques encompass sample preparation, structural analysis, morphological analysis, energy dispersive X-ray (EDX) analysis, and frequency-dependent dielectric analysis, providing a detailed understanding of the material's composition, structure, and dielectric behavior. Additionally, the chapter addresses the limitations associated with the sol-gel method in synthesizing CAO, offering critical insights into the challenges and constraints encountered during the fabrication process.

Chapter 4

Deposition of $CuAlO_2$ by digitally processed DC sputtering

Through meticulous experimentation and analysis, this chapter aims to elucidate the intricacies of depositing $CuAlO_2$ using digitally processed DC sputtering (DPDS), providing a comprehensive understanding of the synthesis process and offering insights into achieving optimal results.

4.1 Previous works on the crystal growth of CAO

Ievtushenko et al. [93] investigate the influence of substrate temperature on the properties of Cu – Al – O films deposited using the reactive ion beam sputtering method. The study covers temperatures ranging from 80 to 380 °C in 50 °C increments. The results show that an increase in substrate temperature leads to the formation of the $CuAlO_2$ phase. Moreover, the Al/Cu stoichiometric ratio decreased with increasing substrate temperature, leading to the formation of the $CuAlO_2$ phase.

CuAlO thin films were deposited on (0001) sapphire substrates using an Al-Cu metallic target by Hsieh [94] using RF sputtering. The films were annealed at various temperatures (600, 800, and 1000 °C) in a nitrogen atmosphere. The results revealed that the as-deposited films were amorphous, and annealing at 600 °C led to the crystallization of CuO. At 800 °C, the films exhibited a crystallized $CuAlO_2$ phase with a preferred (00l) growth orientation, and at 1000 °C, the crystallization decreased with the growth of (012) and (018) planes. They noticed that samples' crystallinities have a reversed effect with the Al contents, i.e., the increments in Al contents lead to a decrement in a crystalline structure. It is proposed that the increasing Al contents distort the lattice while occupying the Cu site. (00l) plane might

be the lowest energy surface where CuAlO is preferentially rearranged. The increasing Al contents distort film crystalline with more structural defects that trap hole concentration and decrease electrical conductivity.

Liu et al.[95] deposited CuAlO film by RF reactive magnetron sputtering on n-Si wafers while using $Cu_{0.42}Al_{0.58}$ alloy target at different substrate temperatures. They noticed an amorphous phase, sharp as well as intense crystalline peaks and broadening peaks at 800 °C, 870 - 940 °C, and 1000 °C, respectively. In such materials, phase transition can easily occur, leading to highly crystalline formation at a narrow temperature range. For p-$CuAlO_2$, interstitial oxygen and copper vacancies are responsible for hole conductivity. The conductions were found to be dependent on the improvement in film crystallinity and phase purity.

N. Tsuboi et al. [96] employed a dc-reactive sputtering method, utilizing Cu and Al elemental targets with Ar-diluted oxygen gas, and prepared $CuAlO_2$ films (see Figure **??**). By controlling the deposition parameters, such as Cu and Al deposition periods and post-annealing temperatures, they achieved stoichiometric $CuAlO_2$ films through post-annealing at temperatures exceeding 700 in a nitrogen atmosphere. The $\frac{Cu}{Al}$ ratio in the as-deposited films decreased with increasing Al deposition periods (t_{Al}). Oxygen molar fraction decreased with post-annealing at temperatures higher than 700, approaching 0.5.

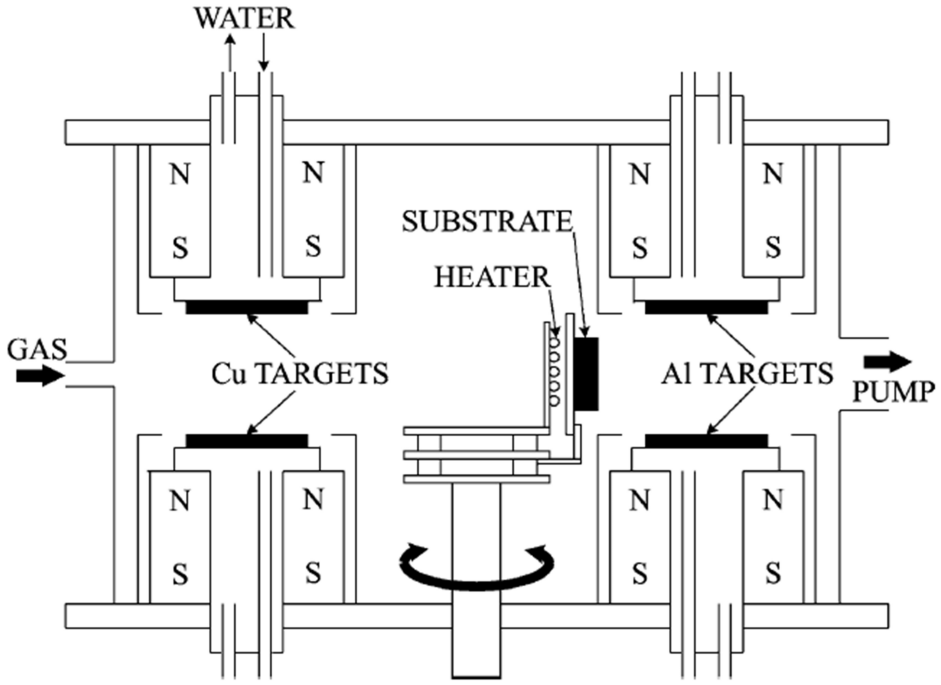

Fig. 4.1 Schematic representation of the dc-reactive sputtering system with two pairs of the facing Cu and Al elemental targets. [96].

An N-doped $CuAlO_2$ film was grown by Pan et al.,[97] on a quartz substrate by RF magnetron sputtering technique using a ceramic target. In the XRD pattern, they examined [001], which is the preferential orientation for the N-doped $CuAlO_2$ crystal growth. The optical transparency improved slightly with N doping. Along with Cu vacancy interstitial oxygen, the acceptor impurity N also contributes to the conductivity of thin film. The N-doped film showed one order more conductivity than the undoped film. Moreover, it was noted that with the excess N concentration in the interstitial site (i.e., more than 15%), the mobility declined due to the carriers' scattering effect.

By Al-Cu mosaic target, Hsieh et al., [98] grew Cu-Al-O films on a glass substrate by the RF sputtering method. The oxygen partial pressure (Opp) was fixed at 10 %, and the dependency of thin film behaviors on varying substrate temperatures and RF power was investigated. The film growth rate was found to be proportional to RF power. Higher RF power provides more argon ions favorable for higher bombardment on the target materials, leading to a rise in the growth rate. Structural analysis was made on varying RF power. For RF power < 100 W, the deposited film showed an amorphous nature, having insufficient energy to gain an ordered fashion. The formation of $CuAlO_2$ and $CuAl_2O_4$ crystallized was detected for RF power 100 W to 200 W. $CuAlO_2$ (110) plane was clearly observed for RF power > 200 W. However, the $CuAlO_2$ peaks disappeared for RF power of 300 W due to greater surface damage by the bombardment of energetic particles and a faster growth rate, which led to the formation of the CuO phase.

Luo et al. [99] used the RF magnetron sputtering technique to deposit $CuAlO_2$ on a glass substrate. The XRD analysis confirmed the crystalline nature of the $CuAlO_2$ films, and no significant changes in the XRD spectra were observed for the different growth conditions. The Au electrode was deposited on $CuAlO_2$ by shadow masking, and electrical measurements were performed. The decrement in Cu/Al and increment in O/Al improved hole concentration, revealing the enhancement of hole concentration due to the increments of acceptors (i.e., VCu and Oi). Oi has a deep-level defect, so it does not contribute to $CuAlO_2$'s conductivity, while VCu is the origin of p-type conductivity. The increments in oxygen content increased the Oi formation probability; as a result, the formation probability of VCu was also maximized. Hence, Oi directly relates to VCu, enhancing the conduction mechanism in $CuAlO_2$ thin film.

Under the RF magnetron sputtering technique, Yongjian [100], CuAlO is deposited on quartz and silicon (100). XRD revealed that as-deposited CAO has an amorphous nature while film annealed under air ambiance possessed CuO phase. However, the CAO phase was dominant for film annealed in argon ambiance. The hall measurement has confirmed the p-type electrical nature. With the changing of annealing mood from air ambiance to argon,

the increment in the hall mobility as well as carrier concentration of the film was ascribed to the improvement in grain boundary and crystallization.

YJ Zhang [101] synthesized CuAlO thin film on Si and quartz substrates via an RF magnetron sputtering system. XRD revealed the amorphous nature of the as-deposited film deposited at room temperature and the crystalline nature of the annealed one. Irrespective of the annealing temperature, the film possessed stable p-type conduction, which was examined by hall measurement. The samples were transformed from amorphous to crystalline for the annealing temperature of 700 to 900 °C. This transformation causes the reduction of Cu vacancy, which leads to a decrease in the carrier concentration with the sample. At the same time, the formation of crystalline structures reduced the scattering as well as trapping of carriers, so hall mobility was enhanced. However, for the further increment in annealing temperatures to 1000 °C, the appearance of micro cracks and formation of impurities due to phase transformation caused a decrease in mobility and increments in resistivity of the grown thin film.

The study by Yongjian Zhang et al. [102] investigated the preparation of Cu – Al – O films using the radio frequency (RF) magnetron sputtering method on silicon (100) and quartz substrates with a copper and aluminum composite target. The deposition rate (RD) of the film increased with increasing $r_{\mathrm{Cu/Al}}$. Higher sputtering yield of Cu as compared to Al enhanced deposition rate ($1.13\,\mathrm{nm}\cdot\mathrm{min}^{-1}$ to $1.46\,\mathrm{nm}\cdot\mathrm{min}^{-1}$) for increasing $r_{\mathrm{Cu/Al}}$ from 20% to 50%. Moreover, a sputtered Cu atom possesses more energy than Al, making it favorable for defect formation. XRD analysis revealed that $r_{\mathrm{Cu/Al}}$ plays a significant role in the preferred growth orientation of $CuAlO_2$. For $r_{\mathrm{Cu/Al}}$ of 20%, the XRD peaks have an intense nature of (104), (015), and low intensity (018) corresponding to $CuAlO_2$. It was examined for $r_{\mathrm{Cu/Al}}$ of 45% (018), and the peak became significantly intense, suggesting the preferred orientation along it. However, for $r_{\mathrm{Cu/Al}}$ of 55%, the preferred direction shifted from (018) to (104).

While using aluminum and copper targets, Yongjian Zhang, [103], a Cu-Al-O film was grown on Si and quartz substrate by RF magnetron sputtering. The total pressure was set fixed, and then P_{o} increased to establish a relation between R_{D} and P_{o}. The film deposition rate (R_{D}) exhibited an inverse relation with increasing oxygen partial pressure (P_{o}) due to the reduction of sputtering gas (Ar). Moreover, in an oxygen-excessed system, the formation of an oxidation layer resists further sputtering. With increasing P_{o}, increments in the number of atoms in the deposition chamber increased, leading to more plasma collisions and blockage of sputtering atoms; hence, R_{D} decreased. $R_{\mathrm{D}} = 1.9\,\mathrm{nm\ min}^{-1}, 0.7\,\mathrm{nm\ min}^{-1}$ for $P_{\mathrm{o}} = 2.4\times10^{-4}, 1.7\times10^{-3}$ respectively, was recorded. In the SEM result, it was observed that there were large grains for small P_{o}, and increasing P_{o} samples depicted uniform and well-defined grain boundaries.

Blažek [104] deposited CAO on Si (100) substrates by the dual magnetron reactive sputtering method. The elemental composition was reported to depend on the length of –ive voltage pulse at the Al/Cu target. It is observed that Cu contents in the film were increasing, and Al contents were decreasing with the increasing –ive voltage pulse. Adding Cu in the Al_2O_3 enhanced hardness and resistance to cracking of film; however, it reduced the transparency. It was opaque for the film composition of more than 16 % atomic ratio of Cu. The researchers revealed that CAO's structural, optical, and mechanical properties could be controlled while changing the amount of Cu added to Al_2O_3 film.

Hsieh et al., [105] via RF magnetron sputtering technique using a pure copper target and a mosaic target deposited CAO film on a Corning 1737 substrate. In this research work, they studied the effect made on conductivity and transparency with the Al content of CAO. For the Al contents of 0%, a CuO crystal structure may be developed. With the addition of Al contents, the peak shifted toward a higher angle and then disappeared. The reason for peak shifting and the transformation of the crystalline structure to the amorphous phase was due to the substitution of Al^{3+} (0.53 Å) ions with Cu^{2+} (0.73 Å). The smaller Al size makes peak shifting and further substitution of Al to Cu, making lattice distortion and decreasing the crystalline nature. For the CAO film, it was observed that the carrier concentration decreased while resistivity and the optical band gap increased for increasing Al contents in the film.

Chen [106] deposited Cu-Al-O films on a p-type silicon substrate via magnetron sputtering. The amorphous nature of the as-sample transformed to the crystalline phase when it was annealed at 800 °C.

In the discussion above, the deposition of CAO thin film typically involved either DC/RF reactive sputtering or co-sputtering techniques. However, the current research first time employs an LBL approach coupled with saturation oxidation and sputter interruption to achieve a highly ordered stacking growth of the CAO layer by layer. Importantly, non-radical oxidation is prioritized to minimize surface damage, which distinguishes our approach from conventional sputtering methods.

4.2 Background in choosing digitally processed DC sputtering (DPDS)

Wide-band-gap metal oxides (MOs) with high mobility and reliable optical transparency are increasingly in demand for large-area electronic and optoelectronic devices. Among these MOs, n-type materials are prevalent in commercial applications, surpassing their p-type counterparts. This research focuses on $CuAlO_2$ (CAO) due to its p-type nature and potential

as a transparent conductive oxide (TCO) material. CAO consists of AlO_6 octahedra forming a basal layer with alternating stacking layers of the O – Cu – O dumbbell structure along the *c* direction. However, CAO typically exhibits a polycrystalline nature, which poses challenges in achieving high-quality films and optimal Cu-O-Cu lattice connectivity, consequently leading to low field-effect mobility [26].

To address these issues, a layer-by-layer (LBL) deposition approach is proposed, enabling the *c*-direction stacking of CuO and AlO layers, with a focus on the *d*-spacing of CAO. Recently, digitally processed DC sputtering (DPDS) has emerged as an atomically precise deposition method, as reported in previous studies [46], [47]. This study utilizes the DPDS-conducted LBL approach for CAO thin film growth for the first time.

The LBL approach enables precise control of the growth process, leading to ordered CuO, AlO stacking, and formation of long-range structural integrity, which is believed to facilitate carrier transport increase. There is no scattering, and it contributes to the improvement of mobility. Moreover, the LBL deposition facilitates better control over the growth process, which minimizes the formation of grain boundaries in CAO and also contributes to higher mobility. The DPDS allows the deposition rate to be 0.57 nm/cycle under the d-spacing of the (002) plane for good CAO crystallinity. In the growth of CAO by DPDS-assisted LBL, non-radical oxidation was prioritized to avoid possible surface damage[47]. In this report, structural analysis and electrical performance of the fabricated CAO p-TFTs have been presented.

4.3 Sample preparation for sputtering

Substrate preparation and cleanliness substantially influence the material properties of ultra-thin films, particularly those spanning only a few nanometers. The substrate's freedom from hydrocarbons and other adsorbed species is imperative, as these can impede the deposited film by influencing its morphology or introducing impurities.

In this study, p-type Si (100) wafer substrates were used for the deposition of CAO thin film. Initial processing involved cutting Si wafers into 1 cm by 1 cm samples utilizing a diamond cutter. Subsequently, these samples underwent a thorough ultrasonic cleaning regimen. First, they were immersed in an acetone bath for 10 minutes, ensuring the removal of any contaminants. Following this, the samples underwent an additional ultrasonic cleaning step, this time in a methanol bath for 10 minutes. To conclude the preparatory steps, the cleaned samples were dried using nitrogen (N_2) gas before their introduction into the vacuum chamber for the deposition process. The detailed procedural steps are visually represented in the schematic provided in Fig.4.2, elucidating the sequential stages of sample preparation.

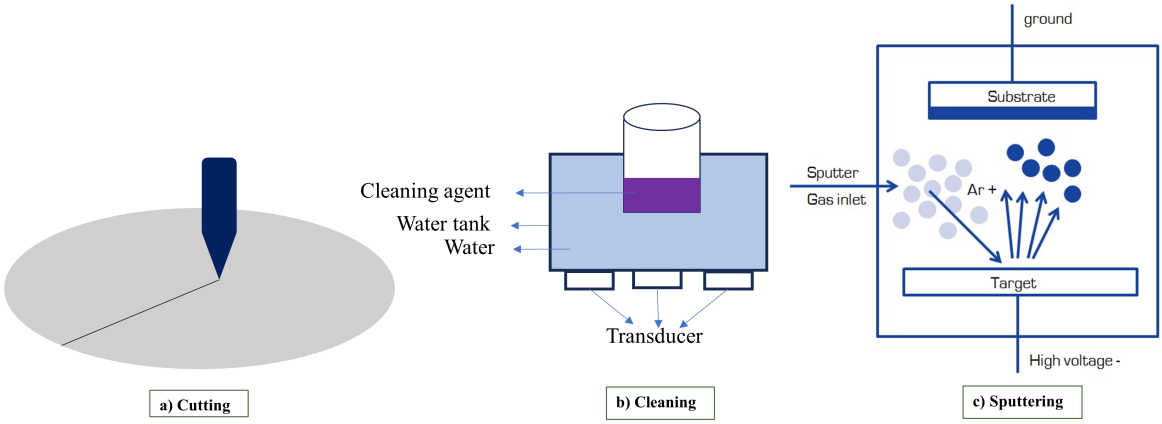

Fig. 4.2 Schematic of Si-substrate preparation for sputtering.

This comprehensive substrate treatment ensures the removal of unwanted residues on the surface for the subsequent deposition of films. The utilization of ultrasonic cleaning in both acetone and methanol baths enhances the efficacy of contaminant removal, addressing the necessity for a meticulously cleaned substrate in the fabrication of ultrathin films.

In this work, deposition was performed by the DPDS system (SHINCRON CO., LTD. P-RAS), which utilizes a digital pattern generator (DPG) for pulsed-DC sputtering. The DPDS system consists of two cathodes attached with a high-voltage switch (HV-SW) for each and one DC power supply. Each cathode is directly driven through HV-SW by the DPG to generate pulsed plasma independently, which allows sputtering of the selected metal target and sputtering pauses[46]. On the other hand, oxygen is supplied by generating a valve open/close pulse in synchronization with the sputtering interruption to achieve saturation adsorption/oxidation after deposition of the metal atomic layer [47]. The deposition was performed on Si (100) substrates utilizing Cu and Al metallic targets of 2 inches diameter under a layer-by-layer (LBL) approach.

4.4 Deposition parameter optimization

4.4.1 Plasma stability optimization for CAO growth under DPDS

Using the LBL approach, ensuring plasma stability is necessary for achieving uniform and high-quality thin films. In our study, we meticulously assessed plasma stability at both Cu and Al targets across varying voltage settings, spanning from 270V to 500V. Our observations unveiled distinct behaviors at different voltage levels. At lower voltages, specifically in the range of 270V to 300V, maintaining plasma stability proved challenging at the Cu target, resulting in spontaneous sparking. However, with voltages over 300V to 500V, we

achieved optimal plasma stability for the Cu target. Conversely, for the Al target, stability was compromised beyond 370V, with the estimated range of stable plasma lying between 340V and 370V. Given that in our DPDS, we utilize a single power supply for both metallic targets, a strategic voltage optimization was essential. After careful consideration, we found that setting the voltage at 350V for both targets yielded the best results in the growth of CAO thin films. This voltage setting ensured a stable plasma environment for both the Cu and Al metallic targets, facilitating uniform and high-quality thin film deposition.

4.4.2 Deposition rate (Rd) for each metallic target

The layer-by-layer deposition technique plays a pivotal role in the fabrication of crystalline films, necessitating precise control over deposition rates for optimal film quality. Sputtering times at both targets were set to 1 sec, oxygen supply times were also set to 1 sec, and purge time was set to 3 sec. The deposition rates were then determined under these conditions separately for each target in the O_2 environment. Under such deposition conditions, the Rd of Cu was estimated to be 0.0222 nm/sec or 0.11111 nm/cycle, while the Rd of Al was 0.01555 nm/sec or 0.07777 nm/cycle as shown in Fig. 4.3 (a, b).

4.4.3 Film transparency with increasing oxygen supply

In the deposition process under the specified sputtering conditions, a glass slab was affixed to the substrate to assess the transparency of the resulting films. Notably, films grown under an oxygen flow rate of 13 sccm, specifically a purge time of 3 sec, exhibited superior transparency, as shown in Fig. 4.3(c).

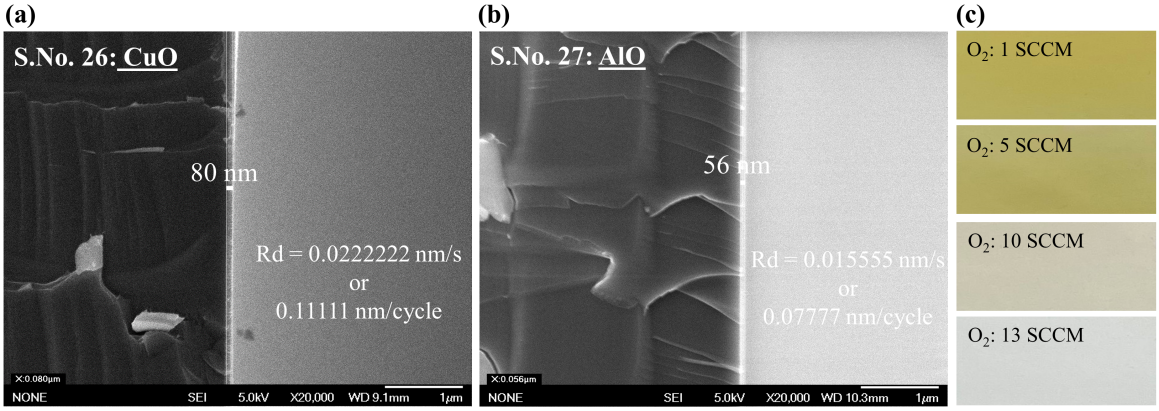

Fig. 4.3 Deposition rate of a) CuO, b) AlO, and c) variation in the oxygen supply Vs. glass slab transparency.

4.4.4 Overview of sequence design

In our investigation, we observed that Cu exhibits a deposition rate approximately three times higher than that of Al as a metallic target. Consequently, to achieve Cu/Al stoichiometric deposition, we set the Cu sputtering time to 1.9 seconds and the Al sputtering time to 6 seconds. Considering the voltage stability range of 340 to 370 for both targets, we established the voltage settings for both Cu and Al targets at 350 V. This voltage configuration ensures consistent plasma stability, critical for uniform and high-quality film deposition. For achieving saturation oxidation, an oxygen introducing time of 1 second coupled with a purge time of 3 seconds proved sufficient. Therefore, we set the oxygen introducing time to 1 second, followed by a purge time of 3 seconds, optimizing the oxidation process for the desired film properties.

4.5 Optimization of DPDS conditions for the LBL growth

The sputtering process employed 2-inch diameter Cu and Al metal targets, utilizing Si(100) and SiO_2/Si as substrates. Each metal target underwent independent pulsed-DC plasma generation by DPDS in an Ar atmosphere. The process was conducted without substrate heating, at a pressure of 5 Pa, with an Ar flow rate of 50 SCCM, and a pulsed oxygen supply of 13 SCCM during sputtering interruptions. Consequently, the LBL deposition of CAO can be achieved using DPDS.

The DPDS system utilizes a DC power supply with three operation modes: constant voltage (C_v), constant current (C_c), and constant power (C_p). These modes allow the limitation of operation voltage, current, and power, respectively. To ensure stable ignitions for frequent plasma generation on each target, the voltage limit was set to 350 V in C_v mode, and the current limit was set to 0.25 A in C_c mode. Figure 4.4(b) shows the voltage and current responses of the DC power supply output during the LBL deposition process exhibited a sharp overshoot in current ($I_{overshoot}$) at the rising edge of the current pulse, likely due to micro-arcing at the Al metal target, which was subsequently limited by the C_c mode. Clear transitions between metal sputtering and oxygen supply during sputtering interruptions were readily discernible.

To manage fluctuations in plasma impedance, the deposition rate was controlled under C_p mode, with Al sputtering conducted at 70 W in this mode. Conversely, Cu sputtering was performed in C_v mode due to the higher plasma impedance, with an average power of approximately 60 W. Continuous monitoring of the precise responses of voltage and current pulses throughout the sputtering process indicated the establishment of a reliable layer-by-layer deposition process. The sputtering conditions are detailed in Table 4.1.

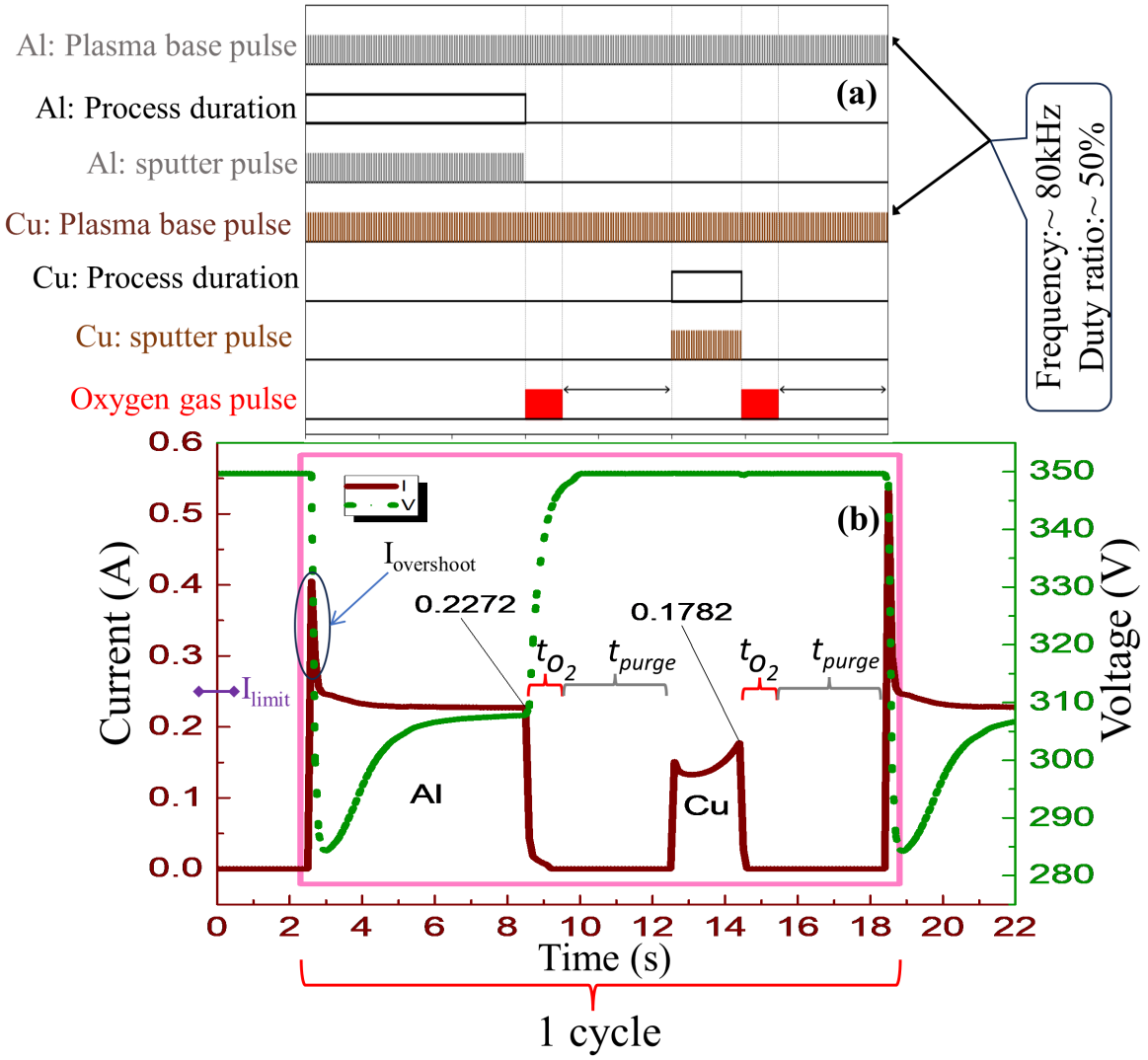

Fig. 4.4 (a) Schematics of digital processing for LBL sputtering of CAO (b) Pulse voltage and plasma current during the sputtering process.

Table 4.1 Experimental Parameters and Quantities

Parameters	Quantities	Parameters	Quantities
DC power supply [W]	70	Voltage [V]	350
Current [A]	1	Sub. rot [rpm]	10
Cu sputtering time [sec]	1.9	Al sputtering time [sec]	6
Oxygen introducing time [sec]	2	Cycle length [sec]	15.9

4.5.1 Deposition rate of 0.57nm/cycle under (002) plane of CAO

The deposition rate plays a crucial role in the LBL approach, particularly in the context of fabricating materials with specific structural characteristics. In our study, we specifically chose the c-axis coordination of CAO to advance our LBL approach. The atomic arrangement indicates the Cu-O-Al-O stacked structure along the c-axis with the unit cell height of 1.14 nm, as shown in Fig.4.5(b). The LBL deposition of CAO was performed along the c-axis, a sequential Cu-O-Al-O deposition as one cycle. The repetition of CAO stacking in a unit cell is twice; hence, the deposition was desirable to half the height, i.e., 0.57 nm. In such a context, the deposition rate was set to 0.57 nm/cycle, corresponding to the d-spacing of (002) in CAO.

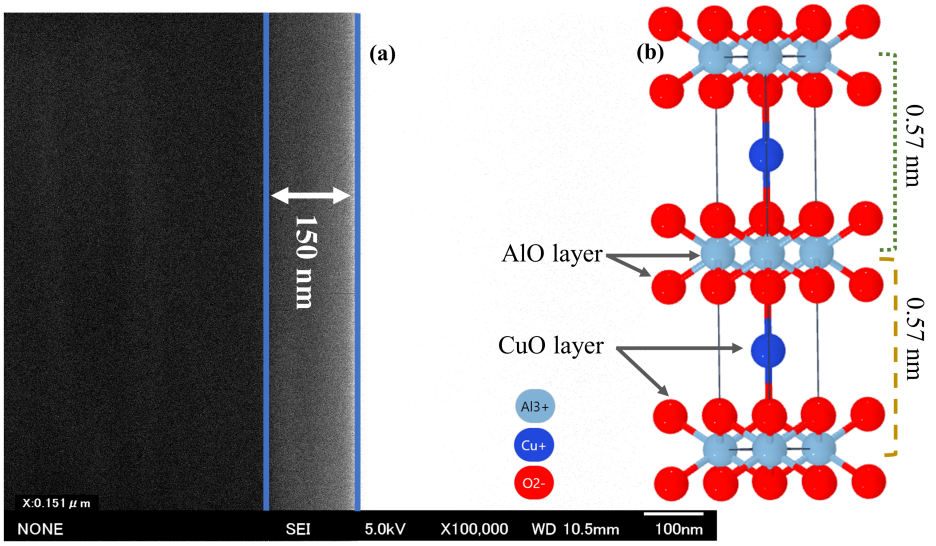

Fig. 4.5 FESEM image of (a)150 nm CAO thin film and (b) CAO (Hexagonal structure) unit cell.

To control the deposition rate and tailor the composition precisely, we systematically altered the pulsed sputtering time for each target, as illustrated in Fig. 4.4 (a). The experimental data aligns with our expectations. The calculated deposition rate, derived from FESEM

results shown in Fig. 4.5 is determined to be 0.57 nm per cycle—falling within the desired range.

4.5.2 Stoichiometry optimization

The elemental composition of the deposited films was further elucidated through electron probe micro-analysis (EPMA) as shown in Fig.4.6. Remarkably, the Al to Cu ratio demonstrated reasonable agreement with the stoichiometric ratio for CAO, underscoring the effectiveness of our controlled deposition parameters. The DPDS conditions were determined

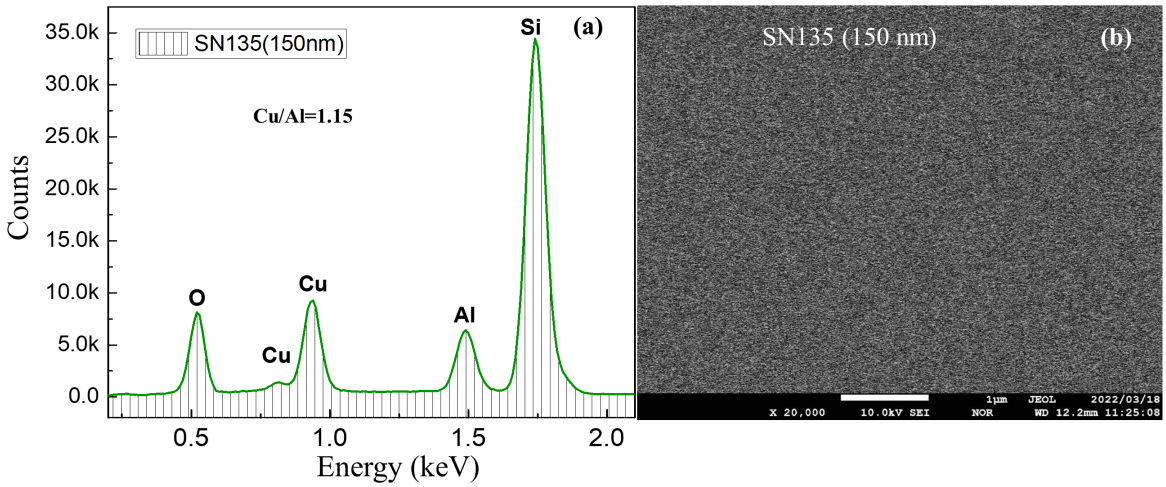

Fig. 4.6 EPMA and SEM images of 150 nm CAO thin film.

to achieve the LBL process precisely tailored to the requisite metal composition through measurements conducted using an EPMA.

4.5.3 Crystallinity evaluation

In investigating the crystalline and amorphous nature of the synthesized samples, XRD using $CuK\alpha_1$ was employed. This analysis provided valuable insights into the structural characteristics of the deposited films, shedding light on the material's phase composition and crystallinity. The LBL-deposited CAO films were annealed in air at different temperature ranges up to 1000 °C, as shown in Fig.4.7. This annealing process effectively enhanced the chemical and physical stability of the CAO samples [107, 108]. From the XRD graph, it is evident that no discernible peaks were observed in both films annealed below 500 °C. However, in the CAO, for post-annealing temperatures exceeding 600 °C, several peaks emerged. Specifically, at 35.8°, peaks indicative of the presence of CuO were observed in the

film annealed at 600 °C. Subsequently, with further increments in annealing temperatures beyond 800 °C, distinct peaks corresponding to CAO became noticeable.

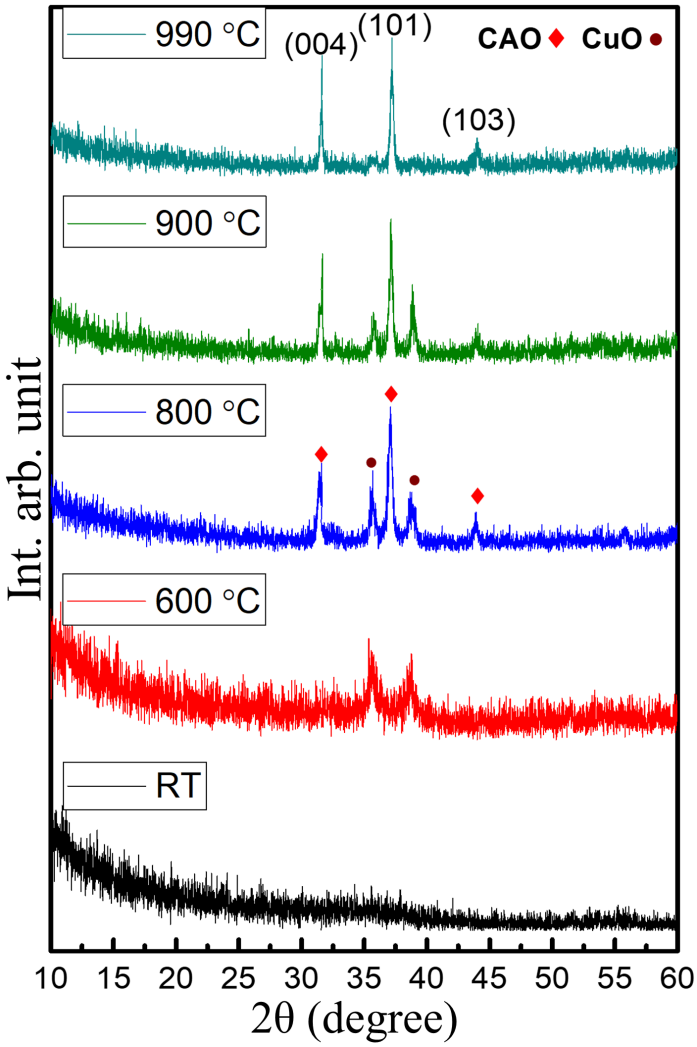

Fig. 4.7 XRD patterns; 150nm thin film of CAO annealed at different temperatures.

The diffraction peaks at 2Θ values of 31.28° and 36.89°, corresponding to the crystallographic planes (004) and (102), respectively, are attributed to CAO. As the annealing temperature increased, the number of peaks decreased, suggesting a phase conversion towards CAO. The observed changes in peak positions and intensities signify the influence of annealing conditions on the crystallographic properties, revealing a nuanced interplay between temperature and film structure. The increased energy absorption at higher temperatures contributes to the enhancement in crystalline nature, particularly at elevated temperatures [26]. Notably, the peaks of CAO (004) become more prominent in the XRD pattern at higher temperatures, indicating a preferred growth orientation along the (004) direction. The XRD

results affirm the hexagonal crystal structure for CAO in the space group P63/MMC. The calculated crystalline parameters are mentioned in the Table 4.2.

Table 4.2 Crystalline parameters extracted from XRD plots of the 150nm CAO thin films annealed at 990 °C

Pos. 2theta (°)	FWHM	d-spacing	Crystallite size
150 nm			
31.2825	0.0866	2.85942	421
36.8973	0.3464	2.43617	306
45.0283	0.5196	2.01336	183

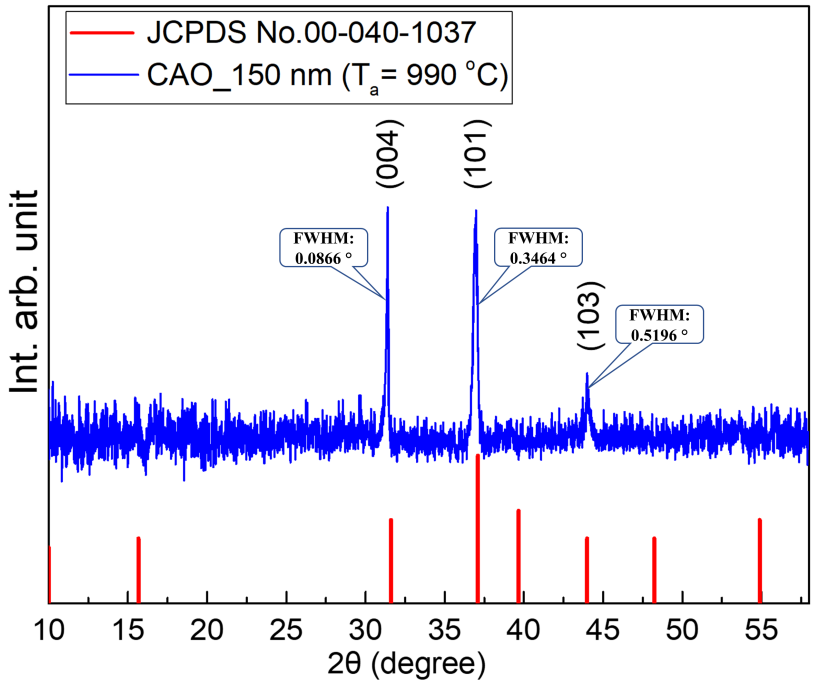

Fig. 4.8 XRD patterns of 150 nm CAO film annealed at 990 °C comparing with JCPDS reference.

Comparing the XRD pattern of the 150 nm CAO film annealed at 990 °C with JCPDS No.00-040-1037, the hexagonal structure of CAO with space group $P6_3/mmc$ can be confirmed as shown in Fig. 4.8. However, the diffraction peaks that appear are limited to those c-axis oriented (004) and tilted from the c-axis (101) and (103). Moreover, the peak intensity ratio is changed compared to the powder diffraction, and the (004) diffraction peak becomes stronger. Here, the FWHM of (004), (101), and (103) are 0.0866°, 0.3464°, and 0.5196°, respectively.

Fig. 4.9 shows rocking curves for the diffraction peaks of (004) and (101) to gain insights into the c-axis crystallization of the 150 nm CAO film annealed at 990 °C. Remarkably, the (004) diffraction rocking curve showed a sharp peak with an FWHM of 0.057° overlapping on a constant background. In contrast, no such peak was detected for the (101) diffraction. The sharp peak on the (004) diffraction rocking curve indicates high orientation to the c-axis of CAO. We have speculated that there are two pathways for forming the CAO crystalline phase: phase transition from the CuO phase and direct formation from the LBL-deposited lattice. The former shows randomly oriented diffraction, such as the (101) diffraction and the constant background of (004) rocking curves. On the other hand, the latter exhibits a fine peak in the (004) rocking curve due to the c-axis-oriented LBL deposition. The smaller FWHM and the formation of the XRD rocking peak indicate the preferred orientation of CAO along the (004) direction.

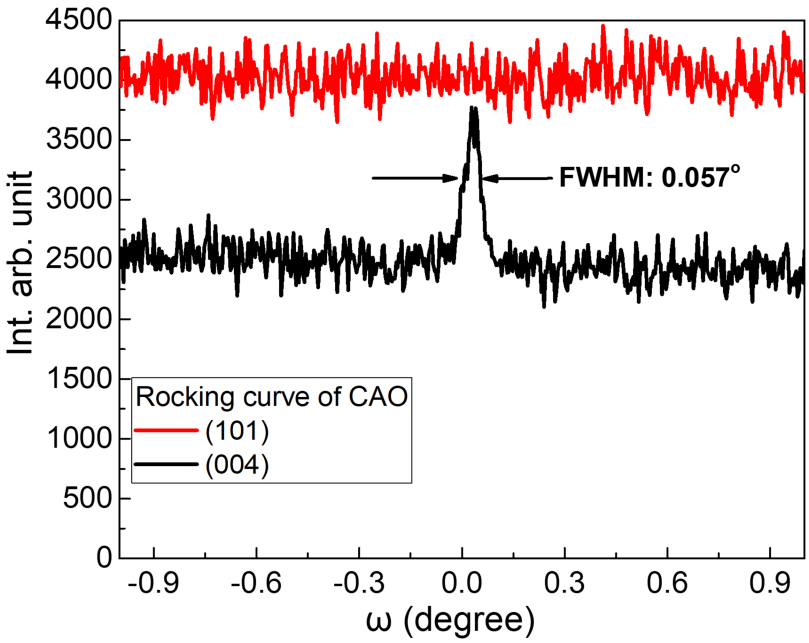

Fig. 4.9 150 nm CAO film annealed at 990 °C; XRD ω-rocking curve scan of CAO (004) and (101) planes

Therefore, the prominent background signal observed in the rocking curve X-ray diffraction indicates the coexistence of randomly and highly oriented crystalline planes at this elevated temperature.

4.5.4 Morphological analysis of the 150 nm CAO thin films

The surface morphologies of the CAO thin films were examined using scanning electron microscopy (SEM), as illustrated in Fig. 4.10. The as-deposited CAO thin film exhibited an initial grain size of approximately 40 nm. Subsequent annealing of the samples at 990°C facilitated the coalescence of smaller grains, forming larger grains with an increased size of about 150 nm. The augmentation in grain size is attributed to thermally activated processes such as grain growth and recrystallization during the annealing treatment [109]. The reduction in the trapping sites of the grain boundaries is beneficial to the charge transport that helps to improve the mobility of the annealed CAO thin films [110].

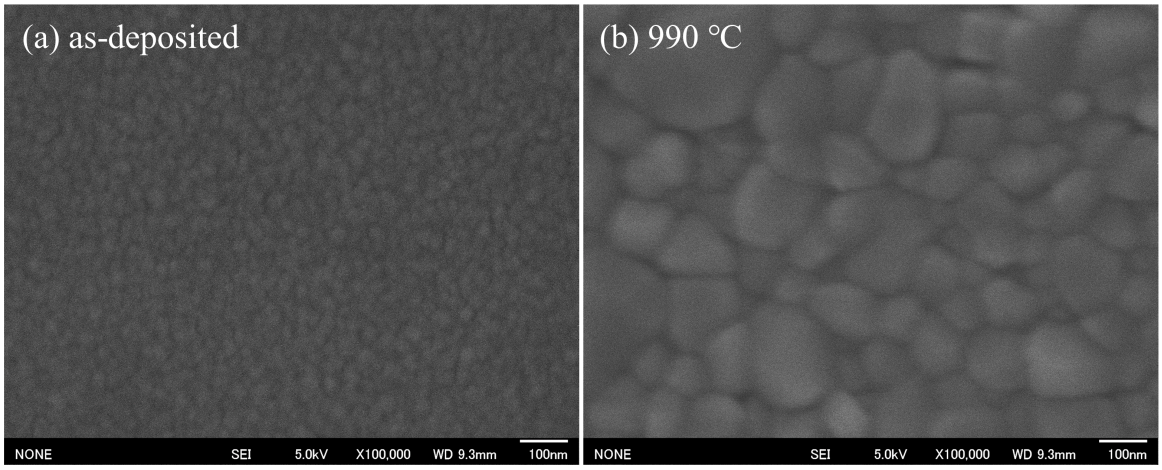

Fig. 4.10 FESEM images for the 150 nm CAO a) as-deposited thin film, b) annealed thin film at 990 °C.

4.5.5 Stoichiometry of the 150 nm CAO films at different thickness and temperatures

The confirmation of $CuAlO_2$ stoichiometry in the CAO films deposited on Si by DPDS was examined through an EPMA, wherein the Cu/Al ratio approached unity, confirming the targeted stoichiometric composition of the films. Furthermore, the utilization of a LBL approach was instrumental in maintaining homogeneity throughout the film thickness. Figure 4.11 (a) illustrates the effectiveness of this method in preserving the desired stoichiometry, affirming the precision achieved through the deposition process.

Concerning the impact of annealing on stoichiometry, EPMA analysis was extended to include samples subjected to varying annealing temperatures. In Fig. 4.11 (b), it is evident that the Cu/Al ratio remained almost the same despite changes in annealing conditions. In

addition, there is no significant decrease in the oxygen molar fraction caused by the annealing. This observation suggests that the annealing temperature (600 °C–990 °C) did not adversely affect the stoichiometry of the CAO films.

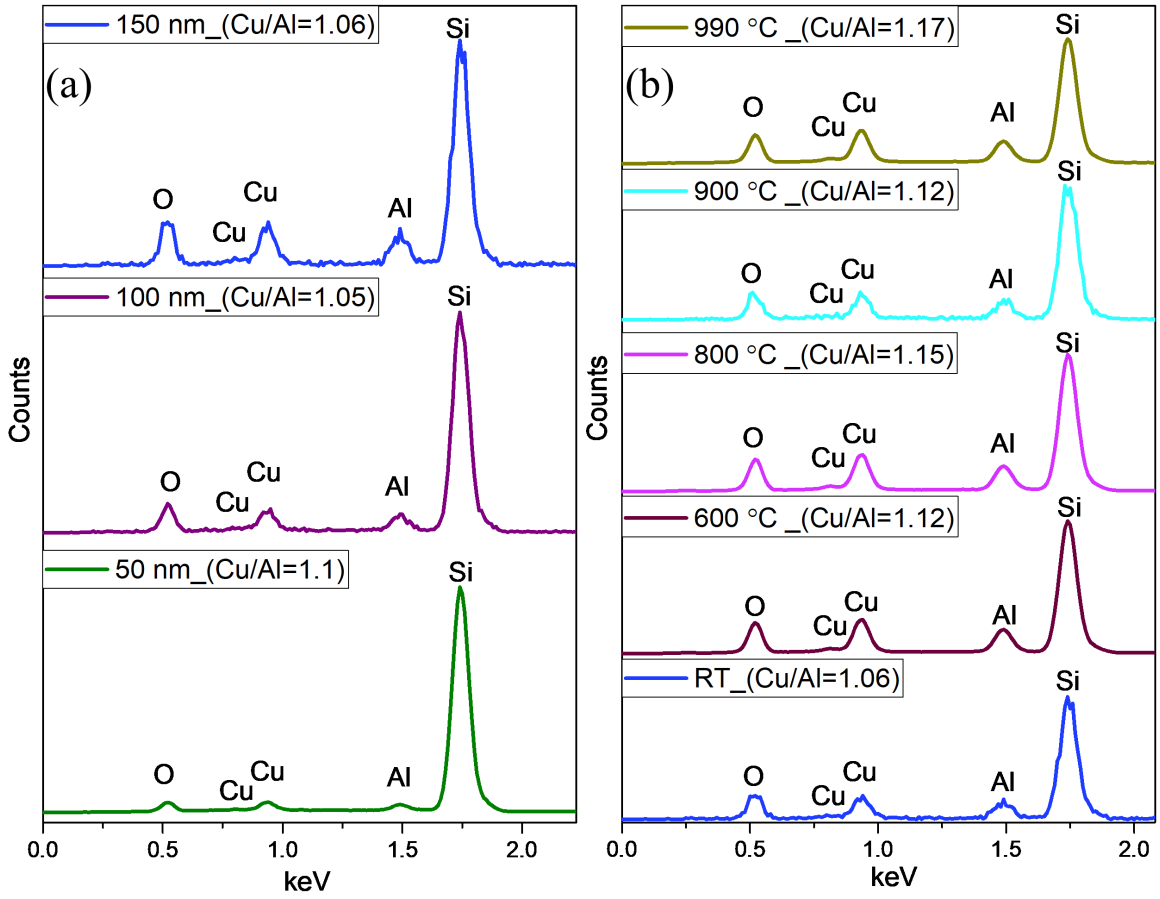

Fig. 4.11 EPMA spectrum illustrating the CAO thin film under a) different film thicknesses and b) varying annealing temperatures.

4.6 Summary of Chapter 4

Chapter 4 focuses on the deposition of CAO using digitally processed DC sputtering (DPDS), detailing the optimization of deposition parameters and presenting the results obtained. The chapter begins with a review of previous works on CAO crystal growth via sputtering. It then delves into the rationale behind choosing DPDS and describes the sample preparation process for sputtering. Subsequent sections discuss the optimization of deposition parameters. Further optimization is explored for the Layer-by-Layer (LBL) growth technique, covering aspects such as deposition rate, stoichiometry, crystallinity evaluation, and morphological analysis of

the CAO thin films. The chapter concludes with an examination of the stoichiometry of the CAO films at different thicknesses and temperatures, providing a comprehensive overview of the deposition process and its outcomes.

Chapter 5

Fabrication and characterization of p-type $CuAlO_2$ TFT

Chapter 5 delves with an in-depth exploration of the fabrication process of CAO p-TFT devices. This includes the deposition of the $CuAlO_2$ thin films and the patterning of electrodes. Subsequently, the chapter consists of the characterization of these fabricated TFTs.

5.1 Fabrication of CAO TFTs

The thin-film transistor (TFT) architecture integrates active channels, electrodes, and dielectric layers. In this study, highly oriented $CuAlO_2$ (CAO) was deposited for a bottom-gate, top-contact TFT configuration on a SiO_2/Si substrate using a shadow masking technique for precise patterning. Initially, a 200 nm SiO_2 layer was meticulously deposited on a p-Si substrate. Subsequently, a precisely positioned shadow mask facilitated controlled growth of the CAO channel on the SiO_2/Si substrate. Finally, the source (S) and drain (D) electrodes were deposited atop the CAO/SiO_2/Si structure using a thermal evaporator. The shadow masking approach enabled deposition of Al source and drain electrodes on the CAO/SiO_2/Si structure, establishing desired electrical connections. Additionally, a back-gate electrode was formed on the backside of the substrate. Precise patterning and controlled deposition of the layers, facilitated by shadow masking, allowed the fabrication of a bottom-gate, top-contact TFT configuration with a highly oriented CAO active channel. The bottom-gate, top-contact TFT architecture is widely used in thin-film transistor technology. In this configuration, the gate electrode is positioned beneath the active channel layer, while the source and drain electrodes are deposited on top of the channel material. The dielectric layer, SiO_2 in this case, acts as the gate insulator, separating the gate electrode from the active channel. Utilizing

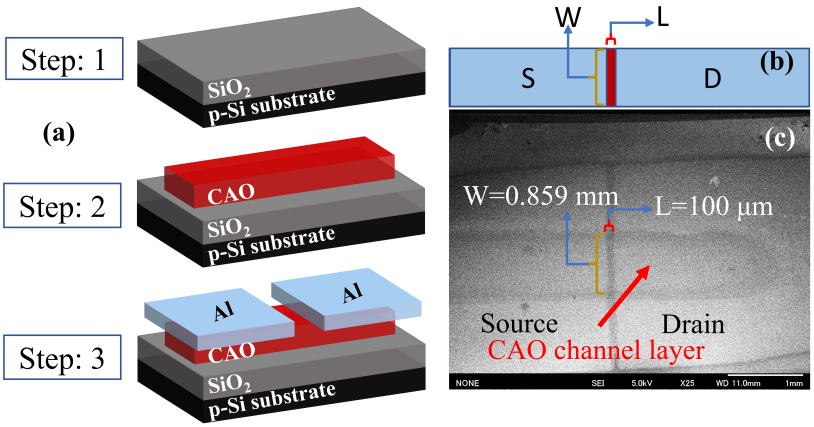

Fig. 5.1 (a) Schematic illustration of the CAO TFT fabrication scheme (b) Schematic of TFT structure (c) FESEM image of CAO TFT.

a shadow mask during deposition ensured precise patterning and controlled growth of the CAO active channel on the SiO_2/Si substrate. This technique involves strategically placing a patterned mask with openings to selectively expose specific substrate regions, allowing material deposition only in desired areas. Furthermore, deposition of Al source and drain electrodes atop the CAO/SiO_2/Si structure, facilitated by shadow masking, established necessary electrical connections for TFT operation. The back-gate electrode, formed on the substrate's backside, completes the bottom-gate configuration, enabling the application of gate voltage to modulate CAO active channel conductivity. This fabrication approach, combining layer-by-layer CAO deposition using DPDS and shadow masking, provided precise control and patterning of components required for bottom-gate, top-contact TFT structure. The schematic of the fabrication steps is illustrated in Fig. (5.1a). The separation between S/D electrodes is termed channel length (L), while the overlapping distance between the electrodes is termed channel width (W), as shown in Fig. (5.1b). The channel dimension of the CAO was investigated by FESEM, where the W and L of CAO channel layers were 0.859 mm and 100 µm, respectively, as shown in Fig. (5.1c). The cross-section of the FESEM image of the fabricated CAO p-TFT is demonstrated in Fig. 5.2, where a 150 nm CAO layer serves as a channel layer and a 200 nm thick SiO_2 is used as the gate dielectric.

5.2 TFT characteristics

The CAO TFT devices were evaluated using two characteristic curves: transfer (I_{ds} vs. V_{gs}) and output (I_{ds} vs. V_{ds}) curves, following conventional methods[29]. I_{ds} and V_{ds} indicate the current and voltage between the drain and source electrodes, respectively, and V_{gs} indicate

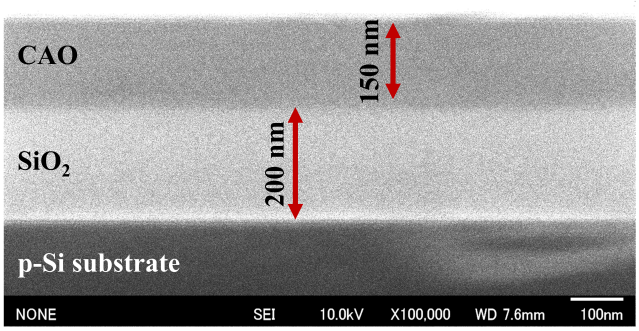

Fig. 5.2 Cross-section of FESEM image obtained from CAO grown on SiO_2/Si substrate.

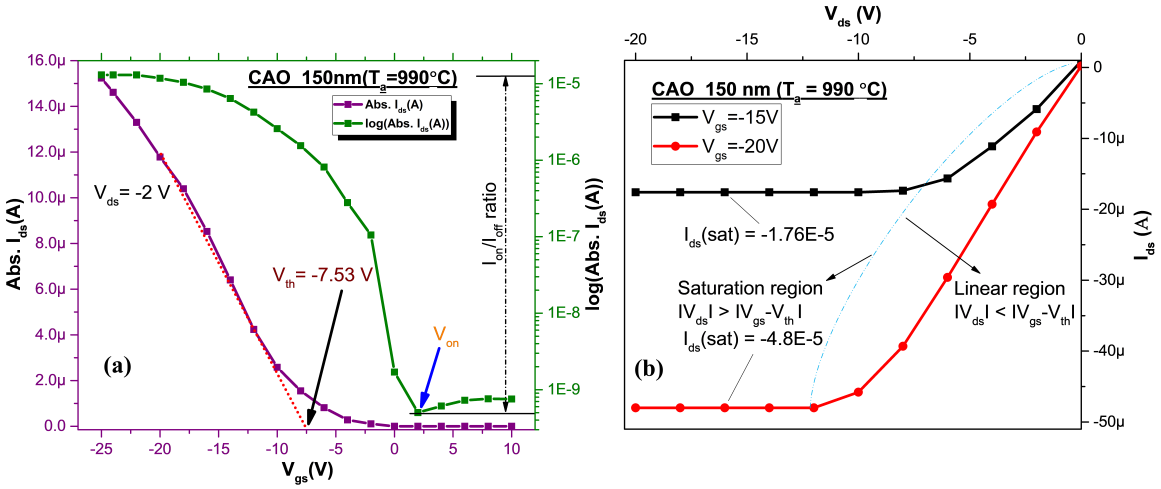

Fig. 5.3 (a) Transfer characteristics (I_{ds} vs. V_{gs}); 150-nm CAO p-type TFT (b) Output characteristics (I_{ds} vs. V_{ds}); 150-nm CAO p-type TFT annealed at 990 °C.

the gate voltage. Keithley electrometers were used for the electrical characterization. The two characteristic curves of the TFT of CAO films annealed at 990 °C and without annealed are shown in Fig. (5.3) and Fig. (5.4), respectively.

Both fabricated CAO TFTs show typical p-type behavior. The transfer curves in Fig. (5.3a) and Fig. (5.4a) indicate full depletion of the CAO channel at V_{gs} = 0 V. Applying a negative bias to V_{gs}, a capacitive injection of holes takes place at the interface of CAO/SiO_2, subsequently modulating the I_{ds} flowing between the source and drain electrodes. Note that the TFT characteristics are observed in the as-deposited sample, as shown in Fig. (5.4), despite the amorphous phase of CAO. The transfer curve for each sample is for $V_{ds} = -2V$, which is in the linear region of the output curve. The CAO TFT's threshold voltage (V_{th}) is an important parameter determined by a horizontal axis intercept of a linear extrapolation of the transfer curve[111],[112]. V_{th} for the highly oriented and as-deposited CAO TFT were -7.53 V and -9.0 V, respectively. In annealing, the thermal energy facilitates the healing of crystal

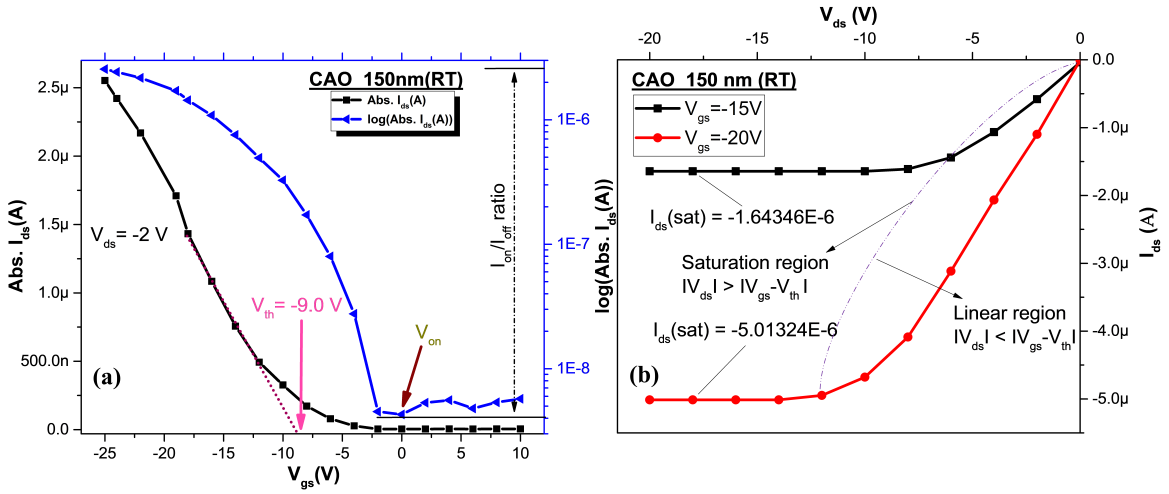

Fig. 5.4 (a) Transfer characteristics (I_{ds} vs. V_{gs}); 150-nm CAO p-type TFT (b) Output characteristics (I_{ds} vs. V_{ds}); 150-nm CAO p-type TFT as-deposited.

defects, which minimizes the hole traps at the CAO/SiO_2 interface [113], consequently reducing the V_{th} in the higher annealing CAO TFT. The transfer characteristics also show an on/off ratio of 3×10^4 for the annealed sample and 6×10^2 for the as-deposited sample, respectively. The device has a width of 859 μm and a channel length of 100 μm, but there is no surface passivation. Therefore, it was speculated that the relatively high off current was due to the leakage current through the grain boundary and surface in such a wide channel. Moreover, the 200 nm thickness of the SiO_2 gate is enough to prevent gate leakage. The charge transfer to the gate should have actually occurred, but the gate current containing the leakage current could not be measured within the gate drive voltage range of the DC measurements. Therefore, we believe that the gate current does not significantly affect the drain current characteristics.

Due to the long channel length, the gradual channel approximation analysis was used to calculate the field-effect mobility of CAO layers from experimentally obtained TFT characteristics [29]. The field-effect mobility μ_{FE} in the linear region can be estimated using differential transfer conductance $\frac{\partial I_{ds}}{\partial V_{gs}}$ following Eq. (5.1).

$$\mu_{FE} = \frac{L}{WC_iV_{ds}} \cdot \frac{\partial I_{ds}}{\partial V_{gs}} \tag{5.1}$$

where L and W are the length and width of the CAO channel layer, and C_i is the areal capacitance of the gate oxide. C_i has been estimated to be 1.73×10^{-8} (F/cm^2) from the thickness and the relative permittivity (ε_r = 3.9) of SiO_2.

On the other hand, the output curves shown in Fig.(5.3b) and Fig.(5.4b) show the saturation of I_{ds} clearly, and the saturated value ($I_{\mathrm{ds}}^{\mathrm{sat}}$) depends on V_{gs}, which are typical transistor characteristics. I_{ds} decreases with V_{ds} and then reaches $I_{\mathrm{ds}}^{\mathrm{sat}}$ at V_{ds} = V_{gs} - V_{th}. The value of $I_{\mathrm{ds}}^{\mathrm{sat}}$ increases with V_{gs} due to the channel carrier generation. $I_{\mathrm{ds}}^{\mathrm{sat}}$ is obtained from the saturation region of the output curve and is expressed by the following Eq. (5.2),

$$I_{\mathrm{ds}}^{\mathrm{sat}} = \frac{1}{2}\frac{W}{L}C_i\mu_{FE}\left(V_{gs} - V_{th}\right)^2 \tag{5.2}$$

The mobility (μ_{FE}) is a measure of how efficiently the majority of carriers move under the influence of an electric field in TSC MOs, typically obtained through field-effect measurements. In ideal TFTs, mobility is assumed constant, unaffected by variations in V_{gs}. However, real TFTs often exhibit mobility changes with both V_{gs} and V_{ds} [17]. Understanding the voltage dependence of mobility is crucial for accurate device characterization. The most accurate estimation of μ_{FE} in the saturation region, particularly at high V_{ds}, accounting for the effect of V_{gs}, is obtained through Eq.5.3, which utilizes the measured saturation region output conductance.

$$\mu_{FE} = \frac{2L}{WC_i} \cdot \left(\frac{d\sqrt{I_{\mathrm{ds}}^{\mathrm{sat}}}}{dV_{gs}}\right)^2 \tag{5.3}$$

Notably, this equation does not require prior knowledge of other parameters like the transistor threshold voltage. By incorporating the effects of V_{gs}, it provides a more comprehensive estimation of mobility under real operating conditions.

Also, the carrier concentration in the channel region exhibits a non-uniform distribution, as it accumulates near the semiconductor-insulator interface when V_{gs} and V_{ds} are applied. Here, the effective conductivity of the CAO channel layer is defined as σ, then $I_{\mathrm{ds}}^{\mathrm{sat}}$ at $V_{ds} = V_{gs} - V_{th}$ can be expressed as,

$$I_{\mathrm{ds}}^{\mathrm{sat}} = \frac{W.t}{L}\sigma\left(V_{gs} - V_{th}\right) \tag{5.4}$$

where t is the CAO thickness. The effective channel conductivity σ was estimated using Eq. (5.4) from the output curves. The extracted TFT properties from the characteristic curves have been tabulated in Table 5.1.

The reported μ_{FE} for the solution-processed CAO TFT after post-annealing is 0.1 [26]) to 1.36 $\mathrm{cm^2V^{-1}s^{-1}}$ [114]. Meanwhile, the CAO TFT synthesized through magnetron sputtering exhibited a field-effect mobility of 0.97 $\mathrm{cm^2V^{-1}s^{-1}}$ [33]. The directed formation of CAO via DPDS-assisted LBL deposition offers a unique advantage by creating an orderly atomic

arrangement with superior electronic characteristics. The controlled and precise deposition process allows for the formation of a well-structured and defect-minimized CAO lattice. This structured lattice arrangement facilitates the efficient transport of charge carriers within the CAO film, which serves as an excellent foundation for TFTs. The well-structured lattice also seems responsible for transistor characteristics in the as-deposited CAO TFT; even in the amorphous phase, it exhibited mobility of $0.50\,\mathrm{cm^2V^{-1}s^{-1}}$, comparable to the solution processing followed by annealing. We expected the directional crystallization by LBL deposition and following thermal annealing. The LBL creates a well-ordered CAO lattice, and the thermal treatment contributes to the further refinement of its crystalline structure and enhances the quality of the CAO film, bringing uniformity to the carrier path and enhancing hole transport[115]. The combined process positively influenced the TFT characteristics of the annealed CAO layer, improving the mobility of $4.1\,\mathrm{cm^2V^{-1}s^{-1}}$. The difference in mobility arising in the linear and in saturation regions is due to a notable contact resistance that a device experiences, contributing significantly to a discernible decrease in the effective V_{ds} [116]. This mobility value is good, but we still believe it is restricted due to the persistence of a fraction of the CAO crystal planes retaining a random orientation. To achieve this coveted complete c-axis orientation of the CAO crystalline planes, further atomically precise control over the annealing conditions should be considered, which is expected to lead to an additional enhancement in mobility.

On the other hand, the conductivity of 0.19×10^{-2} S/cm for the as-deposited and 1.8×10^{-2} S/cm for annealed CAO TFTs at $V_{gs} = 20$ V is relatively low despite the high mobility; this suggests a low carrier concentration. Due to the $CAO/SiO_2/Si$ configuration, it is fully depleted, making Hall measurement difficult at $V_{\mathrm{gs}} = 0$. Therefore, the carrier density was estimated from the effective conductivity and found to be on the order of 10^{16} $\mathrm{cm^{-3}}$. On the other hand, CAO films grown using the DC magnetron sputtering technique reveal a higher carrier concentration of 1.5×10^{17} $\mathrm{cm^{-3}}$ along with a Hall mobility of $13.1\,\mathrm{cm^2/V \cdot s}$ [117]. No intentional p-type doping was carried out in this work. The origin of holes in Cu_2O was reported to be the ionized Cu vacancies and ionized interstitial oxygen [118]. In the LBL process, oxidation is performed based on saturated oxygen adsorption, so increasing the ionized interstitial oxygen seems challenging. Improving the LBL process by controlling Cu vacancy and intentional doping is necessary.

Table 5.1 Extracted TFT properties of TC and OC characteristics.

Thickness (nm)	Annealing (°C)	Threshold voltage (V)	Field-effect mobility ($\mathrm{cm^2V^{-1}s^{-1}}$)		Effective channel conductivity (S/cm)	
			$\mu_{FE(\mathrm{lin})}$	$\mu_{FE(\mathrm{sat})}$	$V_{gs} = 15\,\mathrm{V}$	$V_{gs} = 20\,\mathrm{V}$
(a) 150	RT	-9.0	0.55	0.50	0.08×10^{-2}	0.19×10^{-2}
(b) 150	990	-7.53	3.6	4.1	0.92×10^{-2}	1.8×10^{-2}

5.3 A Comparative Analysis of the CAO p-Type TFTs

Numerous studies have explored the fabrication and characterization of p-type TFTs incorporating materials such as Cu_2O and CAO. Within CAO TFTs, the CuO layer is crucial in facilitating hole transportation within the device. In comparison to crystalline materials, amorphous materials offer several advantages for TFT applications. Their lack of grain boundaries facilitates better uniformity and relatively simpler manufacturing processes. Additionally, their compatibility with low-temperature processing makes them suitable for deposition on flexible substrates. Among p-type amorphous semiconductors, a-Cu_2O stands out, although its transparency is limited. Conversely, CAO, known for its transparent properties, offers additional advantages for transparent applications. Table 5.2 offers a comparative analysis of p-TFT device performance. This study encompasses discussions on both amorphous and crystalline CAO TFTs. It's worth noting that the current a-CAO also exhibits promising transistor characteristics.

Sol-gel fabricated TFTs examine low field effect mobility compared to the sputtering methods. This difference can be attributed, in part, to the inherent non-uniformity of films commonly observed in sol-gel processes, leading to substantial scattering phenomena. Notably, in the presented data, the highest field-effect mobility of 0.97 $cm^2V^{-1}s^{-1}$ is achieved for crystalline CAO fabricated via Radio Frequency Magnetron Sputtering (RFMS), accompanied by a prominently observed Hall mobility of 39.5 $cm^2V^{-1}s^{-1}$ [33].

Table 5.2 Exploring the Electrical Performance in p-Type TFTs

Method	Phase	Type	Sub.	Tdep (°C)	Tpda (°C)	μHall ($cm^2V^{-1}s^{-1}$)	Nh (cm^{-3})	σ (S/cm)	Vth	μFE ($cm^2V^{-1}s^{-1}$)	Ion/Ioff	T (%)	Eopt (eV)	Year	Ref
PLD	$CuAlO_2$	Hall	$(0001)Al_2O_3$	700		10.4	1.3×10^{17}	9.5×10^{-2}				60-70	3.5	1997	[6]
RFMS	$CuAlO_2$	Hall	$(0001)Al_2O_3$	RT	900	0.4	3×10^{18}						3.45	2011	[119]
RFMS	$CuAlO_2$:CuO	TFT/Hall	SiO_2/n-Si	940		8.6	3.6×10^{18}	5	-5	0.97	8×10^2		3.46	2012	[33]
RFMS	$CuAlO_2$	Hall	SiO_2/n-Si	940		39.5	4.3×10^{15}	2.7×10^{-2}					3.79	2012	[33]
RFMS	$Cu_{0.83}AlO_{2.16}$	Hall	Glass	500		0.82	1.5×10^{15}	1.9×10^{-4}						2013	[99]
RFMS	a-Cu_2O	Hall	Quartz	RT		0.243	1.92×10^{19}							2013	[120]
PLD	$CuAlO_2$	Hall	$(0001)Al_2O_3$	650	1000	8.14	2.7×10^{17}					85	3.54	2014	[121]
solgel	Cu_2O	TFT	SiO_2/p-Si	350	700		1.79×10^{17}		-14.7±0.8	0.006±0.004	10^3	60	3.25	2018	[26]
solgel	Cu_2O, $CuAlO_2$	TFT	SiO_2/p-Si	350	1000		1.03×10^{17}		-1.3±0.5	0.098±0.009	10^3	80	3.8	2018	[26]
solgel	$CuAlO_2$	TFT	SiO_2/p-Si	400	900				-34.65±4.5	0.33±0.05	10^5	80	3.68	2019	[32]
LBL-DPDS	a-$CuAlO_2$	TFT	SiO_2/p-Si	RT			1.9×10^{15}	1.9×10^{-3}	-9	0.5	6×10^2			this work	
	$CuAlO_2$	TFT	SiO_2/p-Si	RT	990		1×10^{16}	1.8×10^{-2}	-7.53	4.1	3×10^4			this work	

In the present study, a DPDS-assisted LBL approach was employed for CAO thin film deposition. The optimized annealed CAO TFT exhibited remarkable mobility of $4.1\,cm^2/Vs$, a threshold voltage of $-7.53\,V$, and an I_{on}/off ratio of 3×10^4. Notably, as-deposited CAO TFTs also exhibited TFT characteristics with a threshold voltage of $-9.0\,V$, an I_{on}/off ratio of 6×10^2, and a field-effect mobility of $0.5\,cm^2/Vs$.

Compared to solution-based TFTs, the improved V_{th} values were observed in CAO TFTs grown by DPDS-assisted LBL, both in as-deposited and annealed states. DPDS typically yields high-quality and uniform thin films compared to solution-based deposition methods.

The resulting CAO films deposited by sputtering under LBL ensure highly ordered CuO and AlO layers with uniform film thickness, lowering the interface roughness and leading to improvement in V_{th}. Later, annealing processes can further enhance the properties of CAO films. Annealing promotes crystallization, which can lead to reduced trap states and improved charge transport characteristics. As a result, annealed CAO TFTs exhibit lower V_{th} values due to improved carrier mobility. The performance of as-deposited CAO TFT is comparable to reported solution-processed TFTs.

For the as-deposited CAO TFT, the I_{on}/I_{off} is comparable to the reported CAO TFT deposited by magnetron sputtering. The main reason for the low I_{on}/I_{off} ratio is mainly attributed to the fact that it had a leakage current through the grain boundary and surface in such a wide channel TFT, which increased the OFF current and thus reduced the ratio consequently. In the TFTs, substrate resistance does exist, but it does not significantly influence the I_{DS} during DC measurements without gate leakage. This is because DC measurements reflect a steady state, where the gate current becomes zero, indicating no current flow through the gate terminal. Furthermore, despite the expectation of charge transfer to the gate, the 200 nm thickness of the SiO_2 gate serves as an effective barrier against gate leakage. In such a way, the gate current minimally impacts the drain current characteristics. It's noteworthy that annealing brought improvement in crystallinity and enlargement of grain size, which improved the grain boundary and surface; consequently, the I_{on}/I_{off} improved for the annealed CAO p-TFT.

The superior performance achieved through the DPDS approach can be attributed to enhanced crystallinity and orderly stacking of CuO and AlO along the c-direction, minimizing carrier scattering and consequently improving TFT performance.

5.4 Summary of Chapter 5

Chapter 5 provides a detailed examination of the fabrication process of CAO a p-type TFTs using shadow masking, along with a thorough analysis of the electrical characteristics of CAO via electrometers. It begins with a discussion on the fabrication and reported results of p-type CAO TFTs, followed by an explanation of the CAO TFT fabrication process. The chapter then delves into the characterization of TFT characteristics, exploring parameters such as field effect mobility, threshold voltage, and conductivity.

Chapter 6

Conclusion and future work

6.1 Conclusion

In summary, Al-substituted $CuMn_{1-x}Al_xO_2$ samples were successfully synthesized via the sol-gel auto-combustion route using nitrate precursors. XRD analysis revealed an enlargement of the unit cell with Al substitution, while SEM images depicted irregular grains ranging in size from 108 nm to 363 nm. Dielectric studies showed an increase in the real part of the dielectric constant with Al content, alongside decreased tangent losses, indicating improved leakage current. Higher Al content corresponded to lower resistive behavior according to Nyquist plots. The grain resistance and capacitance are in the range of 3.6 M to 4.9 M and 31.3 pF to 85.5 pF, respectively. The sol-gel synthesis offered cost-effectiveness and ease of use but may not yield high-quality CAO. Subsequently, (CAO) was deposited on Si-substrate by DPDS sputtering for further investigation.

$CuAlO_2$ having a dominance phase along the (004) plane was grown by DPDS under the LBL approach. C-axis oriented CAO thin film was obtained at an annealing temperature of 990 °C by carefully optimizing the deposition rates. The deposition process exhibited a consistent and uniform growth rate of 0.57 nm per cycle, as evidenced by the constant pulse voltage and plasma current profiles. Under such a process, CAO p-TFT was successfully fabricated. For the optimized CAO p-TFT, the threshold voltage of -7.53 V and field effect mobility of 4.1 $cm^2V^{-1}s^{-1}$ was recorded. Moreover, p-TFT properties and field-effect mobility comparable to the annealed CAO reported previously were observed in the as-deposited CAO films. We speculate that DPDS-assisted LBL for the controlled stacking is a good approach in the growth of CAO thin film and in implementing CAO as a channel layer for p-TFTs.

6.2 Future Work

The current mobility value achieved in our study demonstrates promising advancements. Yet, we acknowledge that its potential is somewhat hindered by the presence of a fraction of the CAO crystal planes retaining random orientations. To realize the desired complete c-axis orientation of the CAO crystalline planes, it is imperative to delve deeper into achieving atomically precise control over the annealing conditions. By refining our understanding and controlling these conditions, we anticipate unlocking further enhancements in mobility, thereby boosting the performance of our materials.

One of its most important properties, the low conductivity of the CAO, is still the main problem. No intentional p-type doping was carried out in this work. The origin of holes in Cu_2O was reported to be the ionized Cu vacancies and ionized interstitial oxygen. For the $CuAlO_2$ thin films, in 1997, Kawazoe demonstrated a room temperature conductivity of $0.1\,S\,cm^{-1}$ [6]. Addressing the persistent challenge of low conductivity in p-type $CuAlO_2$, future research will focus on optimizing Zn doping concentrations and deposition techniques to enhance electrical properties. Building upon the findings of Aston et al. [122] regarding Zn substitution for Al and its compensatory effect through oxygen deficiency, Dong's investigations explore the effectiveness of Zn^{2+} doping in $CuAl_1-xZnxO_2$ thin films deposited via rf magnetron sputtering [123]. Initial results demonstrate a significant increase in electrical conductivity with Zn doping, reaching a maximum conductivity of $0.124\,S\,cm^{-1}$ at a Zn concentration of 0.5%, while excessive Zn concentration induces heavy scattering due to increased lattice defects. In the LBL process, oxidation is performed based on saturated oxygen adsorption, so increasing the ionized interstitial oxygen seems challenging. Improving the LBL process by controlling Cu vacancy and intentional doping is necessary. Leveraging advanced deposition methods such as DPDS for atomically precise deposition and enhanced film quality, future studies aim to refine the conductivity enhancement mechanism of Zn-doped $CuAlO_2$ thin films, facilitating their integration into practical electronic applications.

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Appendix A

Performance Evaluation of TFTs:

The TFT device is evaluated using two main characteristic curves: output (I_D vs. V_{DS}) and transfer (I_D vs. V_g) characteristic curves. In the linear and saturation regions, I_D can be estimated by the Shichman-Hodges FET model.

Linear region: when the magnitude of V_{DS} is small ($V_{DS} \ll (V_g - V_{Th})$, then I_D increases linearly.

$$I_D = \frac{W\mu C_{ox}}{L}(V_g - V_{Th})V_{DS}$$

Saturation region: when V_{DS} is large ($V_{DS} \gg (V_g - V_{Th})^2$), then I_D gains a saturation state.

$$I_D = \frac{W\mu C_{ox}}{2L}(V_g - V_{Th})^2$$

Where W, μ, C_{ox}, and L are the channel width, mobility, capacitance, and channel length, respectively.

$$C_{ox} = \frac{C}{A} = \frac{k\varepsilon_0}{d}$$

Where k, ε_0, and d are the dielectric constant of the gate dielectric material, the electrical permittivity of vacuum, and the thickness of the layer.

Carrier mobility, current on/off ratio, threshold voltage, and sub-threshold swing are important parameters involved in the evaluation of TFT devices, which can be extracted from the characteristic curves.

A.0.1 Threshold Voltage (V_{Th}):

It is the minimum V_g that causes the accumulation of carriers on a semiconductor-dielectric interface and turns on the TFT device. For n-type TFTs, if V_{Th} is positive, the device is in enhancement mode, and if it is negative, the device is in depletion mode. For p-type TFTs, it

follows the same but in the opposite fashion. Enhancement mode is desirable as no voltage is required to turn off the transistor, making circuit design easier and minimizing power dissipation. From the linear region of I_D vs. V_g, V_{Th} can be deduced for low V_{DS}, and for high V_{DS}, it can be determined from $I_D^{1/2}$ vs. V_g plot.

A.0.2 Carrier Mobility:

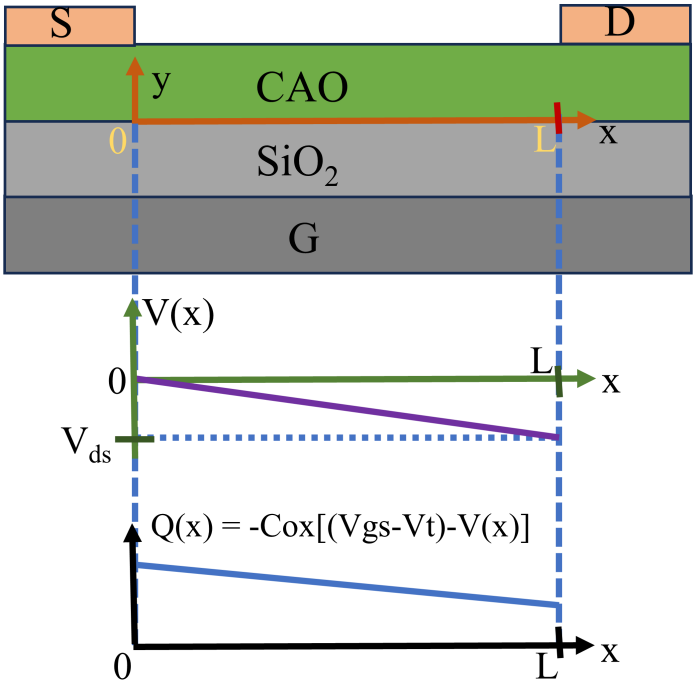

Fig. A.1 Gradual channel approximation

In the analysis of the electrical properties of TFT, the gradual channel approximation is made as schematically represented by Fig.A.1. In such a model, the electric field between the S-G electrode is comparatively larger than the electric field between the S-D electrodes, where the dielectric thickness (d) and the channel length (L) satisfy the relation $L/d \geq 10$. The application of V_{gs} increases the density of carrier accumulation at the semiconductor-dielectric interface, forming one-dimensional potential (i.e., across the channel). The total charge density along the channel is given by

$$Q = -C_{ox} V_{total}(x)$$

Here, C_{ox} is the gate oxide dielectric constant, and $V_{total}(x)$ is the total potential along the distance (x) across the S-D electrode resulting from applied V_{ds} and V_{gs}. However, in a real

device, V_{th} is required to fill traps before the mobile charge carriers are accumulated. In such a way, $V_{total}(x) = V_{gs} - V(x) - V_{th}$, thus the equation becomes,

$$Q_{mobile} = -C_{ox}(V_{gs} - V(x) - V_{th})$$

The mobile charges create the current I_d between S-D electrodes, defined as

$$I_d = \mu Q W E_x$$

$$I_d = \mu Q W \left(-\frac{dV}{dx}\right)$$

$$I_d dx = -\mu Q W dV$$

Now, substituting the value of Q,

$$I_d dx = W \mu C_{ox}(V_{gs} - V(x) - V_{th}) dV$$

Assuming that the charge-carrier mobility does not vary with the applied potential, integrating equations along the channel from $x = 0$ to L and from $V = 0$ to V_{ds}, such as

$$\int_0^L I_d dx = W \mu C_{ox} \int_0^{V_{ds}} (V_{gs} - V(x) - V_{th}) dV$$

$$I_{d(lin)} = \frac{W}{L} \mu C_{ox} \left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}(V_{ds})^2\right]$$

Due to pinch-off at saturation region results in an effective maximum V_{ds} of $V_{ds} = V_{gs} - V_{th}$, substituting the values, the above equation for the saturation drain current will be,

$$I_{d(sat)} = \frac{W}{2L} \mu C_{ox}(V_{gs} - V_{th})^2$$

Taking the derivative of $I_{d(lin)}$ and $I_{d(sat)}$ with respect to V_{gs}, the calculation of the charge-carrier mobility in the linear and saturation regions, respectively,

$$\mu_{lin} = \frac{L}{W C_{ox} V_{ds}} \frac{dI_D}{dV_{gs}}$$

$$\mu_{sat} = \frac{2L}{W C_{ox}} \left(\frac{d\sqrt{I_D}}{dV_{gs}}\right)^2$$

A.0.3 Current On/Off Ratio (I_{on}/I_{off})

It is the ratio of channel current for TFT that is ON and in the OFF state. I_{on}/I_{off} can be deduced from the characteristic curve while dividing the value of I_{Dmax} by I_{Dmin}. For an ideal transistor, I_{Dmin} must be zero, but here in the case of a p-type copper oxide-based transistor the electron accumulation in the off-state due to minority carriers formed by Cu_i (copper interstitial), the current ID_{min} has a nonzero current even in the OFF state of TFT [124]. Devices having I_{on}/I_{off} values more than 10^5 to 10^6 are desirable for rapid switching and high-resolution displays.

Appendix B

Related Publications

B.1 Journal

[1] **Mehdi Ali**, Daiki Yamashita, and Hideo Isshiki (2024). Growth of $CuAlO_2$ on SiO_2 under a layer-by-layer approach conducted by digitally processed DC sputtering and its transistor characteristics, *Japanese Journal of Applied Physics*, 63 035502.

B.2 Conference

[1] **Mehdi Ali**, Daiki Yamashita, and Hideo Isshiki (2023). Synthesis of $CuAlO_2$/Si heterostructures by DPDS-assisted LBL approach and their transistor characteristics, *Solid State Devices and Materials (SSDM2023)*, September 5th - 8th, 2023.

[2] **Mehdi Ali** and Hideo Isshiki (2022). Fabrication and characterization of $CuAlO_2$ thin film transistor by Digitally Processed DC Reactive Sputtering, *Joint ECTI-BEC and ASEA-UEC Workshop 2022*, December 9th, 2022.

[3] H. Isshiki, G. Nakamura, G. Fabiola, K. Takamura, **M. Ali**, Y. Zhang, Y. Tanaka, and S. Saisho (2022). Atomically Precise Deposition of Multi-Element Metal Oxide Layered Crystals Alternating Digitally Processed DC Sputtering and Surface Oxidation, *Material Research Society (MRS) Spring Meeting*, May 8th-13th, 2022.

[4] **Mehdi Ali** and Hideo Isshiki (2022). Growth of $CuAlO_2$/Si by Digitally Processed DC Reactive Sputtering, *Joint ECTI-BEC and ASEA-UEC Workshop 2021*, December 10th, 2021.

[5] **Mehdi Ali** and Hideo Isshiki (2022). Synthesis and Characterization of p-type $CuAlO_2$ by Digitally Processed DC Reactive Sputtering, *UEC mini-conference*, March 3rd, 2021.