Rapid Single-Flux-Quantum NOR Logic Gate Realized through the Use of Toggle Storage Loop

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BRIEF PAPER

Rapid Single-Flux-Quantum NOR Logic Gate Realized through the Use of Toggle Storage Loop

Yoshinao MIZUGAKI[†a)], ***Member***, **Koki YAMAZAKI**[†], ***and*** **Hiroshi SHIMADA**[†], ***Nonmembers***

SUMMARY Recently, we demonstrated a rapid-single-flux-quantum NOT gate comprising a toggle storage loop. In this paper, we present our design and operation of a NOR gate that is a straightforward extension of the NOT gate by attaching a confluence buffer. Parameter margins wider than ±28% were confirmed in simulation. Functional tests using Nb integrated circuits demonstrated correct NOR operation with a bias margin of ±21%.

key words: *superconducting digital gates, Nb IC, single-flux-quantum circuits*

1. Introduction

Superconducting digital circuits have been expansively developed for the last three decades [1]–[11]. Among several superconducting digital technologies, the rapid single-flux-quantum (RSFQ) technology [1], where the existence and absence of a single flux quantum (SFQ) in a superconducting loop respectively represent the binary digital states of "1" and "0", is the most developed and widely used. One achievement is a 33 GHz-clock RAM-embedded microprocessor in which 10,603 Nb Josephson junctions (JJs) are integrated [12].

For designing RSFQ digital circuits, logic cell libraries, in which tens of logic cells are compiled, have been established and being extended. Recently, we experimentally demonstrated operation of a NOT gate [13], of which the equivalent circuit is shown in Fig. 1, as an alternative NOT logic cell compatible with the library referred to as "CONNECT" [14]. Its configuration was similar to the NOT gates described in [15] and [16]. By using this NOT gate structure, we succeeded to reduce the cell size from 80 μm × 80 μm to 80 μm × 40 μm [13].

Its NOT operation sequence is briefly explained as follows. When an SFQ comes from the input terminal, it is stored in the toggle storage loop (J_4-L_7-L_8-J_5-L_{10}-L_9) through J_1 and J_5. Then, an SFQ from the clock terminal is transferred not to the output terminal but to the storage loop through J_4, which annihilates the stored SFQ. It means that the input "1" results in the output "0". When an SFQ comes from the clock terminal without a preceding SFQ from the input terminal, it is transferred to the output terminal. This means that the input "0" results in the output "1".

This NOT gate can be applied to other negative logic gates. It was numerically presented that a NOR gate was realized by combining this NOT gate and a confluence buffer [13], [16], whereas experimental verification was not conducted. Since a NOR gate is one of the universal logic gates that can implement any Boolean function, it is worth while to verify the operation of the proposed NOR gate in experiments. In this paper, we present our design and functional tests of the NOR gate on niobium integrated circuits.

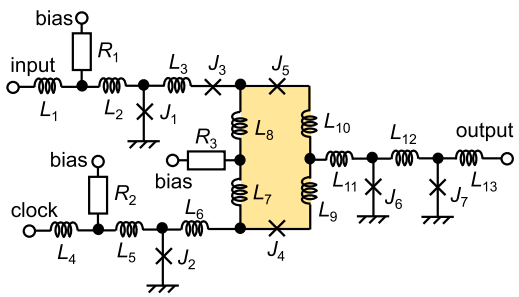

Fig. 1 Equivalent circuit of a NOT gate comprising a toggle storage loop. All Josephson junctions (JJs) are externally shunted to make the McCumber parameter β_c be 0.89 for ensuring compatibility with the CONNECT library [14]. The storage loop is filled in light brown.

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[†]The authors are with The University of Electro-Communications, Chofu-shi, 182–8585 Japan.
a) E-mail: y.mizugaki@uec.ac.jp

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2. Configurations of NOR Gate

The equivalent circuit of the NOR gate is shown in Fig. 2. It consists of a confluence buffer and a NOT gate. More specifically, the input terminal of the NOT gate shown in Fig. 1 is replaced with a confluence buffer with two input terminals, which realizes a 2-input NOR function. The loop consisting of J_{11}-L_{17}-L_{18}-J_{12}-L_{20}-L_{19} works as a toggle storage loop.

We obtained the circuit parameters by using a

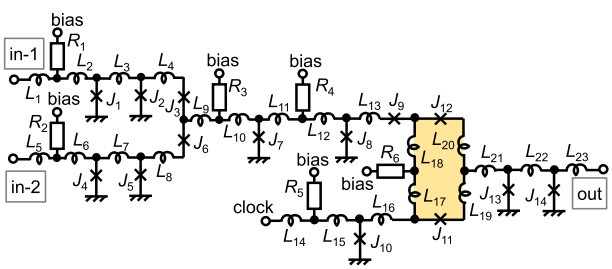

Fig. 2 Equivalent circuits of the NOR gate. All JJs are externally shunted to make the McCumber parameter β_c be 0.89 for ensuring compatibility with the CONNECT library. The storage loop is filled in light brown.

Table 1 Optimization results of the circuit parameters for the NOR gate. Values of inductances (L_i), junction critical currents (J_i), and resistances (R_i) are presented in units of pH, μA, and Ω, respectively. The nominal bias voltage is 2.5 mV. The inductance value of L_9 was fixed to 0.01 pH during the optimization.

$L_{1,5,14}$	$L_{2,6}$	$L_{3,7}$	$L_{4,8}$	L_{10}	L_{11}	L_{12}	L_{13}
0.83	1.90	2.28	1.23	4.32	1.66	1.42	3.50
L_{15}	L_{16}	L_{17}	L_{18}	L_{19}	L_{20}	L_{21}	L_{22}
1.50	3.33	8.97	1.01	0.63	0.59	1.37	5.50
L_{23}	$J_{1,4}$	$J_{2,5}$	$J_{3,6}$	J_7	J_8	J_9	J_{10}
1.51	200	195	148	165	261	100	196
J_{11}	$J_{12,13}$	J_{14}	$R_{1,2}$	R_3	R_4	R_5	R_6
143	100	208	8.34	9.00	13.3	16.7	17.0

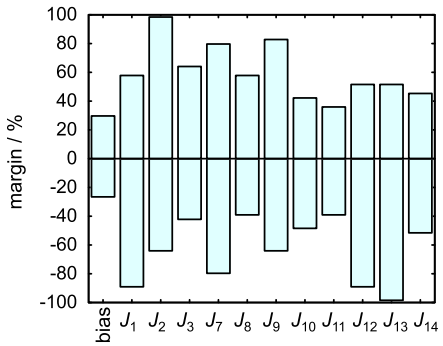

Fig. 3 Margins of the bias voltage and junction critical currents for the NOR gate.

Josephson circuit simulator "JSIM" [17] and an optimization program "SCOPE2" [18]. The obtained parameters are tabulated in Table 1 [13], whereas the margins of the bias voltage and junction critical currents are plotted in Fig. 3. Relatively satisfactory margins wider than ±28% are confirmed.

We confirmed by numerical simulation that the NOR gate worked correctly at clock frequencies up to 51.3 GHz for the nominal bias voltage (2.5 mV). We also numerically simulated operation of the NOR gate cell compiled in the CONNECT library, which demonstrated that its maximum clock frequency for the nominal bias voltage was 36.8 GHz. These results indicated that the NOR gate developed in this work would have advantage for high speed operation.

Our NOR gate is a straightforward extension of the NOT gate by attaching a confluence buffer, and therefore, it would not offer the most efficient design. In addition, our NOR gate is designed to be compatible with cells in the CONNECT library. For example, Myoren *et al.* presented another RSFQ NOR gate with numerical results [19]. The number of JJs in their NOR gate was 6, whereas that in our NOR gate is 14. However, our NOR gate would provide a guide to other negative logic functions utilizing a toggle storage loop.

3. Experimental Results and Discussion

We designed test circuits of the NOR gate with digital cells in the CONNECT library. Inductance extraction program

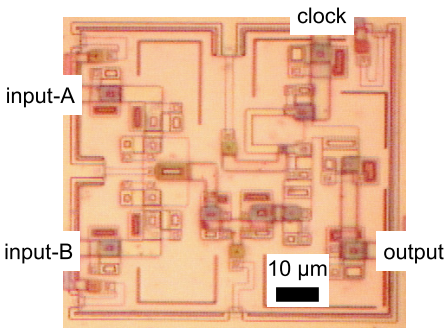

Fig. 4 Photomicrographs of a NOR gate cell. The cell size is 80 μm × 80 μm.

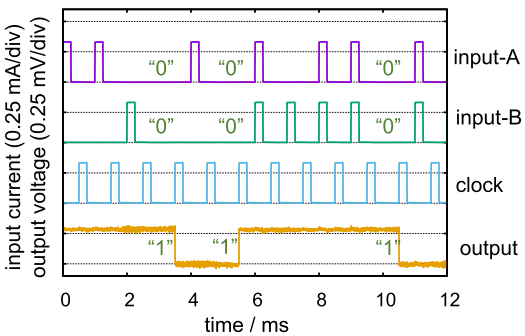

Fig. 5 Waveforms of functional tests of a NOR gate. An SFQ was fed to the input-A, input-B, and clock terminal at the rising edges of input current signals. For the output signal of an SFQ-to-dc converter, no voltage transition represented "0" output, whereas a high-to-low or low-to-high voltage transition represented "1" output.

"InductEX" [20] was used for design of inductance layouts. Conventional Josephson transmission lines, dc-to-SFQ converters, and an SFQ-to-dc converter were used for the IO elements. Test chips were fabricated using a 25-μA/μm^2 Nb/AlO$_x$/Nb integration process [21] at the National institute of Advanced Industrial Science and Technology, Japan. Figure 4 shows photomicrographs of a fabricated NOR gate cell, each of which the dimensions are 80 μm × 80 μm.

In measurements, a test chip was cooled in a liquid helium bath. The output voltage was acquired with a digital oscilloscope via a 40-dB low-noise preamplifier. Low-speed tests to confirm the gate functions were conducted.

Results for functional tests of a NOR gate are presented in Fig. 5. Correct operations were confirmed. The bias margin was ±21%, slightly narrower than the numerical result of ±28%.

4. Conclusion

We presented our design and operation of a NOR gate comprising a confluence buffer and a toggle storage loop. The NOR gate was a straightforward extension of a NOT gate, a toggle storage loop with a confluence buffer attached. Functional tests using Nb/AlO$_x$/Al integrated circuits demonstrated correct NOR operation. An experimental bias margin as wide as 21% was confirmed for the NOR gate. The

results of the NOR gate operation opened a path for other negative logic functions utilizing a toggle storage loop.

Acknowledgments

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