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doi: 10.7567/JJAP.57.098006

One-dimensional array of small tunnel junctions fabricated using 30-nm-diameter gold nanoparticles placed in a 140-nm-wide resist groove

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We present percolative arrays of gold nanoparticles (NPs) formed in a resist groove. To enhance the connection probability, the width of the resist groove (140 nm) was designed to be approximately five times larger than the diameter of gold NPs (30 nm). Two-stage deposition of gold NPs was employed to form bridge connections between the source and drain electrodes. Dithiol molecules coated on surfaces of gold NPs worked as tunnel barriers. 5 of 12 samples exhibited Coulomb blockade characteristics, in one of which the gate response was confirmed.

Operation of single-electron (SE) devices is based on the Coulomb blockade (CB) phenomenon that appears in arrays of small tunnel junctions.[1)] One important parameter related to SE devices is the charging energy of an electron on an island electrode, which is commonly referred to as E_C and should be greater than the thermal energy of the environment. Since E_C is inversely proportional to the total capacitance of an island electrode, smaller island electrodes are preferable to higher operation temperatures. Over the last two decades, gold nanoparticles (NPs) have often been used for island electrodes in SE devices.[2–15)] Fabrication of gold NP arrays with well-defined positioning is thus important to improve the yield and performance of SE devices with NP island electrodes.

Among nanofabrication techniques, electron-beam (EB) lithography is one of the established methods of patterning features down to 10 nm. Jiang et al. demonstrated the one-dimensional (1D) arrangement of gold NPs in grooves of lithographic resist patterns.[16)] The widths of the resist grooves and the thicknesses of the electric double layers (EDLs) surrounding gold NPs in a colloidal solution were the key factors for the arrangement.[17)] In their

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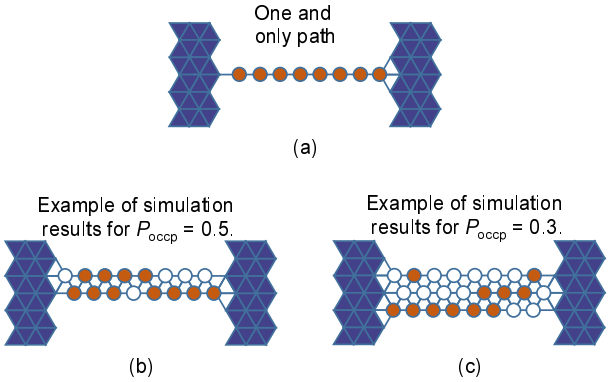

Fig. 1. (Color online) Percolative connections in (a) one, (b) two, and (c) three rows of NP sites. Triangular grids are assumed. The length L of a row (the number of NP sites in a row) is 8. The one and only path exists for one row of sites, as shown in (a). In (b) and (c), examples of simulation results are presented, where 0.5 and 0.3 were the minimum occupation probabilities (P_{occp}) exhibiting percolative connection for two and three rows, respectively.

work, 1D arrays with different NP sizes and interdistances were realized.

In this brief note, we describe our SE devices fabricated using a 1D array of gold NPs formed in a groove of a lithographic resist pattern. We implemented two ideas in our fabrication process. (i) The interdistances between gold NPs presented by Jiang et al.[16] were too long to realize electron tunneling. Since the electric repulsive force between NPs in a colloidal solution stops NP deposition on the substrate, we additionally deposited gold NPs after dithiol treatment on the previously formed NPs.[2] This two-stage deposition would realize gold NP arrays connected through dithiol tunnel barriers. (ii) Because pure 1D arrangement was hardly expected to be robust to form a series array of tunnel junctions, we designed resist grooves to have widths slightly larger than the nominal diameter of gold NPs to increase the connection probability.

Before we describe our fabrication process, we present numerical results of percolative connection through paths with randomly placed NPs. In a pure 1D array of gold NPs, one flaw in the NP arrangement and/or in the the junction formation results in disconnection. Figure 1 shows examples of percolative connections[18] in one, two, and three rows of NP sites. Here, triangular grids are assumed, while two-stage deposition is not calculated.

All NP sites must be filled to realize percolative connection in pure 1D placement ($W = 1$, where W is the number of rows) as shown in Fig. 1(a). The connection probability P_{cnnct} is expressed as $P_{cnnct} = {P_{occp}}^{L}$, where L and P_{occp} are the length of (the number of NP sites in) a row and the occupation probability of each NP site, respectively. As shown in Figs. 1(b)

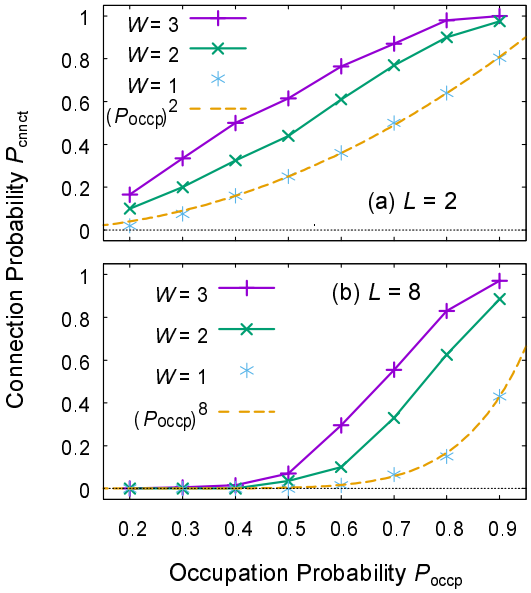

Fig. 2. (Color online) Numerical results for P_{cnnct} plotted as functions of P_{occp} for $L = 2, 8$ and $W = 1, 2, 3$.

and 1(c), on the other hand, P_{cnnct} is improved for the two- ($W = 2$) and three-row ($W = 3$) systems because the paths through neighboring rows assist percolative connection.

We numerically simulated percolative connection for the systems of $L = 2, 8$ and $W = 1, 2, 3$. P_{cnnct} was derived from 200 simulations for each P_{occp} value between 0.2 and 0.9 in increments of 0.1. It is confirmed in Fig. 2 that results for the pure 1D array ($W = 1$) agree with the mathematical models of $P_{\mathrm{cnnct}} = {P_{\mathrm{occp}}}^2$ and $P_{\mathrm{cnnct}} = {P_{\mathrm{occp}}}^8$ for $L = 2$ and 8, respectively. On the other hand, P_{cnnct} values for both L values of 2 and 8 are increased when W is increased to 2 or 3. These results support the idea that NP placement in a field wider than a pure 1D array would increase the yield of connections. Note that percolative connections for $W = 2$ and 3 shown in Figs. 1(b) and 1(c) include parallel connections of NPs to compensate for high P_{cnnct} values. The trade-off between high P_{cnnct} and less parallel connections would be optimized in the future with the parameters L, W, and P_{occp}.

On the basis of the results described above, we fabricated an array of gold NPs in a resist groove, the width of which was relatively large. The fabrication process is illustrated in Fig. 3. First, three electrodes made of NiCr/Au were prepared on an oxidized Si substrate by EB lithography, angle shadow evaporation, and lift-off [Fig. 3(a)]. The thicknesses of the first and second NiCr/Au layers deposited were 5/20 and 5/40 nm, respectively, where the evaporation angles were adjusted so that the Au layers completely covered the NiCr layers near the electrode gap. The widths of the source (S) and drain (D) electrodes were both 800 nm, whereas the gap length between them was approximately 60 nm. The gate (G) electrode

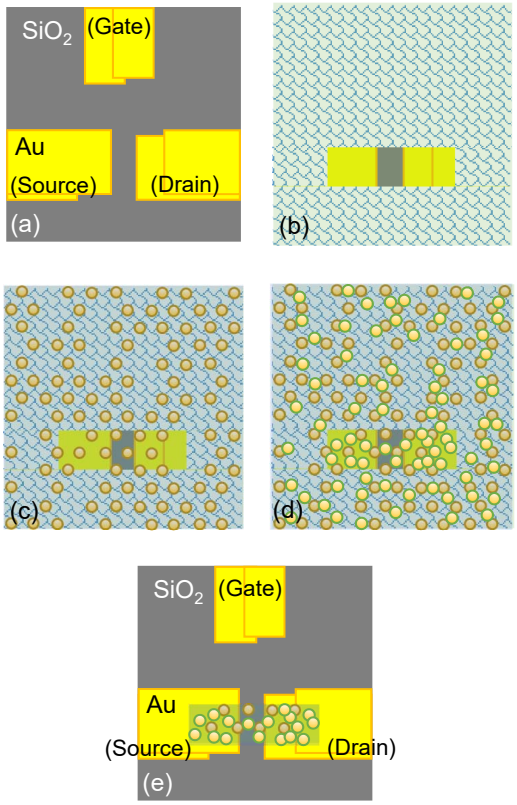

Fig. 3. (Color online) Schematic illustration of fabrication process (top view). (a) Three electrodes made of NiCr/Au were prepared on an oxidized Si substrate by EB lithography, angle shadow evaporation, and lift-off. (b) A resist groove was formed by EB lithography around the gap between the source (S) and drain (D) electrodes, which was followed by APTES treatment to form a silane monolayer on the substrate surface. (c) Gold NPs were distributed on the surface in a gold NP citric solution, followed by butane dithiol treatment to terminate the surface of gold NPs (and electrodes) with dithiol molecules. (d) The second deposition of gold NPs was executed in a gold NP citric solution to form bridge connections of NPs through tunnel junctions. (e) The EB resist was lifted off.

was placed at a distance of 200 nm from the S and G electrodes.

Next, a resist groove was formed by EB lithography around the electrode gap. A 130-nm-thick ZEP-520A layer was used as a resist. The width of the groove was 140 nm, which was approximately five times larger than the diameter of gold NPs (30 nm). After the lithography, the sample was immersed in a 1% aqueous solution of 3-aminopropyl triethoxysilane (APTES) for 10 min to form a silane monolayer on the substrate surface [Fig. 3(b)].

The sample was then immersed in a colloidal citric solution of 30-nm-diameter gold NPs for 6 h (the first deposition). Gold NPs were distributed separately on the surface because of the EDLs surrounding the NPs.[2,16,17,19] After the immersion, the surface was modified by immersing the sample in a 0.5 mM ethanol solution of butane dithiol to terminate the surface

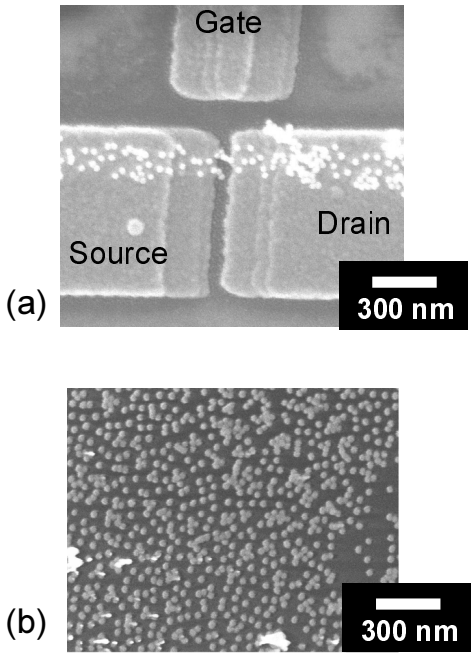

Fig. 4. (a) SEM image of a sample. A band of gold NPs is confirmed over the S and D electrodes. These electrodes are connected through an array of four gold NPs. The density of gold NPs was determined to be 382 particles/μm^2. (b) SEM image of gold NPs on a flat substrate without a resist groove. The density of gold NPs was 984 particles/μm^2.

of gold NPs (and electrodes) with dithiol molecules [Fig. 3(c)].

After the dithiol treatment, gold NPs were deposited again by immersing the sample in a colloidal citric solution of 30-nm-diameter gold NPs for 2 h (second deposition).[2)] Bridge connections of gold NPs were expected to be formed through tunnel junctions [Fig. 3(d)].

Finally, the resist layer with gold NPs was lifted off. The S and D electrodes would be connected through tunnel junctions in arrays of gold NPs [Fig. 3(e)].

An SEM image of a sample is shown in Fig. 4(a). A band of gold NPs formed in a resist groove was found over the S and D electrodes. The density of gold NPs in the band was determined to be 382 particles/μm^2. On the other hand, Fig. 4(b) shows gold NPs on a flat substrate without a resist groove, the NP density of which was 984 particles/μm^2. If we assume a simple hexagonal closest packed structure of 30-nm-diameter gold NPs, the density should be 1,283 particles/μm^2. Then, the P_{occp} in a resist groove is calculated as 0.298, whereas that on a flat substrate is 0.767. One possible reason for such low NP densities is that gold NPs surrounded by an EDL in a citric solution have effective diameters larger than those of gold NPs.[16,17,19)] In our experiments, the EDL thickness and effective NP diameter were estimated to be 13 and 56 nm, respectively, with the assumption that the ionic strength

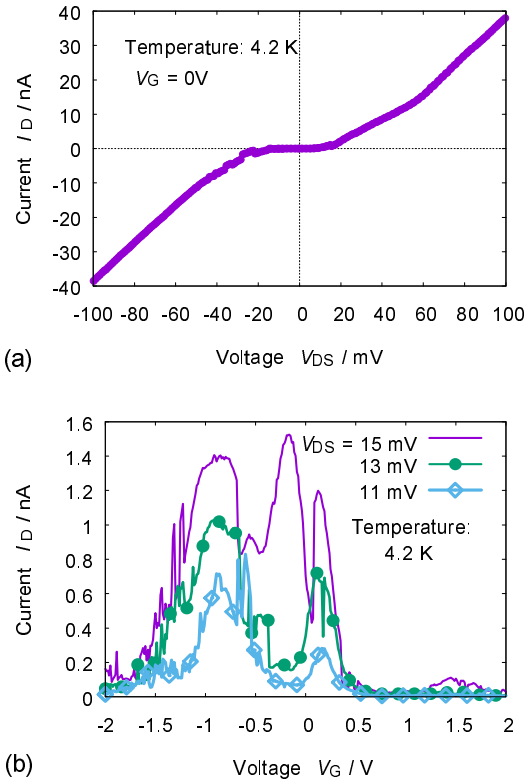

Fig. 5. (Color online) (a) I_D–V_{DS} characteristics for $V_G = 0$ measured in a liquid helium bath. (b) I_D–V_G characteristics at various V_{DS} values.

was 5.9×10^{-4} mol/L.[19] Moreover, Jiang et al. suggested that the hydrophobic resist walls would prevent gold NPs from approaching the groove bottom.[16]

Figure 4(a) also shows that the S and D electrodes are connected through an array of four gold NPs. We cooled the sample in a liquid helium bath and measured its electric characteristics using a semiconductor parameter analyzer (Keithley SCS-4200). During the measurements, the S and D electrodes were always symmetrically voltage-biased, that is, the drain voltage V_D and source voltage V_S were respectively set to $+V_{DS}/2$ and $-V_{DS}/2$, where $V_{DS} = V_D - V_S$ and $V_D + V_S = 0$.

Figure 5(a) shows the drain current I_D versus V_{DS} characteristics for the gate voltage V_G of zero. Current suppression due to the CB was confirmed at arround $V_{DS} = 0$. The Coulomb gap voltage was estimated as 31 mV by extrapolating the I_D–V_{DS} curve for $|V_{DS}| > 50$ mV.

We fabricated 12 samples on three different chips. 5 of the 12 samples exhibited I_D–V_{DS} characteristics with a CB region. The remaining 7 samples were insulative. The experimental P_{cnnct} was then 0.42 for the experimental P_{occp} of 0.298, which was close to the numerical result of $P_{cnnct} = 0.335$ for $(L, W, P_{occp}) = (2, 3, 0.300)$, as shown in Fig. 2(a). In addition, one

sample shown in Fig. 4(a) responded to V_G. Figure 5(b) shows the I_D–V_G characteristics at variousl V_{DS} values. I_D was modulated by V_G nonmonotonically.

Note that the characteristics were slightly unstable. For example, a peak of I_D at $V_G = -0.2$ V suddenly appeared when V_{DS} was increased to 15 mV. The stability of device characteristics, which was not focused on in this work, should be improved in the future.

Acknowledgments This work was partly supported by JSPS KAKENHI Grant Numbers 15K13999 and17K04979, and by JST-CREST Grant Number JPMJCR14F. The authors are grateful to M. Moribayashi, T. Yagai, and other laboratory members in UEC Tokyo for fruitful discussion and technical support. The support from Nation-wide Cooperative Research Projects, Research Institute of Electrical Communication, Tohoku University is also acknowledged.

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