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Gate-tuned negative differential resistance observed at room temperature in an array of gold nanoparticles

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Abstract We fabricated a single-electron (SE) device by using gold nanoparticles (Au NPs). Drain, source, and gate electrodes on a SiO_2/Si substrate were formed by using electron beam lithography (EBL) and thermal evaporation of Au. Subsequently, solutions of 3-nm-diameter and 5-nm-diameter Au NPs were dropped on the device to make current paths through Au NPs among the electrodes. Measurements of the device exhibited negative differential resistance (NDR) in the current-voltage characteristics between the drain and source electrodes at room temperature (298 K). The NDR behavior was tuned by applying a gate voltage.

Keywords Single-electron device · Negative differential resistance · Gold nanoparticles

1 Introduction

Single-electron (SE) devices with advantages of nanometer scale and low power consumption are prospective for integrated circuit applications [1]. Fabrication of room temperature SE devices requires an island size in the order of a few nanometers to suppress thermal effects [2]. To form such a tiny island, many techniques such as silicon technology [3], nano-oxidation process [4] or specific materials like carbon nanotube [5] have been used in fabrication processes. However, it is a tough challenge to pattern the island exactly in an ultrasmall size. One way to solve this problem is the use of gold nanoparticles (Au NPs) as islands of SE devices [6,7]. From the viewpoint of device properties, one of the interesting and useful characteristics of SE devices is negative differential resistance (NDR) [8,9], since NDR phenomena are widely applied in logic circuits [10–12], memory cells [13], multiplexers [14], oscillators [15,16], and amplifiers [17,18]. Nonetheless, the operation temperature of the fabricated NDR SE device has been limited under 1 K [9].

In this paper, we report a relatively simple fabrication method of an NDR SE device working at room temperature (298 K). We used standard electron beam lithography (EBL) for making three electrodes and several drops of solutions of Au NPs to form an array of small islands. NDR characteristics were observed at room temperature. Moreover, thanks to a three-terminal structure, the NDR characteristics was controlled by changing a gate voltage. The gate-tuned NDR characteristics were partially reproduced by Monte-Carlo simulation of a simplified array of tunnel junctions.

2 Fabrication process

Our fabrication process consisted of two steps. Firstly, drain, source and gate electrodes were prepared on a Si chip covered by SiO_2. The patterning was done by using a standard EBL with a PMMA resist followed by

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thermal evaporation of 30-nm-thick Au film and lift-off. The complexity of the fabrication process was reduced by forming a large gap in the order of a few micrometers between the drain and source electrodes. Secondly, an array of small islands were formed by dropping solutions of Au NPs. We used a combination of two kinds of solutions: 0.1μL of a toluene solution containing 0.1 wt% of 3-nm-diameter Au NPs chemisorbed via decanethiol [19], and 0.1μL of a citric solution containing 0.005 wt% of 5-nm-diameter Au NPs. We used 3-nm Au NPs to make the charging energies of island electrodes large enough for room temperature operation. 5-nm Au NPs were added to reduce resistance between the drain and source electrodes, which we empirically employed.

Scanning electron microscopy (SEM) images of the device are illustrated in Fig. 1. For clarity, edges of the drain, source, and gate electrodes are indicated by yellow dashed lines. The gap size between the drain and source electrodes is 3.1 μm. The distance from the gate top to the drain electrode is 7.3 μm. The gate electrode is placed asymmetrically to the drain and source electrodes. In our experiments, NDR characteristics were obtained in devices having an asymmetrically placed gate electrode, although it was unclear if such asymmetry was necessary for NDR.

In Fig. 1, white areas are arrays of Au NPs. It is observed in the wide area image (Fig. 1(a)) that distribution of Au NPs is not uniform. The magnified image around the gap between the drain and source electrodes (Fig. 1(b)) shows Au NPs of higher density, whereas there are much less Au NPs confirmed near the drain electrode in Fig. 1(c).

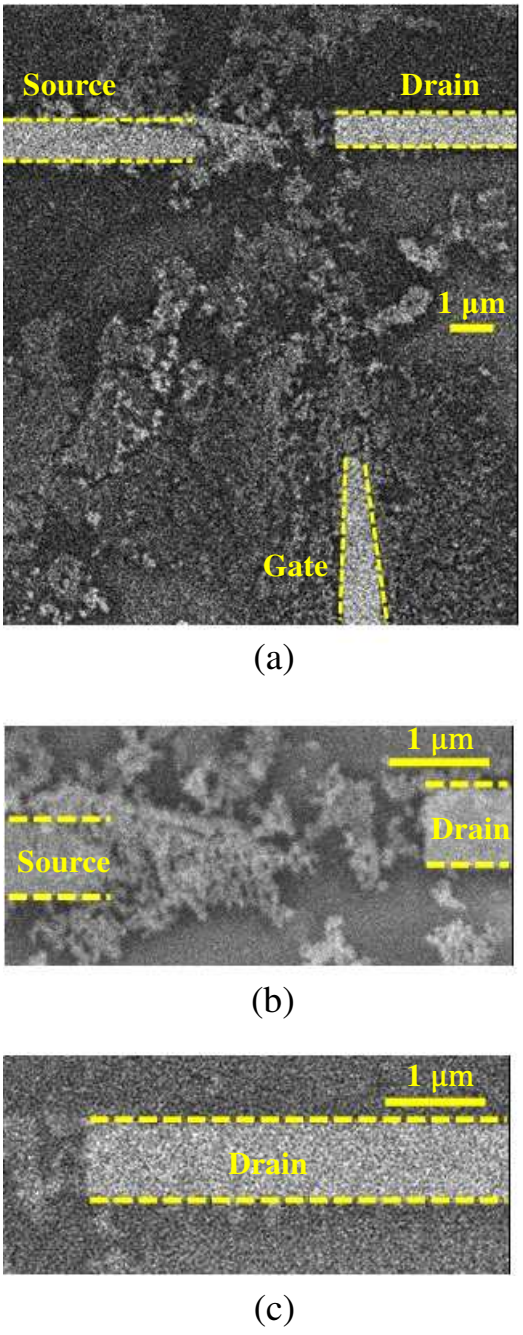

Fig. 1 Scanning electron microscopy (SEM) images of the fabricated device. (a) Wide area including three electrodes. (b) Magnified image around the gap between the drain and source electrodes. (c) Magnified image around the drain electrode.

3 Results

Electrical characteristics were measured at room temperature (298 K) by using a semiconductor parameter analyzer (SPA). Figure 2 shows a schematic configuration of the measurement set-up. A voltage applied to the drain electrode V_D and that applied to the source electrode V_S were the same in magnitude and opposite in polarity.

Figure 3(a) plots currents as functions of the drain-source voltage V_{DS} ($= V_D - V_S$) swept from -4 to $+4$ V with the fixed gate voltage V_G of 0.5 V. The drain current I_D, source current I_S, and gate current I_G are respectively represented by blue solid, blue dotted, and black solid curves. It can be seen that I_D and I_S have the identical amplitude with opposite polarity. I_G is smaller than 0.6 nA. NDR behavior (shown by the arrow in Fig. 3(a)) is confirmed in the region of 1.9 V $< V_{DS} <$ 2.5 V. In our experiments including other devices, NDR characteristics appeared when the magni-

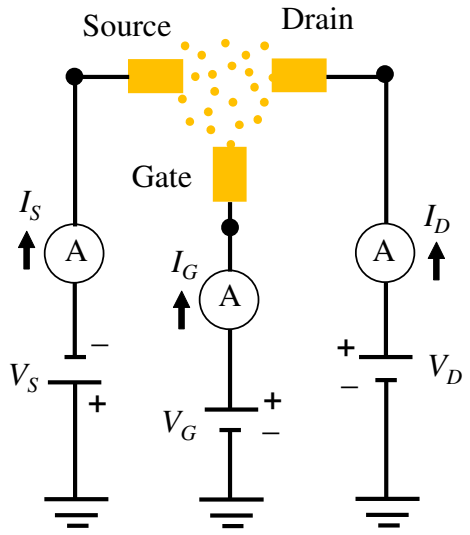

Fig. 2 A model of setting up measurement using a semiconductor parameter analyzer (SPA). Gold nanoparticles are presented by orange solid circles which distribute randomly among the electrodes

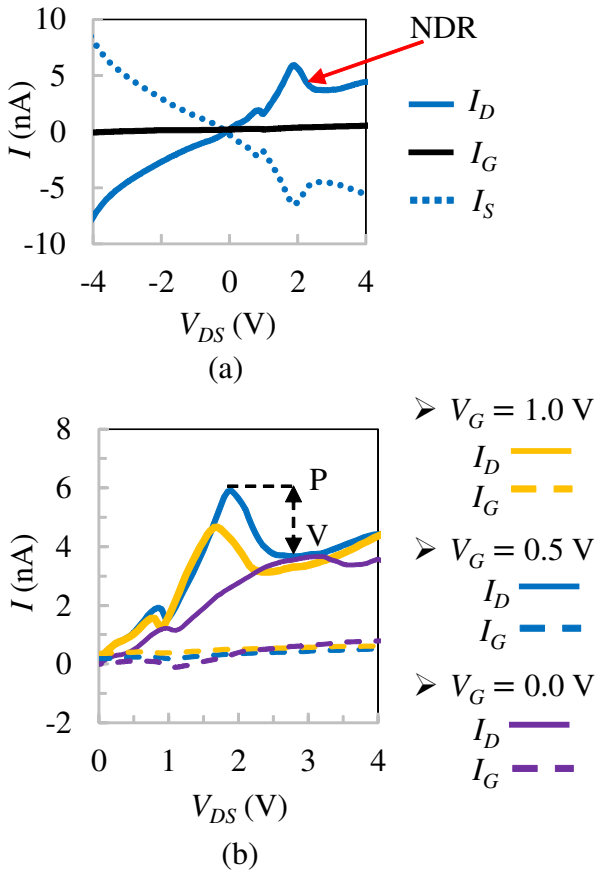

Fig. 3 Currents are plotted with the offset values at $V_G = V_{DS} = 0.0$ V substrated. (a) Drain current I_D, source current I_S, and gate current I_G as functions of V_{DS}. Gate voltage V_G is 0.5 V. (b) I_D and I_G versus V_{DS} at different V_G values of 0.0 V, 0.5 V, and 1.0 V. P and V respectively stand for the peak and valley points of the negative differential resistance (NDR)

tude of V_{DS} was swept in the increasing direction. The origin of this asymmetry is not clearly understood. Our simulation described later did not include the asymmetric position of the gate electrode.

Effects of the gate voltage on the NDR behavior are shown in Fig. 3(b), where I_D and I_G for V_G of 0.0 V, 0.5 V, and 1.0 V are respectively shown in solid and dashed curves. The absolute gate currents are less than 0.8 nA. We here focus on the most noticeable NDR appearing in region of 1.5 V $< V_{DS} <$ 2.5 V, although the other NDR characteristics are also confirmed in Fig. 3(b). The height between the peak and the valley (P-V height) of the NDR is shown by a double arrow. The P-V height is increased when V_G rises from 0.0 V to 0.5 V, whereas it is decreased when V_G increases further from 0.5 V to 1.0 V.

A controlling role of V_G on the NDR behavior is explicitly demonstrated in Fig. 4. Dependence of the P-V height on V_G is plotted in Fig. 4(a), where oscillation of the P-V height is confirmed. On the whole range of V_G, the P-V height is the highest (2.3 nA) at $V_G = 0.6$ V and the lowest (0.29 nA) at $V_G = 0.0$ V. NDR characteristics are also demonstrated in terms of the drain conductance, $G_D = dI_D/dV_{DS}$, in Fig. 4(b). White area corresponds to the region in which the device does not exhibit NDR (that is, $G_D > 0$). Blue areas present remarkable NDR regions of $G_D < -4$ nS. Negative G_D plotted on the $V_G - V_{DS}$ plane clearly shows the NDR behaviors.

4 Discussion

It is a straightforward hypothesis that the NDR is attributed to Coulomb blockade (CB) phenomena in the array of Au NPs. Electrical connections among three electrodes can be understood with a percolation model [20]. Whereas our previous samples, which were fabricated using 15-nm-diameter Au NPs, exhibited nonlinear current-voltage ($I - V$) characteristics only at low temperature (77 K) [20], we employed Au NPs of smaller sizes (diameters of 3 nm and 5 nm) in this work and raised the operation temperature to 298 K, at least. (We did not measure the device characteristics at temperatures higher than 298 K.)

As we described in the introduction, NDR features were investigated previously. There are two major types of mechanisms suggested for NDR in SE devices. The first one is a combination of an SE transistor and an

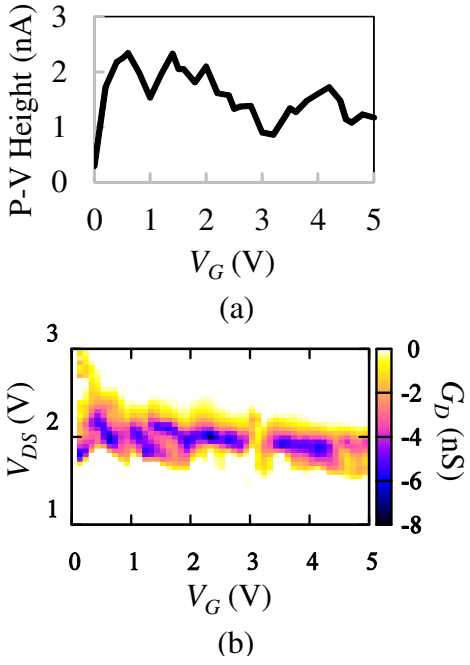

Fig. 4 (a) Heights (P-V height) between peak and valley points of the NDR plotted as a function of the gate voltage V_G. (b) Drain conductance, $G_D = dI_D/dV_{DS}$, plotted on the $V_{DS} - V_G$ plane

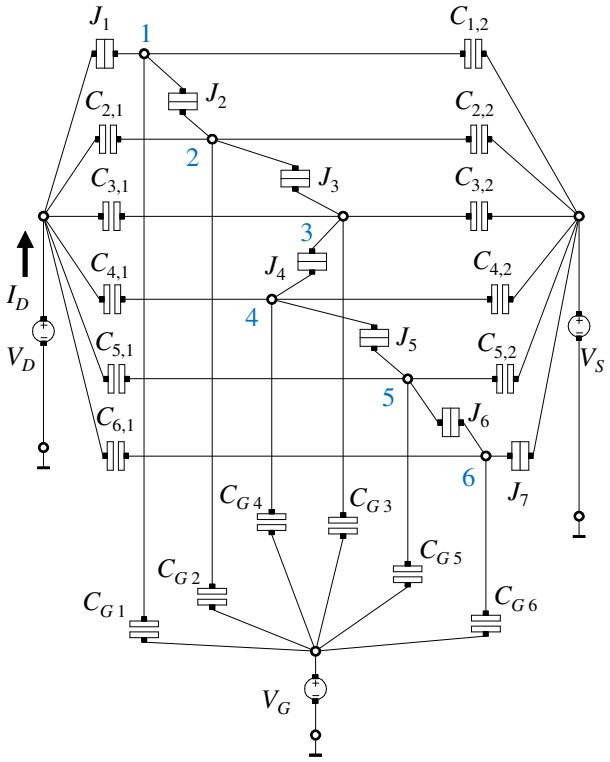

Fig. 5 Simulation model comprising three electrodes (the drain, source, and gate), 6 dots (labeled with blue numbers from 1 to 6), 7 tunnel junctions (J_1, J_2, ..., J_7), 10 coupling capacitors ($C_{i,j}$; $i = 1, 2, ..., 6$; $j = 1, 2$), and 6 gate capacitors (C_{G1}, C_{G2}, ..., C_{G6})

SE box, where the island of the SE box is coupled to the island of the SE transistor via a capacitor [9]. Although the SE transistor itself has no NDR in its $I-V$ characteristics, the charge in the SE box shifts the operation point, resulting in NDR. The second one is a one-dimensional array of small tunnel junctions in a multi-dot film [8]. When a part of the current path in the array is in the opposite direction, and when there is imbalance of tunnel resistances, NDR could be obtained because of a potential barrier in the array and asymmetric tunneling probability of electrons and holes.

Although it is difficult to determine the current paths in our device even by using SEM images, percolative connections of Au NPs suggest that NDR in our device could be understood using the second model. That is, current paths and tunnel resistances in our device are not supposed to be mono-directional nor uniform, which possibly induces NDR characteristics. Therefore, the situation is similar to the array model in [8]. Since the dependence of NDR properties on the gate voltage was not investigated in [8], we simulated it numerically.

We have simulated the circuit model shown in Fig. 5. The model is composed of 6 dots (1, 2, ..., 6) which play the role of islands. The positions of the dots 3 and 4 are in the opposite direction while other dots are placed in order. Each dot is capacitively coupled to the drain and source terminals via $C_{i,j}$ ($i = 1, 2, ..., 6$; $j = 1, 2$) whose values are chosen as described below. There are 7 tunnel junctions $J_1, J_2, ..., J_7$ on the path connecting between the drain and source terminals. The gate terminal is connected to each dot via a gate capacitance C_{Gi} with $i = 1, 2, .., 6$.

As described in [8], NDR phenomena are driven from the asymmetric distribution of the dots between the drain and source terminals. Under some conditions, this opposite electric field prevents electron tunneling, resulting in the NDR. In addition, variation of the tunnel resistance also affects the P-V height. Although there are several sets of parameters that reproduce NDR characteristics, we here present one set as follows: $C_{1,2} = C_{6,1} = C_0$; $C_{2,1} = C_{5,2} = 9C_0$; $C_{2,2} = C_{5,1} = 2C_0$; $C_{3,1} = C_{4,2} = 2C_0$; $C_{3,2} = C_{4,1} = 4C_0$, $C_{G1} = C_{G2} = ...C_{G6} = 0.1C_0$), the junction capacitance and resistance for J_1, J_2, J_3 are C_0 and R_0, those for J_4, J_5, J_6, J_7 are $0.5C_0$ and $2R_0$. All C_{Gi} are assumed to be identical, which means that the gate charges are coupled equally to all dots.

Monte-Carlo simulation was executed using SIMON program [21] in the conditions of 298 K and no co-tunneling. In the simulation model, the single-electron

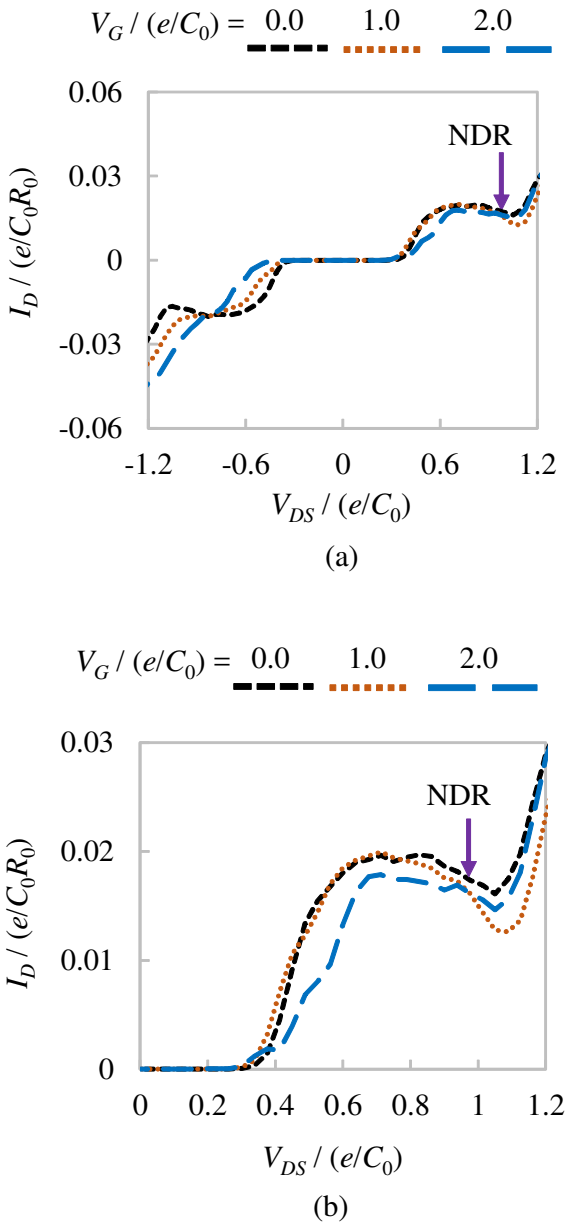

Fig. 6 Numerical $I_D - V_{DS}$ curves for $V_G/(e/C_0) = 0.0$, 1.0, and 2.0 at $T = 298$ K. $V_{DS}/(e/C_0)$ is swept from -1.2 to $+1.2$. (a) For $-1.2 \leq V_{DS}/(e/C_0) \leq +1.2$. (b) For $0 \leq V_{DS}/(e/C_0) \leq +1.2$

charging energy of the dot 2, $(E_C)_2 = e^2/2(C_{J_2}+C_{J_3}+C_{2,1}+C_{2,2}+C_{G2})$, is the smallest among the dots. Here, temperature T of 298 K is equivalent to $0.21(E_C)_2/k_B$, in which k_B is the Boltzmann constant. $I_D - V_{DS}$ characteristics for $V_G/(e/C_0)$ of 0.0, 1.0, and 2.0 are respectively presented by short dashed, dotted, and long dashed curves in Fig. 6. At $V_G/(e/C_0) = 0.0$, NDR features appear symmetric for both the positive and negative V_{DS}, which is different from the experimental result. For a finite $V_G/(e/C_0)$, NDR features become asymmetric and more noticeable at positive V_{DS}. In addition, it is confirmed that the P-V height is modulated by V_G.

As described above, the circuit model in Fig. 5 partly reproduces asymmetric, gate-tuned NDR phenomena observed in our device. Even though our model is extensively simplified in comparison with the real device, it suggests that random arrays of Au NPs could exhibit NDR phenomena.

5 Conclusion

In conclusion, we fabricated the SE device by using the relatively simple method of fabrication. The device exhibited the NDR phenomena at room temperature (298 K). Moreover, the NDR behavior was controlled by changing the gate voltage. The gate-tuned NDR characteristics were partially reproduced by simulating a simplified array of tunnel junctions.

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