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Fabrication of Resistively-Coupled Single-Electron Device Using an Array of Gold Nanoparticles

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Abstract We demonstrated one type of single-electron (SE) device that exhibited electrical characteristics similar to those of resistively-coupled SE transistor (R-SET) at 77 K and room temperature (287 K). Three Au electrodes on an oxidized Si chip served as drain, source, and gate electrodes were formed by using electron beam lithography (EBL) and evaporation techniques. A narrow (70-nm-wide) gate electrode was patterned by using thermal evaporation, whereas wide (800-nm-wide) drain and source electrodes were made by using shadow evaporation. Subsequently, aqueous solution of citric acid and 15-nm-diameter gold nanoparticles (Au NPs) and toluene solution of 3-nm-diameter Au NPs chemisorbed via decanethiol were dropped on the chip to make the connections between the electrodes. Current-voltage characteristics between the drain and source electrodes exhibited Coulomb blockade (CB) at both 77 K and 287 K. Dependence of the CB region on the gate voltage was similar to that of an R-SET. Simulation results of the model based on the scanning electron microscopy (SEM) image of the device could reproduce the characteristics like the R-SET.

Keywords Coulomb blockade (CB) · gold nanoparticles (Au NPs) · single-electron transistor (SET)

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1 Introduction

Single-electron (SE) devices [1,2] are promising candidates which are able to be combined with CMOS [3,4] or even replace CMOS in some future applications [5]. The nomenclature of "single-electron device" is defined that "a device operates based on the Coulomb blockade (CB) effect with the one-electron-precision charge transfer" [6]. This definition means that the number of electrons are transferred between the electrodes of the SE device might be a few hundred, although one or a few transferring electrons are usual for the SE device [6]. Recently, with the introduction of new materials (e.g., high-k gate dielectric) and emerging device structures (e.g., Double/Multi-Gate MOSFET, FinFET, Silicon-On-Nothing (SON), Vertical MOSFET, and Ballistic MOSFET), the tremendous progress in CMOS scaling has pushed CMOS into nanoscale [7,8]. Nevertheless, SE devices are able to compete with nanoscale CMOS [7] because of good scalability [3,4], ultra-low power consumption [7,9–11], and new functionalities related to SE charging effects such as the ability to control small numbers of electrons precisely [11–13], high programmability [14], multiple-valued operation [15], and super sensitivity [16].

The fundamental device in the field of single electronics is a single-electron transistor (SET) consisting of a small island between two tunnel junctions in series. Two typical types of SETs include capacitively-coupled SETs (C-SETs) and resistively-coupled SETs (R-SETs)

[17,18]. A C-SET with a gate capacitance exhibits periodic Coulomb diamonds whereas an R-SET with a gate resistance shows only one Coulomb diamond.

Although C-SETs have been realized in wide varieties of structures [19–27], a serious drawback of C-SET-based devices is that the operation point is sensitive to background charge fluctuations [18,28]. R-SETs do not suffer from this problem, in which a leakage of the initial background charge is passed through the gate resistor [18]. Moreover, R-SETs can achieve a high voltage gain [7,18]. These advantages make R-SETs prospective for applications in logic circuits as well as amplifiers [17,29].

In realization of R-SETs, the fabricated R-SETs have remained under a limitation of low operation temperature, such as sub-1-K [18], [30]−[32]. The purpose of this paper is to improve the operation temperature of the R-SET by using two types of gold nanoparticles (Au NPs), 15-nm-diameter and 3-nm-diameter Au NPs. Here, the 15-nm-diameter Au NPs were used to contribute the conductivity to the wide (200-nm-wide) gap between the drain and source electrodes whereas the 3-nm-diameter Au NPs were used to exhibit the large charging energy which allowed the device to operate at high temperature. Monte-Carlo simulation was executed using the SIMON program [33].

2 Fabrication method

The fabrication processes were as follows. Firstly, on an oxidized Si chip, a narrow (70-nm-wide) gate electrode was patterned by using standard electron-beam lithography (EBL) with a single PMMA resist, thermal evaporation of 10-nm-thick Au, and lift-off process. Secondly, drain and source electrodes were formed by using EBL with a PMMA/copolymer bi-layer resist, shadow evaporation of 20-nm-thick and 45-nm-thick Au, and lift-off process. Schematic drawing of the shadow evaporation process is described in Fig. 1. Thirdly, 5 μL of an aqueous solution of citric acid with 0.007 wt% of 15-nm-diameter Au NPs was dropped on the chip. Finally, 3 μL of a toluene solution with 0.1 wt% of 3-nm-diameter Au NPs chemisorbed via decanethiol [34, 35] was dropped on the chip.

Figure 2 shows scanning electron microscopy (SEM) images of the device after measurements. The narrow gate electrode has a 70-nm width. Both drain and source electrodes have the same width of 800 nm. In Fig. 2(b), it can be seen that Au NPs constitute a two-dimensional array between the drain and source electrodes. Because there are some voids shown by yellow arrows (Fig. 2(b)), the two-dimensional array was separated into four regions labeled as A, B, C, and D. In each region, each

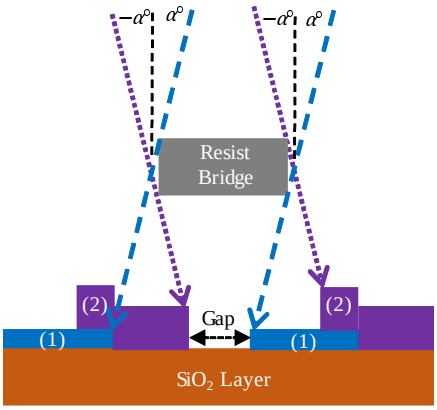


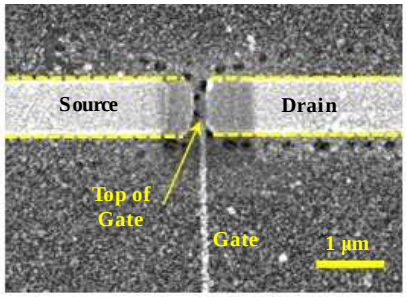
Fig. 1 Schematic drawing of a shadow evaporation process. The resist bridge is the remained part of the top layer of the bi-layer resist after development. The first layer which is shown by the symbol (1) and represented by blue color is firstly deposited from an angle of α degrees. Then the second layer which is shown by the symbol (2) and represented by purple color is deposited from another angle of $-\alpha$ degrees. The space between the second layer on the left side and the first layer on the right side is a gap between the source and drain electrodes in this experiment

yellow dashed line shows the shortest path containing Au NPs between the drain and source electrodes. From top to bottom, they are numbered from 1 to 4 and have lengths of 296 nm, 200 nm, 200 nm, and 206 nm, respectively. The gap ($\geq$ 200 nm) between the drain and source electrodes is relatively large in comparison with that in previous literature using Au NPs [25,26], which reduces the complexity in fabrication process. Besides, the path shown by the light-blue dotted curve is one of actual paths in each region (A, B, C, and D). The gate electrode penetrates 190 nm into the gap. It seems that the gate electrode is connected to the fourth path.

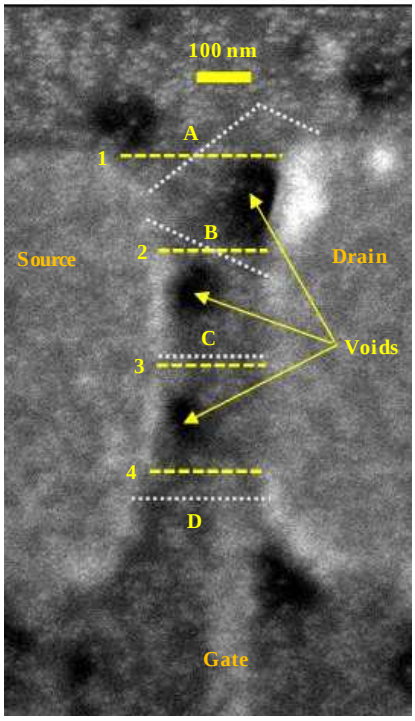
A measurement circuit was established using a semiconductor parameter analyzer (SPA) as shown in Fig. 3. A drain voltage V_D, a source voltage V_S, and a gate voltage V_G were applied to the drain, source, and gate electrodes, respectively. V_D and V_S were the same in magnitude and opposite in polarity. The measurements at 77 K were done by dipping the device into liquid nitrogen. At room temperature (287 K), the device was exposed in the air.

3 Characteristics at 77 K

Figure 4 illustrates the relationships between currents and drain−source voltage V_{DS} ($= V_D - V_S$) of the device at 77 K. In Fig. 4(a), drain currents I_D at different gate voltages V_G of −25 V, 0 V, and +25 V are shown by blue dashed, black solid, and dark-orange dotted curves, respectively. At V_G = 0 V, a Coulomb blockade (CB)



(a)



(b)

Fig. 2 (a) Scanning electron microscopy (SEM) image of the device after measurements. There are three electrodes including drain, source, and gate electrodes. For clarity, edges of the drain and source electrodes are shown by yellow dashed lines. Top position of the gate electrode inside the gap between the drain and source electrodes is illustrated by a yellow arrow. (b) Magnified image around the gap between the drain and source electrodes. Because of voids shown by yellow arrows, there are four regions labeled as A, B, C, and D. For each region, the shortest path containing Au NPs between the drain and source electrodes is represented by the yellow dashed line. From top to bottom, they are numbered from 1 to 4. Besides, the path shown by the light-blue dotted curve is one of actual paths in each region (A, B, C, and D)

region is observed between V_{DS} of -5.1 V and $+4.0$ V (namely, $|I_D| < 0.05$ nA for -5.1 V $< V_{DS} < +4.0$ V). At $V_G = \pm 25$ V, the CB region is not observed. I_D, at $V_{DS} = 0$ V, are 1.7 nA and -1.4 nA for V_G of -25 V and $+25$ V, respectively. This means that there is the current flowing through the device as V_G is applied

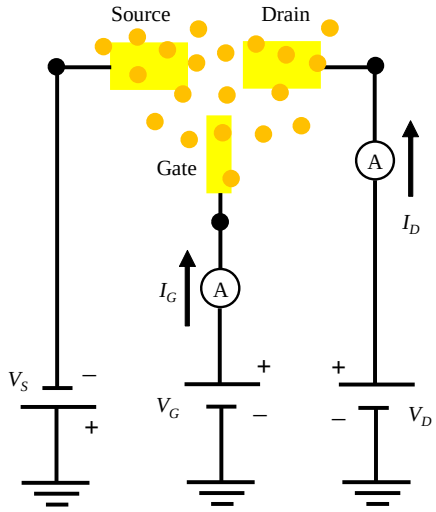


Fig. 3 Set-up of measurement by using a semiconductor parameter analyzer (SPA). Drain, source, and gate electrodes are shown by yellow rectangles. Au NPs are represented by orange solid circles which distribute randomly among the electrodes

to the device. Gate currents I_G at V_G of -25 V, 0 V, and $+25$ V are respectively represented by blue dashed, black solid, and dark-orange dotted curves in Fig. 4(b). The absolute gate current $|I_G|$ is less than 0.03 nA at $V_G = 0$ V. Yet, for V_G of -25 V and $+25$ V, I_G are respectively -1.7 nA and $+1.6$ nA. This means that I_G flows through the device when V_G is applied to the device.

A survey of I_D on the $V_{DS} - V_G$ plane is shown in Fig. 5. White and black areas represent the ranges of I_D above $+0.8$ nA and below -0.8 nA, respectively. The CB region ($|I_D| < 0.05$ nA) is described by a pink area. It is observed that there is only one Coulomb area on the whole range of V_G from -35 V to $+35$ V. Therefore, the electrical characteristics at 77 K are categorized into those of an R-SET.

4 Characteristics at room temperature

Current−voltage characteristics of the device at 287 K are illustrated in Fig. 6. In Fig. 6(a), I_D plotted as functions of V_{DS} at different V_G of -25 V, 0 V, and $+25$ V. The measured range of V_{DS} at 287 K is smaller than that at 77 K to avoid breaking the device during the measurements at high temperature. At $V_G = 0$ V, I_D represented by a black solid curve exhibits the CB region between V_{DS} of -3.2 V and $+2.0$ V (namely, $|I_D| < 0.05$ nA for -3.2 V $< V_{DS} < +2.0$ V), which is narrower than that at 77 K because of thermal fluctuations [2]. At $V_G = \pm 25$ V, there is no CB region. Figure 6(b) illustrates I_G versus V_{DS} at different V_G of -25 V, 0 V,

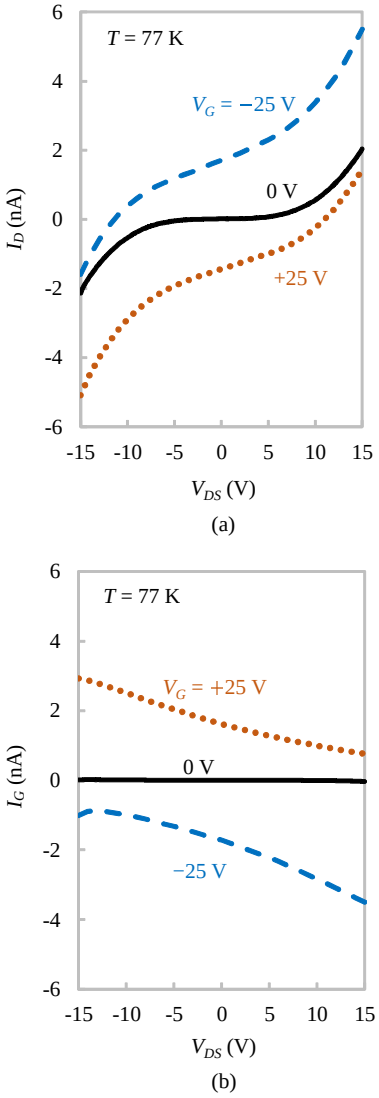


Fig. 4 Measured current−voltage characteristics at 77 K. (a) Drain currents I_D versus drain−source voltage V_{DS} for gate voltages V_G of −25 V, 0 V, and +25 V (from top to bottom). (b) Gate currents I_G plotted as functions of V_{DS} at different V_G of −25 V, 0 V, and +25 V (from bottom to top)

and +25 V. At $V_G = 0$ V, $|I_G|$ is smaller than 0.3 nA. However, at $V_G = \pm$ 25 V, $|I_G|$ reaches a few nA, i.e., I_G flows through the device at 287 K.

Figure 7 shows I_D plotted on the $V_{DS} - V_G$ plane at 287 K. The CB region is represented by a pink area. It can be seen that only one CB region is observed on the whole range of V_G from −35 V to +35 V. The electrical characteristics of the device at 287 K also indicates the properties of an R-SET. The characteristics of the device at 287 K are more complicated than those at 77 K, in which current fluctuations are observed. The fluctuations can arise from the complex connections of Au NPs between the drain and source electrodes and

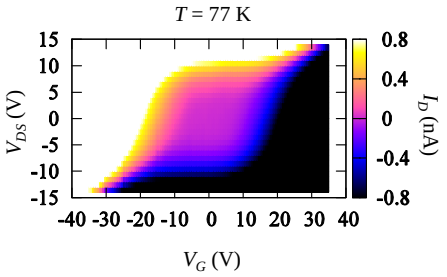


Fig. 5 Measured drain currents I_D plotted as functions of drain−source voltage V_{DS} and gate voltage V_G at 77 K. I_D amplitude is presented as in color bar. White and black areas respectively show I_D above +0.8 nA and below −0.8 nA

the different effects of temperature on the properties of Au NPs between 77 K and 287 K.

5 Discussion

From the viewpoint of charging energies, although the device was formed by both of 15-nm-diameter and 3-nm-diameter Au NPs, we assume that 3-nm Au NPs coated by decanethiol contribute to the nonlinear characteristics while 15-nm Au NPs work as linearly-conductive bridges. The reason for this assumption arises from that the smaller NPs has the larger charging energies [36]. For simplicity, each 3-nm-diameter Au NP chemisorbed via decanethiol and surrounded by several other 3-nm-diameter Au NPs is assumed as a core sphere (radius r_0 of 1.5 nm) isolated from a conducting layer (thickness r_2 of 1.5 nm) by an dielectric layer (thickness r_1 of 1 nm, dielectric constant ε_d). Then, such the unit has a total diameter of 8 nm as shown in Fig. 8. In Fig. 2(b), for simplicity, we consider the shortest paths containing Au NPs between the drain and source electrodes, which are shown by the yellow dashed lines. The paths 1, 2, 3, and 4 have the lengths of 296 nm, 200 nm, 200 nm, and 206 nm, respectively. This means that the paths 1, 2, 3, and 4 have 37 units, 25 units, 25 units, and 25 units, respectively. (Number of units on each path is chosen to be an integer.)

In Fig. 8, an island electrode, a core sphere, has the capacitance C_{island} as follows [36],

$$C_{island} = 4\pi\varepsilon_0\varepsilon_d \frac{r_0(r_0 + r_1)}{r_1}. \quad (1)$$

Here, ε_0 is the vacuum permittivity (8.854×10^{-12} F/m); ε_d is the dielectric constant of alkanethiol (2.6) [26]. As a result, C_{island} is 1.08 aF.

Figure 9 describes the simulation model. We built a simulation model based on the structure of the device in Fig. 2. Firstly, our model composed of three terminals

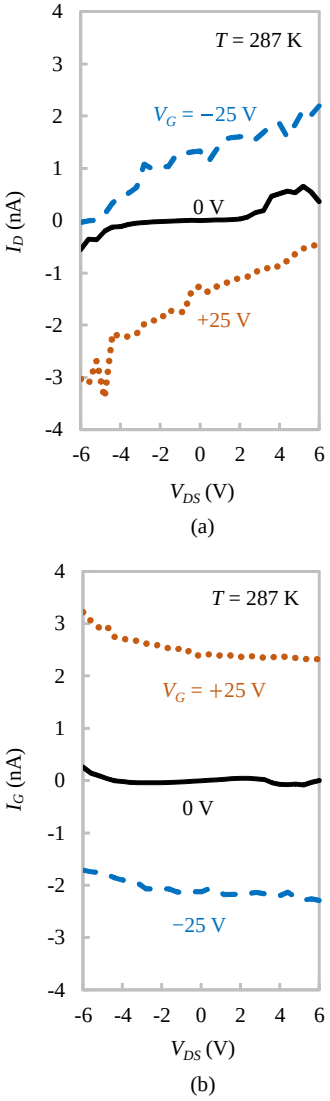


Fig. 6 Measured current−voltage characteristics at room temperature (287 K). (a) Drain currents I_D versus drain−source voltage V_{DS} for gate voltages V_G of −25 V, 0 V, and +25 V (from top to bottom). (b) Gate currents I_G plotted as functions of V_{DS} at different V_G of −25 V, 0 V, and +25 V (from bottom to top)

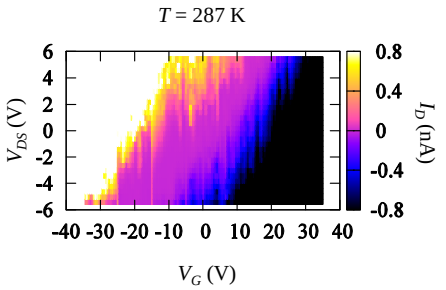


Fig. 7 Measured drain currents I_D plotted as functions of drain−source voltage V_{DS} and gate voltage V_G at room temperature (287 K). I_D amplitude is presented as in color bar. White and black areas respectively show I_D above +0.8 nA and below −0.8 nA

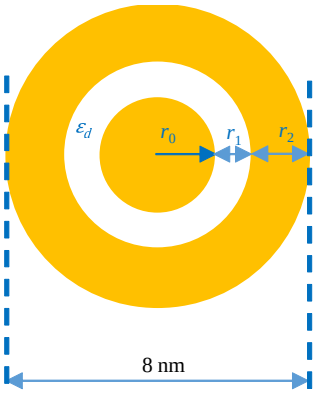


Fig. 8 Each 3-nm-diameter Au NP chemisorbed via decanethiol and surrounded by several other 3-nm-diameter Au NPs is assumed as a core sphere (radius r_0 of 1.5 nm) isolated from a conducting layer (thickness r_2 of 1.5 nm) by a dielectric layer (thickness r_1 of 1 nm, dielectric constant ε_d). Such the unit has a total diameter of 8 nm. Here, for each 3-nm-diameter Au NP surrounding the core sphere, it is assumed that half of the Au NP contributes to the conducting layer of this unit while the other half participates in the conducting layer of the neighbor unit

was derived from the three-electrode device structure. Secondly, four shortest paths containing Au NPs were simplified to four parallel branches consisting of island electrodes and tunnel junctions. The first branch was assumed to have 37 island electrodes whereas the other branches were assumed to have 25 island electrodes on each branch. Each island electrode was assumed to connect to two tunnel junctions. Then, there were 38 tunnel junctions on the first branch and 26 tunnel junctions on the other branches. Finally, because the gate electrode was connected to the fourth path (Fig. 2(b)), we assumed that the gate electrode was resistively connected to the fourth branch. Arrangements of the tunnel junctions could be considered as a matrix of elements $J_{i,j}$, in which i was the position of the branch from top to bottom and j was the position of the tunnel junction from left to right on each branch. The gate resistor (R_G) was connected to the center of the fourth branch, i.e., it was connected to the 13^{th} island electrode. The drain voltage V_D and source voltage V_S were in the same magnitude and opposite in polarity. Direction of drain current I_D was shown by the arrow.

Values of parameters in the simulation model were determined as follows. We assumed that each tunnel junction on the i^{th} branch had a tunnel capacitance C_i and a tunnel resistance R_i, with $i = 1, 2, 3, 4$. In Fig. 2, it was observed that differences between lengths of the actual paths (light-blue dotted curves) and lengths

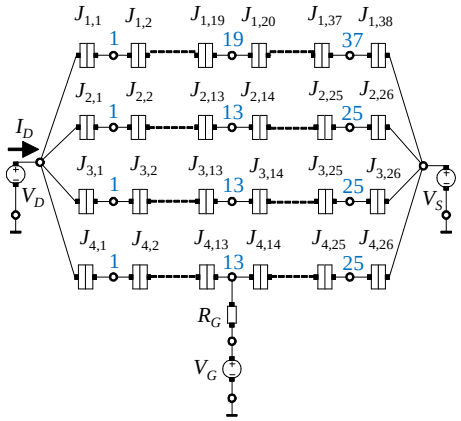


Fig. 9 Simulation model is composed of four parallel branches. The first branch consists of 37 islands (labeled with blue numbers from 1 to 37) and 38 tunnel junctions ($J_{1,1}, J_{1,2}, ..., J_{1,38}$) in series. Three other branches consist of 25 islands (labeled with blue numbers from 1 to 25) and 26 tunnel junctions ($J_{i,1}, J_{i,2}, ..., J_{i,26}$ with i = 2, 3, 4) in series. A gate resistor R_G connects to the 13^{th} island on the fourth branch

of the shortest paths (yellow dashed lines) in regions A, B, and C were in descending order. In addition, these differences in regions B and D were similar. Hence, to compensate these differences, we assumed that $R_1 > R_2$, $R_2 = R_4$, $R_2 > R_3$, $C_1 < C_2$, $C_2 = C_4$, and $C_2 < C_3$. Firstly, according to Eq. (1), each island electrode has C_{island} of 1.08 aF. We assumed that the value of C_{island} was applied for each island on the branch 3. Then, C_3 was evaluated as $C_{island}/2$ which was approximately 0.50 aF; C_1, C_2, and C_4 were respectively chosen as 0.10 aF, 0.20 aF, and 0.20 aF. Secondly, to ensure that the simulated I_D approaches the measured I_D at V_G of 0 V in Figs. 4(a) and 6(a), the resistances R_1, R_2, R_3, and R_4 were selected as 0.60 GΩ, 0.55 GΩ, 0.45 GΩ, and 0.55 GΩ, respectively. Finally, the gate resistance R_G was tuned to reproduce the slope of I_D on the $V_{DS} - V_G$ plane (Figs. 5 and 7), which was chosen as 3.00 GΩ. Simulation was executed by using Monte-Carlo method in the condition of no cotunneling.

Figures 10(a) and (b) compare the simulated I_D with the measured I_D at 77 K and 287 K, respectively. Here, V_G is set at 0 V. The simulated I_D is represented by dark-orange dashed curve whereas the measured I_D is shown by blue dotted curve. It is observed that the simulation results can reproduce the CB regions of the experimental data. Outside the CB regions, the experimental curves change more gradually than the simulation curves, because the distribution of Au NPs in the fabricated device is not as uniform as the above assumption.

Figures 11 and 12 respectively show I_D plotted on the $V_{DS} - V_G$ plane at 77 K and 287 K. The CB regions

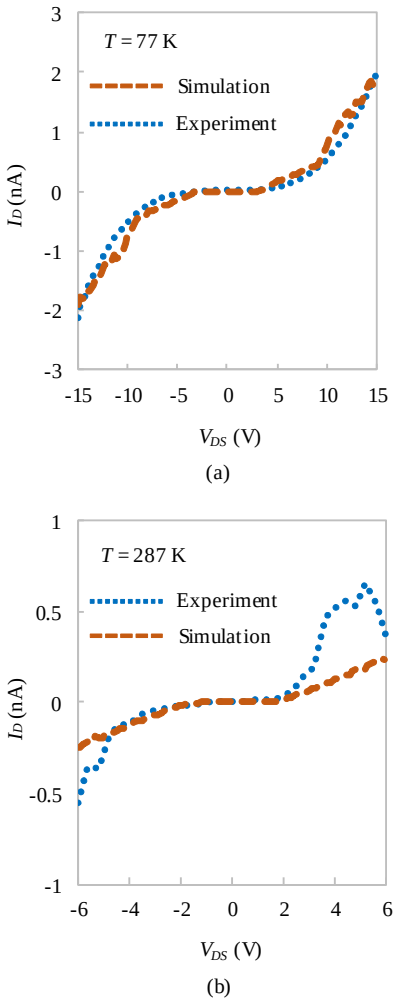


Fig. 10 Simulated and measured drain currents I_D are plotted as functions of drain−source voltage V_{DS} at gate voltage V_G of 0 V. (a) T = 77 K. (b) T = 287 K

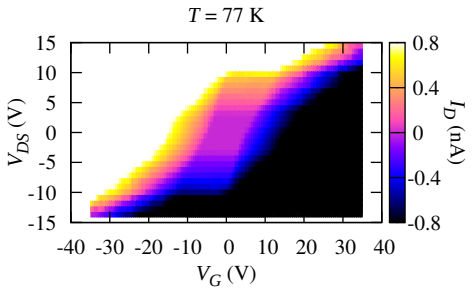


Fig. 11 Simulated drain current curves I_D on the $V_{DS} - V_G$ plane at 77 K. I_D amplitude is presented as in color bar. White area illustrates I_D above +0.8 nA, whereas black area represents I_D below −0.8 nA

are represented by pink areas. By changing V_G, electrical characteristics in Figs. 11 and 12 including only one Coulomb area observed on the whole range of V_G and

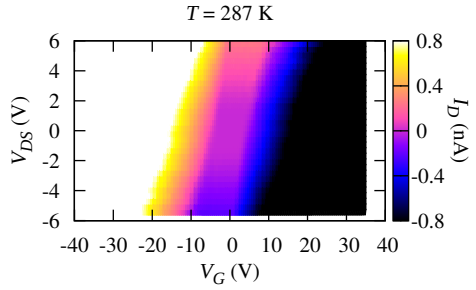


Fig. 12 Simulated drain current curves I_D on the $V_{DS} - V_G$ plane at 287 K. I_D amplitude is presented as in color bar. White area illustrates I_D above +0.8 nA, whereas black area represents I_D below −0.8 nA

the slope of I_D on the $V_{DS} - V_G$ plane look like the experimental data shown in Figs. 5 and 7, respectively.

6 Conclusion

We have realized the SE device by using Au NPs. The narrow gate electrode was first fabricated and followed by the drain and source electrodes by combination EBL and evaporation. Au NPs were used to make the connections between the electrodes. The electrical characteristics of the device observed at 77 K and room temperature (287 K) were similar to those of the R-SET. Based on the SEM image of the device, we built the simulation model whose results can reproduce the characteristics like the R-SET at 77 K and 287 K.

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